# *Sitronix*

## ST7735

### *262K Color Single-Chip TFT Controller/Driver*

## 1  Introduction

The ST7735 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 396 source line and 162 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bit/9-bit/16-bit/18-bit parallel interface. Display data can be stored in the on-chip display data RAM of 132 x 162 x 18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

## 2  Features

**Single chip TFT-LCD Controller/Driver with RAM**
**On-chip Display Data RAM (i.e. Frame Memory)**
  -132 (H) x RGB x 162 (V) bits
**LCD Driver Output Circuits:**
  -Source Outputs: 132 RGB channels
  -Gate Outputs: 162 channels
  -Common electrode output
**Display Resolution**
  -132 (RGB) x 162
    (GM[2:0]= "000", DDRAM: 132 x 18-bits x 162)
  -128 (RGB) x 160
    (GM[2:0]= "011", DDRAM: 128 x 18-bits x 160)
**Display Colors (Color Mode)**
  -Full Color: 262K, RGB=(666) max., Idle Mode OFF
  -Color Reduce: 8-color, RGB=(111), Idle Mode ON
**Programmable Pixel Color Format (Color Depth) for Various Display Data input Format**
  -12-bit/pixel: RGB=(444) using the 384k-bit frame
    memory and LUT
  -16-bit/pixel: RGB=(565) using the 384k-bit frame
    memory and LUT
  -18-bit/pixel: RGB=(666) using the 384k-bit frame
    memory and LUT
**Various Interfaces**
  -Parallel 8080-series MCU Interface
    (8-bit, 9-bit, 16-bit & 18-bit)
  -3-line serial interface
  -4-line serial interface
**Display Features**
  -Programmable partial display duty
  -Line inversion, frame inversion
  -Support both normal-black & normal-white LC
  -Software programmable color depth mode

**Built-in Circuits**
  -DC/DC converter
  -Adjustable VCOM generation
  -Non-volatile (NV) memory to store initial register setting
  -Oscillator for display clock generation
  -Factory default value (module ID, module version, etc)
    are stored in NV memory
  -Timing controller
**Built-in NV Memory for LCD Initial Register Setting**
  -7-bits for ID2
  -8-bits for ID3
  -7-bits for VCOM adjustment
**Wide Supply Voltage Range**
  -I/O Voltage (VDDI to DGND): 1.65V~VDD
    (VDDI ≤ VDD)
  -Analog Voltage (VDD to AGND): 2.6V~3.3V
**On-Chip Power System**
  -Source Voltage (GVDD to AGND): 3.0V~5.0V
  -VCOM HIGH level (VCOMH to AGND): 2.5V to 5.0V
  -VCOM LOW level (VCOML to AGND): -2.4V to 0.0V
  -Gate driver HIGH level (VGH to AGND):
    +10.0V to +15V
  -Gate driver LOW level (VGL to AGND):
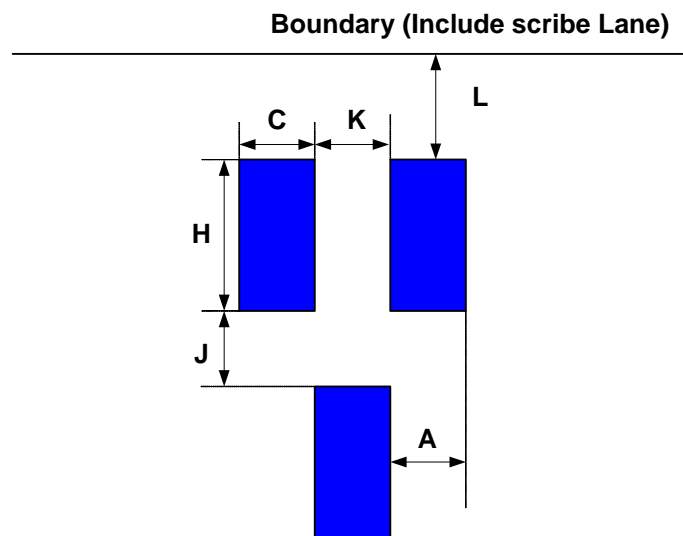    -12.4V to -7.5V
**Operating Temperature: -30℃ to +85℃**

| **ST7735** | **Parallel Interface: 8-bit/9-bit/16-bit/18-bit**<br>**Serial Interface: 3-line/4-line** | ST |

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# ST7735

## 3 Pad arrangement

### 3.1 Output Bump Dimension

**Boundary (Include scribe Lane)**



| Item | Symbol | Size |
|---|---|---|
| Bump pitch | A | 16 um |
| Bump width | C | 16 um |
| Bump height | H | 98 um |
| Bump gap1 (Vertical) | J | 19 um |
| Bump gap2 (Horizontal) | K | 16 um |
| Bump area | C x H | 1568 um2 |
| Chip Boundary (include scribe Lane) | L | 59 um |

# ST7735

**3.2 Input Bump Dimension**
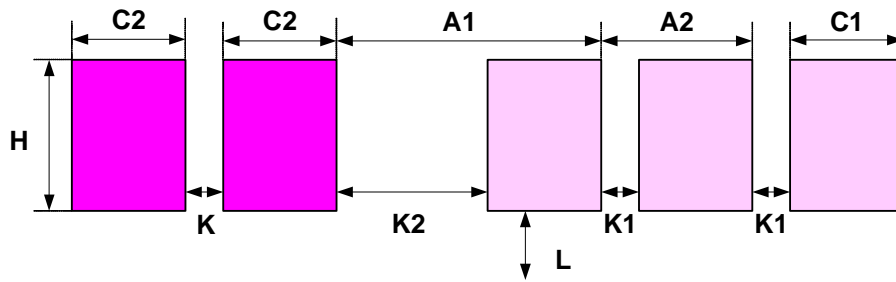


**Boundary (Include scribe Lane)**

| Item | Symbol | Size |
|---|---|---|
| Bump pitch 1 | A1 | 67 um |
| Bump pitch 2 | A2 | 50 um |
| Bump width 1 | C1 | 35 um |
| Bump width 2 | C2 | 40 um |
| Bump height | H | 90 um |
| Bump gap | K | 20 um |
| Bump gap1 | K1 | 15 um |
| Bump gap2 | K2 | 32 um |
| Bump area 1 | C1 X H | 3150 um2 |
| Bump area 2 | C2 X H | 3690 um2 |
| Chip Boundary(include scribe Lane) | L | 59 um |

### 3.3  Alignment Mark Dimension
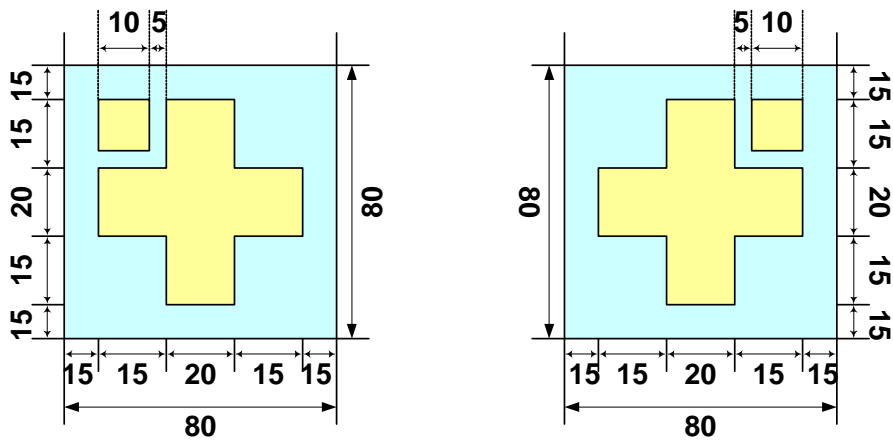


### 3.4  Chip Information

Chip size (um x um): 9900 x 670
PAD coordinate: pad center
Coordinate origin: chip center
Chip thickness (um): 300 (TYP)
Bump height (um): 15 (TYP)
Bump hardness (HV): 75 (TYP)

## 4   Pad Center Coordinates

| No. | PAD Name | X | Y | No. | PAD Name | X | Y | No. | PAD Name | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | DUMMY | -4750 | -231 | 51 | VDD | -2250 | -231 | 101 | DGND | 550 | -231 |
| 2 | VDDIO | -4700 | -231 | 52 | VDD | -2200 | -231 | 102 | DGND | 600 | -231 |
| 3 | EXTC | -4650 | -231 | 53 | VDD | -2150 | -231 | 103 | VDDI | 650 | -231 |
| 4 | DGNDO | -4600 | -231 | 54 | VDD | -2100 | -231 | 104 | VDDI | 700 | -231 |
| 5 | IM0 | -4550 | -231 | 55 | VDD | -2050 | -231 | 105 | VDDI | 750 | -231 |
| 6 | VDDIO | -4500 | -231 | 56 | VDD | -2000 | -231 | 106 | VDDI | 800 | -231 |
| 7 | IM1 | -4450 | -231 | 57 | AGND | -1950 | -231 | 107 | VDDI | 850 | -231 |
| 8 | DGNDO | -4400 | -231 | 58 | AGND | -1900 | -231 | 108 | VDDI | 900 | -231 |
| 9 | DUMMY | -4350 | -231 | 59 | AGND | -1850 | -231 | 109 | VCC | 950 | -231 |
| 10 | VDDIO | -4300 | -231 | 60 | AGND | -1800 | -231 | 110 | VCC | 1000 | -231 |
| 11 | TPI[1] | -4250 | -231 | 61 | AGND | -1750 | -231 | 111 | VCCO | 1050 | -231 |
| 12 | DGNDO | -4200 | -231 | 62 | AGND | -1700 | -231 | 112 | VCI1 | 1100 | -231 |
| 13 | TPI[2] | -4150 | -231 | 63 | RDX | -1630 | -231 | 113 | VCI1 | 1150 | -231 |
| 14 | VDDIO | -4100 | -231 | 64 | D/CX | -1570 | -231 | 114 | VCI1 | 1200 | -231 |
| 15 | SRGB | -4050 | -231 | 65 | TESEL | -1510 | -231 | 115 | VREF | 1250 | -231 |
| 16 | DGNDO | -4000 | -231 | 66 | DGNDO | -1450 | -231 | 116 | VREF | 1300 | -231 |
| 17 | SMX | -3950 | -231 | 67 | D17 | -1390 | -231 | 117 | VREF | 1350 | -231 |
| 18 | VDDIO | -3900 | -231 | 68 | D16 | -1330 | -231 | 118 | DUMMY | 1400 | -231 |
| 19 | SMY | -3850 | -231 | 69 | D15 | -1270 | -231 | 119 | DUMMY | 1450 | -231 |
| 20 | DGNDO | -3800 | -231 | 70 | D14 | -1210 | -231 | 120 | AVDD | 1500 | -231 |
| 21 | DUMMY | -3750 | -231 | 71 | D13 | -1150 | -231 | 121 | AVDD | 1550 | -231 |
| 22 | VDDIO | -3700 | -231 | 72 | D12 | -1090 | -231 | 122 | AVDD | 1600 | -231 |
| 23 | DUMMY | -3650 | -231 | 73 | D11 | -1030 | -231 | 123 | AVDDO | 1650 | -231 |
| 24 | DGNDO | -3600 | -231 | 74 | D10 | -970 | -231 | 124 | AVDDO | 1700 | -231 |
| 25 | DUMMY | -3550 | -231 | 75 | D9 | -910 | -231 | 125 | GVDD | 1750 | -231 |
| 26 | VDDIO | -3500 | -231 | 76 | D8 | -850 | -231 | 126 | GVDD | 1800 | -231 |
| 27 | DUMMY | -3450 | -231 | 77 | D1 | -790 | -231 | 127 | GVDD | 1850 | -231 |
| 28 | DGNDO | -3400 | -231 | 78 | D3 | -730 | -231 | 128 | DUMMY | 1900 | -231 |
| 29 | DUMMY | -3350 | -231 | 79 | D5 | -670 | -231 | 129 | DUMMY | 1950 | -231 |
| 30 | VDDIO | -3300 | -231 | 80 | D7 | -610 | -231 | 130 | C11P | 2000 | -231 |
| 31 | LCM | -3250 | -231 | 81 | TE | -550 | -231 | 131 | C11P | 2050 | -231 |
| 32 | DGNDO | -3200 | -231 | 82 | RESX | -490 | -231 | 132 | C11P | 2100 | -231 |
| 33 | DUMMY | -3150 | -231 | 83 | CSX | -430 | -231 | 133 | C11P | 2150 | -231 |
| 34 | VDDIO | -3100 | -231 | 84 | D6 | -370 | -231 | 134 | C11N | 2200 | -231 |
| 35 | GM2 | -3050 | -231 | 85 | D4 | -310 | -231 | 135 | C11N | 2250 | -231 |
| 36 | DGNDO | -3000 | -231 | 86 | D2 | -250 | -231 | 136 | C11N | 2300 | -231 |
| 37 | GM1 | -2950 | -231 | 87 | IM2 | -190 | -231 | 137 | C11N | 2350 | -231 |
| 38 | VDDIO | -2900 | -231 | 88 | D0 | -130 | -231 | 138 | C12P | 2400 | -231 |
| 39 | GM0 | -2850 | -231 | 89 | WRX | -70 | -231 | 139 | C12P | 2450 | -231 |
| 40 | DGNDO | -2800 | -231 | 90 | DUMMY | 0 | -231 | 140 | C12P | 2500 | -231 |
| 41 | DUMMY | -2750 | -231 | 91 | DUMMY | 50 | -231 | 141 | C12P | 2550 | -231 |
| 42 | GS | -2700 | -231 | 92 | DUMMY | 100 | -231 | 142 | C12N | 2600 | -231 |
| 43 | SPI4W | -2650 | -231 | 93 | DUMMY | 150 | -231 | 143 | C12N | 2650 | -231 |
| 44 | VDDIO | -2600 | -231 | 94 | TPO[3] | 200 | -231 | 144 | C12N | 2700 | -231 |
| 45 | TPO[8] | -2550 | -231 | 95 | TPO[2] | 250 | -231 | 145 | C12N | 2750 | -231 |
| 46 | TPO[7] | -2500 | -231 | 96 | TPO[1] | 300 | -231 | 146 | AGND | 2800 | -231 |
| 47 | TPO[6] | -2450 | -231 | 97 | DGND | 350 | -231 | 147 | AGND | 2850 | -231 |
| 48 | TPO[5] | -2400 | -231 | 98 | DGND | 400 | -231 | 148 | AGND | 2900 | -231 |
| 49 | TPO[4] | -2350 | -231 | 99 | DGND | 450 | -231 | 149 | VCL | 2950 | -231 |
| 50 | OSC | -2300 | -231 | 100 | DGND | 500 | -231 | 150 | VCL | 3000 | -231 |

| No. | PAD Name | X | Y | No. | PAD Name | X | Y | No. | PAD Name | X | Y |
|-----|----------|------|------|-----|----------|------|------|-----|----------|------|------|
| 151 | VCL | 3050 | -231 | 201 | G136 | 4532 | 227 | 251 | G36 | 3732 | 227 |
| 152 | C41P | 3100 | -231 | 202 | G134 | 4516 | 110 | 252 | G34 | 3716 | 110 |
| 153 | C41P | 3150 | -231 | 203 | G132 | 4500 | 227 | 253 | G32 | 3700 | 227 |
| 154 | C41P | 3200 | -231 | 204 | G130 | 4484 | 110 | 254 | G30 | 3684 | 110 |
| 155 | C41N | 3250 | -231 | 205 | G128 | 4468 | 227 | 255 | G28 | 3668 | 227 |
| 156 | C41N | 3300 | -231 | 206 | G126 | 4452 | 110 | 256 | G26 | 3652 | 110 |
| 157 | C41N | 3350 | -231 | 207 | G124 | 4436 | 227 | 257 | G24 | 3636 | 227 |
| 158 | C22P | 3400 | -231 | 208 | G122 | 4420 | 110 | 258 | G22 | 3620 | 110 |
| 159 | C22P | 3450 | -231 | 209 | G120 | 4404 | 227 | 259 | G20 | 3604 | 227 |
| 160 | C22P | 3500 | -231 | 210 | G118 | 4388 | 110 | 260 | G18 | 3588 | 110 |
| 161 | C22N | 3550 | -231 | 211 | G116 | 4372 | 227 | 261 | G16 | 3572 | 227 |
| 162 | C22N | 3600 | -231 | 212 | G114 | 4356 | 110 | 262 | G14 | 3556 | 110 |
| 163 | C22N | 3650 | -231 | 213 | G112 | 4340 | 227 | 263 | G12 | 3540 | 227 |
| 164 | C23P | 3700 | -231 | 214 | G110 | 4324 | 110 | 264 | G10 | 3524 | 110 |
| 165 | C23P | 3750 | -231 | 215 | G108 | 4308 | 227 | 265 | G8 | 3508 | 227 |
| 166 | C23P | 3800 | -231 | 216 | G106 | 4292 | 110 | 266 | G6 | 3492 | 110 |
| 167 | C23N | 3850 | -231 | 217 | G104 | 4276 | 227 | 267 | G4 | 3476 | 227 |
| 168 | C23N | 3900 | -231 | 218 | G102 | 4260 | 110 | 268 | G2 | 3460 | 110 |
| 169 | C23N | 3950 | -231 | 219 | G100 | 4244 | 227 | 269 | DUMMY | 3444 | 227 |
| 170 | VGL | 4000 | -231 | 220 | G98 | 4228 | 110 | 270 | DUMMY | 3428 | 110 |
| 171 | VGL | 4050 | -231 | 221 | G96 | 4212 | 227 | 271 | DUMMY | 3412 | 227 |
| 172 | VGL | 4100 | -231 | 222 | G94 | 4196 | 110 | 272 | DUMMY | 3396 | 110 |
| 173 | VGH | 4150 | -231 | 223 | G92 | 4180 | 227 | 273 | S396 | 3380 | 227 |
| 174 | VGH | 4200 | -231 | 224 | G90 | 4164 | 110 | 274 | S395 | 3364 | 110 |
| 175 | VGHO | 4250 | -231 | 225 | G88 | 4148 | 227 | 275 | S394 | 3348 | 227 |
| 176 | VCOMH | 4300 | -231 | 226 | G86 | 4132 | 110 | 276 | S393 | 3332 | 110 |
| 177 | VCOMH | 4350 | -231 | 227 | G84 | 4116 | 227 | 277 | S392 | 3316 | 227 |
| 178 | VCOMH | 4400 | -231 | 228 | G82 | 4100 | 110 | 278 | S391 | 3300 | 110 |
| 179 | VCOML | 4450 | -231 | 229 | G80 | 4084 | 227 | 279 | S390 | 3284 | 227 |
| 180 | VCOML | 4500 | -231 | 230 | G78 | 4068 | 110 | 280 | S389 | 3268 | 110 |
| 181 | VCOML | 4550 | -231 | 231 | G76 | 4052 | 227 | 281 | S388 | 3252 | 227 |
| 182 | VCOM | 4600 | -231 | 232 | G74 | 4036 | 110 | 282 | S387 | 3236 | 110 |
| 183 | VCOM | 4650 | -231 | 233 | G72 | 4020 | 227 | 283 | S386 | 3220 | 227 |
| 184 | VCOM | 4700 | -231 | 234 | G70 | 4004 | 110 | 284 | S385 | 3204 | 110 |
| 185 | DUMMY | 4750 | -231 | 235 | G68 | 3988 | 227 | 285 | S384 | 3188 | 227 |
| 186 | DUMMY | 4772 | 110 | 236 | G66 | 3972 | 110 | 286 | S383 | 3172 | 110 |
| 187 | DUMMY | 4756 | 227 | 237 | G64 | 3956 | 227 | 287 | S382 | 3156 | 227 |
| 188 | G162 | 4740 | 110 | 238 | G62 | 3940 | 110 | 288 | S381 | 3140 | 110 |
| 189 | G160 | 4724 | 227 | 239 | G60 | 3924 | 227 | 289 | S380 | 3124 | 227 |
| 190 | G158 | 4708 | 110 | 240 | G58 | 3908 | 110 | 290 | S379 | 3108 | 110 |
| 191 | G156 | 4692 | 227 | 241 | G56 | 3892 | 227 | 291 | S378 | 3092 | 227 |
| 192 | G154 | 4676 | 110 | 242 | G54 | 3876 | 110 | 292 | S377 | 3076 | 110 |
| 193 | G152 | 4660 | 227 | 243 | G52 | 3860 | 227 | 293 | S376 | 3060 | 227 |
| 194 | G150 | 4644 | 110 | 244 | G50 | 3844 | 110 | 294 | S375 | 3044 | 110 |
| 195 | G148 | 4628 | 227 | 245 | G48 | 3828 | 227 | 295 | S374 | 3028 | 227 |
| 196 | G146 | 4612 | 110 | 246 | G46 | 3812 | 110 | 296 | S373 | 3012 | 110 |
| 197 | G144 | 4596 | 227 | 247 | G44 | 3796 | 227 | 297 | S372 | 2996 | 227 |
| 198 | G142 | 4580 | 110 | 248 | G42 | 3780 | 110 | 298 | S371 | 2980 | 110 |
| 199 | G140 | 4564 | 227 | 249 | G40 | 3764 | 227 | 299 | S370 | 2964 | 227 |
| 200 | G138 | 4548 | 110 | 250 | G38 | 3748 | 110 | 300 | S369 | 2948 | 110 |

| No. | PAD Name | X | Y |
|-----|----------|------|-----|
| 301 | S368 | 2932 | 227 |
| 302 | S367 | 2916 | 110 |
| 303 | S366 | 2900 | 227 |
| 304 | S365 | 2884 | 110 |
| 305 | S364 | 2868 | 227 |
| 306 | S363 | 2852 | 110 |
| 307 | S362 | 2836 | 227 |
| 308 | S361 | 2820 | 110 |
| 309 | S360 | 2804 | 227 |
| 310 | S359 | 2788 | 110 |
| 311 | S358 | 2772 | 227 |
| 312 | S357 | 2756 | 110 |
| 313 | S356 | 2740 | 227 |
| 314 | S355 | 2724 | 110 |
| 315 | S354 | 2708 | 227 |
| 316 | S353 | 2692 | 110 |
| 317 | S352 | 2676 | 227 |
| 318 | S351 | 2660 | 110 |
| 319 | S350 | 2644 | 227 |
| 320 | S349 | 2628 | 110 |
| 321 | S348 | 2612 | 227 |
| 322 | S347 | 2596 | 110 |
| 323 | S346 | 2580 | 227 |
| 324 | S345 | 2564 | 110 |
| 325 | S344 | 2548 | 227 |
| 326 | S343 | 2532 | 110 |
| 327 | S342 | 2516 | 227 |
| 328 | S341 | 2500 | 110 |
| 329 | S340 | 2484 | 227 |
| 330 | S339 | 2468 | 110 |
| 331 | S338 | 2452 | 227 |
| 332 | S337 | 2436 | 110 |
| 333 | S336 | 2420 | 227 |
| 334 | S335 | 2404 | 110 |
| 335 | S334 | 2388 | 227 |
| 336 | S333 | 2372 | 110 |
| 337 | S332 | 2356 | 227 |
| 338 | S331 | 2340 | 110 |
| 339 | S330 | 2324 | 227 |
| 340 | S329 | 2308 | 110 |
| 341 | S328 | 2292 | 227 |
| 342 | S327 | 2276 | 110 |
| 343 | S326 | 2260 | 227 |
| 344 | S325 | 2244 | 110 |
| 345 | S324 | 2228 | 227 |
| 346 | S323 | 2212 | 110 |
| 347 | S322 | 2196 | 227 |
| 348 | S321 | 2180 | 110 |
| 349 | S320 | 2164 | 227 |
| 350 | S319 | 2148 | 110 |

| No. | PAD Name | X | Y |
|-----|----------|------|-----|
| 351 | S318 | 2132 | 227 |
| 352 | S317 | 2116 | 110 |
| 353 | S316 | 2100 | 227 |
| 354 | S315 | 2084 | 110 |
| 355 | S314 | 2068 | 227 |
| 356 | S313 | 2052 | 110 |
| 357 | S312 | 2036 | 227 |
| 358 | S311 | 2020 | 110 |
| 359 | S310 | 2004 | 227 |
| 360 | S309 | 1988 | 110 |
| 361 | S308 | 1972 | 227 |
| 362 | S307 | 1956 | 110 |
| 363 | S306 | 1940 | 227 |
| 364 | S305 | 1924 | 110 |
| 365 | S304 | 1908 | 227 |
| 366 | S303 | 1892 | 110 |
| 367 | S302 | 1876 | 227 |
| 368 | S301 | 1860 | 110 |
| 369 | S300 | 1844 | 227 |
| 370 | S299 | 1828 | 110 |
| 371 | S298 | 1812 | 227 |
| 372 | S297 | 1796 | 110 |
| 373 | S296 | 1780 | 227 |
| 374 | S295 | 1764 | 110 |
| 375 | S294 | 1748 | 227 |
| 376 | S293 | 1732 | 110 |
| 377 | S292 | 1716 | 227 |
| 378 | S291 | 1700 | 110 |
| 379 | S290 | 1684 | 227 |
| 380 | S289 | 1668 | 110 |
| 381 | S288 | 1652 | 227 |
| 382 | S287 | 1636 | 110 |
| 383 | S286 | 1620 | 227 |
| 384 | S285 | 1604 | 110 |
| 385 | S284 | 1588 | 227 |
| 386 | S283 | 1572 | 110 |
| 387 | S282 | 1556 | 227 |
| 388 | S281 | 1540 | 110 |
| 389 | S280 | 1524 | 227 |
| 390 | S279 | 1508 | 110 |
| 391 | S278 | 1492 | 227 |
| 392 | S277 | 1476 | 110 |
| 393 | S276 | 1460 | 227 |
| 394 | S275 | 1444 | 110 |
| 395 | S274 | 1428 | 227 |
| 396 | S273 | 1412 | 110 |
| 397 | S272 | 1396 | 227 |
| 398 | S271 | 1380 | 110 |
| 399 | S270 | 1364 | 227 |
| 400 | S269 | 1348 | 110 |

| No. | PAD Name | X | Y |
|-----|----------|------|-----|
| 401 | S268 | 1332 | 227 |
| 402 | S267 | 1316 | 110 |
| 403 | S266 | 1300 | 227 |
| 404 | S265 | 1284 | 110 |
| 405 | S264 | 1268 | 227 |
| 406 | S263 | 1252 | 110 |
| 407 | S262 | 1236 | 227 |
| 408 | S261 | 1220 | 110 |
| 409 | S260 | 1204 | 227 |
| 410 | S259 | 1188 | 110 |
| 411 | S258 | 1172 | 227 |
| 412 | S257 | 1156 | 110 |
| 413 | S256 | 1140 | 227 |
| 414 | S255 | 1124 | 110 |
| 415 | S254 | 1108 | 227 |
| 416 | S253 | 1092 | 110 |
| 417 | S252 | 1076 | 227 |
| 418 | S251 | 1060 | 110 |
| 419 | S250 | 1044 | 227 |
| 420 | S249 | 1028 | 110 |
| 421 | S248 | 1012 | 227 |
| 422 | S247 | 996 | 110 |
| 423 | S246 | 980 | 227 |
| 424 | S245 | 964 | 110 |
| 425 | S244 | 948 | 227 |
| 426 | S243 | 932 | 110 |
| 427 | S242 | 916 | 227 |
| 428 | S241 | 900 | 110 |
| 429 | S240 | 884 | 227 |
| 430 | S239 | 868 | 110 |
| 431 | S238 | 852 | 227 |
| 432 | S237 | 836 | 110 |
| 433 | S236 | 820 | 227 |
| 434 | S235 | 804 | 110 |
| 435 | S234 | 788 | 227 |
| 436 | S233 | 772 | 110 |
| 437 | S232 | 756 | 227 |
| 438 | S231 | 740 | 110 |
| 439 | S230 | 724 | 227 |
| 440 | S229 | 708 | 110 |
| 441 | S228 | 692 | 227 |
| 442 | S227 | 676 | 110 |
| 443 | S226 | 660 | 227 |
| 444 | S225 | 644 | 110 |
| 445 | S224 | 628 | 227 |
| 446 | S223 | 612 | 110 |
| 447 | S222 | 596 | 227 |
| 448 | S221 | 580 | 110 |
| 449 | S220 | 564 | 227 |
| 450 | S219 | 548 | 110 |

| No. | PAD Name | X | Y |
|-----|----------|------|-----|
| 451 | S218 | 532 | 227 |
| 452 | S217 | 516 | 110 |
| 453 | S216 | 500 | 227 |
| 454 | S215 | 484 | 110 |
| 455 | S214 | 468 | 227 |
| 456 | S213 | 452 | 110 |
| 457 | S212 | 436 | 227 |
| 458 | S211 | 420 | 110 |
| 459 | S210 | 404 | 227 |
| 460 | S209 | 388 | 110 |
| 461 | S208 | 372 | 227 |
| 462 | S207 | 356 | 110 |
| 463 | S206 | 340 | 227 |
| 464 | S205 | 324 | 110 |
| 465 | S204 | 308 | 227 |
| 466 | S203 | 292 | 110 |
| 467 | S202 | 276 | 227 |
| 468 | S201 | 260 | 110 |
| 469 | S200 | 244 | 227 |
| 470 | S199 | 228 | 110 |
| 471 | DUMMY | 212 | 227 |
| 472 | DUMMY | 196 | 110 |
| 473 | DUMMY | -196 | 110 |
| 474 | DUMMY | -212 | 227 |
| 475 | S198 | -228 | 110 |
| 476 | S197 | -244 | 227 |
| 477 | S196 | -260 | 110 |
| 478 | S195 | -276 | 227 |
| 479 | S194 | -292 | 110 |
| 480 | S193 | -308 | 227 |
| 481 | S192 | -324 | 110 |
| 482 | S191 | -340 | 227 |
| 483 | S190 | -356 | 110 |
| 484 | S189 | -372 | 227 |
| 485 | S188 | -388 | 110 |
| 486 | S187 | -404 | 227 |
| 487 | S186 | -420 | 110 |
| 488 | S185 | -436 | 227 |
| 489 | S184 | -452 | 110 |
| 490 | S183 | -468 | 227 |
| 491 | S182 | -484 | 110 |
| 492 | S181 | -500 | 227 |
| 493 | S180 | -516 | 110 |
| 494 | S179 | -532 | 227 |
| 495 | S178 | -548 | 110 |
| 496 | S177 | -564 | 227 |
| 497 | S176 | -580 | 110 |
| 498 | S175 | -596 | 227 |
| 499 | S174 | -612 | 110 |
| 500 | S173 | -628 | 227 |

| No. | PAD Name | X | Y |
|-----|----------|-------|-----|
| 501 | S172 | -644 | 110 |
| 502 | S171 | -660 | 227 |
| 503 | S170 | -676 | 110 |
| 504 | S169 | -692 | 227 |
| 505 | S168 | -708 | 110 |
| 506 | S167 | -724 | 227 |
| 507 | S166 | -740 | 110 |
| 508 | S165 | -756 | 227 |
| 509 | S164 | -772 | 110 |
| 510 | S163 | -788 | 227 |
| 511 | S162 | -804 | 110 |
| 512 | S161 | -820 | 227 |
| 513 | S160 | -836 | 110 |
| 514 | S159 | -852 | 227 |
| 515 | S158 | -868 | 110 |
| 516 | S157 | -884 | 227 |
| 517 | S156 | -900 | 110 |
| 518 | S155 | -916 | 227 |
| 519 | S154 | -932 | 110 |
| 520 | S153 | -948 | 227 |
| 521 | S152 | -964 | 110 |
| 522 | S151 | -980 | 227 |
| 523 | S150 | -996 | 110 |
| 524 | S149 | -1012 | 227 |
| 525 | S148 | -1028 | 110 |
| 526 | S147 | -1044 | 227 |
| 527 | S146 | -1060 | 110 |
| 528 | S145 | -1076 | 227 |
| 529 | S144 | -1092 | 110 |
| 530 | S143 | -1108 | 227 |
| 531 | S142 | -1124 | 110 |
| 532 | S141 | -1140 | 227 |
| 533 | S140 | -1156 | 110 |
| 534 | S139 | -1172 | 227 |
| 535 | S138 | -1188 | 110 |
| 536 | S137 | -1204 | 227 |
| 537 | S136 | -1220 | 110 |
| 538 | S135 | -1236 | 227 |
| 539 | S134 | -1252 | 110 |
| 540 | S133 | -1268 | 227 |
| 541 | S132 | -1284 | 110 |
| 542 | S131 | -1300 | 227 |
| 543 | S130 | -1316 | 110 |
| 544 | S129 | -1332 | 227 |
| 545 | S128 | -1348 | 110 |
| 546 | S127 | -1364 | 227 |
| 547 | S126 | -1380 | 110 |
| 548 | S125 | -1396 | 227 |
| 549 | S124 | -1412 | 110 |
| 550 | S123 | -1428 | 227 |

| No. | PAD Name | X | Y |
|-----|----------|-------|-----|
| 551 | S122 | -1444 | 110 |
| 552 | S121 | -1460 | 227 |
| 553 | S120 | -1476 | 110 |
| 554 | S119 | -1492 | 227 |
| 555 | S118 | -1508 | 110 |
| 556 | S117 | -1524 | 227 |
| 557 | S116 | -1540 | 110 |
| 558 | S115 | -1556 | 227 |
| 559 | S114 | -1572 | 110 |
| 560 | S113 | -1588 | 227 |
| 561 | S112 | -1604 | 110 |
| 562 | S111 | -1620 | 227 |
| 563 | S110 | -1636 | 110 |
| 564 | S109 | -1652 | 227 |
| 565 | S108 | -1668 | 110 |
| 566 | S107 | -1684 | 227 |
| 567 | S106 | -1700 | 110 |
| 568 | S105 | -1716 | 227 |
| 569 | S104 | -1732 | 110 |
| 570 | S103 | -1748 | 227 |
| 571 | S102 | -1764 | 110 |
| 572 | S101 | -1780 | 227 |
| 573 | S100 | -1796 | 110 |
| 574 | S99 | -1812 | 227 |
| 575 | S98 | -1828 | 110 |
| 576 | S97 | -1844 | 227 |
| 577 | S96 | -1860 | 110 |
| 578 | S95 | -1876 | 227 |
| 579 | S94 | -1892 | 110 |
| 580 | S93 | -1908 | 227 |
| 581 | S92 | -1924 | 110 |
| 582 | S91 | -1940 | 227 |
| 583 | S90 | -1956 | 110 |
| 584 | S89 | -1972 | 227 |
| 585 | S88 | -1988 | 110 |
| 586 | S87 | -2004 | 227 |
| 587 | S86 | -2020 | 110 |
| 588 | S85 | -2036 | 227 |
| 589 | S84 | -2052 | 110 |
| 590 | S83 | -2068 | 227 |
| 591 | S82 | -2084 | 110 |
| 592 | S81 | -2100 | 227 |
| 593 | S80 | -2116 | 110 |
| 594 | S79 | -2132 | 227 |
| 595 | S78 | -2148 | 110 |
| 596 | S77 | -2164 | 227 |
| 597 | S76 | -2180 | 110 |
| 598 | S75 | -2196 | 227 |
| 599 | S74 | -2212 | 110 |
| 600 | S73 | -2228 | 227 |

| No. | PAD Name | X | Y | No. | PAD Name | X | Y | No. | PAD Name | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 601 | S72 | -2244 | 110 | 651 | S22 | -3044 | 110 | 701 | G49 | -3844 | 110 |
| 602 | S71 | -2260 | 227 | 652 | S21 | -3060 | 227 | 702 | G51 | -3860 | 227 |
| 603 | S70 | -2276 | 110 | 653 | S20 | -3076 | 110 | 703 | G53 | -3876 | 110 |
| 604 | S69 | -2292 | 227 | 654 | S19 | -3092 | 227 | 704 | G55 | -3892 | 227 |
| 605 | S68 | -2308 | 110 | 655 | S18 | -3108 | 110 | 705 | G57 | -3908 | 110 |
| 606 | S67 | -2324 | 227 | 656 | S17 | -3124 | 227 | 706 | G59 | -3924 | 227 |
| 607 | S66 | -2340 | 110 | 657 | S16 | -3140 | 110 | 707 | G61 | -3940 | 110 |
| 608 | S65 | -2356 | 227 | 658 | S15 | -3156 | 227 | 708 | G63 | -3956 | 227 |
| 609 | S64 | -2372 | 110 | 659 | S14 | -3172 | 110 | 709 | G65 | -3972 | 110 |
| 610 | S63 | -2388 | 227 | 660 | S13 | -3188 | 227 | 710 | G67 | -3988 | 227 |
| 611 | S62 | -2404 | 110 | 661 | S12 | -3204 | 110 | 711 | G69 | -4004 | 110 |
| 612 | S61 | -2420 | 227 | 662 | S11 | -3220 | 227 | 712 | G71 | -4020 | 227 |
| 613 | S60 | -2436 | 110 | 663 | S10 | -3236 | 110 | 713 | G73 | -4036 | 110 |
| 614 | S59 | -2452 | 227 | 664 | S9 | -3252 | 227 | 714 | G75 | -4052 | 227 |
| 615 | S58 | -2468 | 110 | 665 | S8 | -3268 | 110 | 715 | G77 | -4068 | 110 |
| 616 | S57 | -2484 | 227 | 666 | S7 | -3284 | 227 | 716 | G79 | -4084 | 227 |
| 617 | S56 | -2500 | 110 | 667 | S6 | -3300 | 110 | 717 | G81 | -4100 | 110 |
| 618 | S55 | -2516 | 227 | 668 | S5 | -3316 | 227 | 718 | G83 | -4116 | 227 |
| 619 | S54 | -2532 | 110 | 669 | S4 | -3332 | 110 | 719 | G85 | -4132 | 110 |
| 620 | S53 | -2548 | 227 | 670 | S3 | -3348 | 227 | 720 | G87 | -4148 | 227 |
| 621 | S52 | -2564 | 110 | 671 | S2 | -3364 | 110 | 721 | G89 | -4164 | 110 |
| 622 | S51 | -2580 | 227 | 672 | S1 | -3380 | 227 | 722 | G91 | -4180 | 227 |
| 623 | S50 | -2596 | 110 | 673 | DUMMY | -3396 | 110 | 723 | G93 | -4196 | 110 |
| 624 | S49 | -2612 | 227 | 674 | DUMMY | -3412 | 227 | 724 | G95 | -4212 | 227 |
| 625 | S48 | -2628 | 110 | 675 | DUMMY | -3428 | 110 | 725 | G97 | -4228 | 110 |
| 626 | S47 | -2644 | 227 | 676 | DUMMY | -3444 | 227 | 726 | G99 | -4244 | 227 |
| 627 | S46 | -2660 | 110 | 677 | G1 | -3460 | 110 | 727 | G101 | -4260 | 110 |
| 628 | S45 | -2676 | 227 | 678 | G3 | -3476 | 227 | 728 | G103 | -4276 | 227 |
| 629 | S44 | -2692 | 110 | 679 | G5 | -3492 | 110 | 729 | G105 | -4292 | 110 |
| 630 | S43 | -2708 | 227 | 680 | G7 | -3508 | 227 | 730 | G107 | -4308 | 227 |
| 631 | S42 | -2724 | 110 | 681 | G9 | -3524 | 110 | 731 | G109 | -4324 | 110 |
| 632 | S41 | -2740 | 227 | 682 | G11 | -3540 | 227 | 732 | G111 | -4340 | 227 |
| 633 | S40 | -2756 | 110 | 683 | G13 | -3556 | 110 | 733 | G113 | -4356 | 110 |
| 634 | S39 | -2772 | 227 | 684 | G15 | -3572 | 227 | 734 | G115 | -4372 | 227 |
| 635 | S38 | -2788 | 110 | 685 | G17 | -3588 | 110 | 735 | G117 | -4388 | 110 |
| 636 | S37 | -2804 | 227 | 686 | G19 | -3604 | 227 | 736 | G119 | -4404 | 227 |
| 637 | S36 | -2820 | 110 | 687 | G21 | -3620 | 110 | 737 | G121 | -4420 | 110 |
| 638 | S35 | -2836 | 227 | 688 | G23 | -3636 | 227 | 738 | G123 | -4436 | 227 |
| 639 | S34 | -2852 | 110 | 689 | G25 | -3652 | 110 | 739 | G125 | -4452 | 110 |
| 640 | S33 | -2868 | 227 | 690 | G27 | -3668 | 227 | 740 | G127 | -4468 | 227 |
| 641 | S32 | -2884 | 110 | 691 | G29 | -3684 | 110 | 741 | G129 | -4484 | 110 |
| 642 | S31 | -2900 | 227 | 692 | G31 | -3700 | 227 | 742 | G131 | -4500 | 227 |
| 643 | S30 | -2916 | 110 | 693 | G33 | -3716 | 110 | 743 | G133 | -4516 | 110 |
| 644 | S29 | -2932 | 227 | 694 | G35 | -3732 | 227 | 744 | G135 | -4532 | 227 |
| 645 | S28 | -2948 | 110 | 695 | G37 | -3748 | 110 | 745 | G137 | -4548 | 110 |
| 646 | S27 | -2964 | 227 | 696 | G39 | -3764 | 227 | 746 | G139 | -4564 | 227 |
| 647 | S26 | -2980 | 110 | 697 | G41 | -3780 | 110 | 747 | G141 | -4580 | 110 |
| 648 | S25 | -2996 | 227 | 698 | G43 | -3796 | 227 | 748 | G143 | -4596 | 227 |
| 649 | S24 | -3012 | 110 | 699 | G45 | -3812 | 110 | 749 | G145 | -4612 | 110 |
| 650 | S23 | -3028 | 227 | 700 | G47 | -3828 | 227 | 750 | G147 | -4628 | 227 |

| No. | PAD Name | X | Y |
|-----|----------|-------|------|
| 751 | G149 | -4644 | 110 |
| 752 | G151 | -4660 | 227 |
| 753 | G153 | -4676 | 110 |
| 754 | G155 | -4692 | 227 |
| 755 | G157 | -4708 | 110 |
| 756 | G159 | -4724 | 227 |
| 757 | G161 | -4740 | 110 |
| 758 | DUMMY | -4756 | 227 |
| 759 | DUMMY | -4772 | 110 |
| | | | |
| | ALK-R | 4841 | -220 |
| | ALK-L | -4841 | -220 |

# ST7735

## 5 Block diagram

# ST7735

## 6 Driver IC Pin Description

### 6.1 Power Supply Pin

| Name | I/O | Description | Connect pin |
|------|-----|-------------|-------------|
| VDD | I | Power supply for analog, digital system and booster circuit. | VDD |
| VDDI | I | Power supply for I/O system. | VDDI |
| AGND | I | System ground for analog system and booster circuit. | GND |
| DGND | I | System ground for I/O system and digital system. | GND |

### 6.2 Interface logic pin

| Name | I/O | Description | Connect pin |
|------|-----|-------------|-------------|
| IM2 | I | MCU Parallel interface bus and Serial interface select<br>IM2='1', Parallel interface<br>IM2='0', Serial interface | DGND/VDDI |
| IM1,IM0 | I | - MCU parallel interface type selection<br>-If not used, please fix this pin at VDDI or DGND level.<br><br>| IM1 | IM0 | Parallel interface |<br>|-----|-----|--------------------|<br>| 0 | 0 | MCU 8-bit parallel |<br>| 0 | 1 | MCU 16-bit parallel |<br>| 1 | 0 | MCU 9-bit parallel |<br>| 1 | 1 | MCU 18-bit parallel | | DGND/VDDI |
| SPI4W | I | - SPI4W='0', 3-line SPI enable.<br>- SPI4W='1', 4-line SPI enable.<br>-If not used, please fix this pin at DGND level. | DGND/VDDI |
| RESX | I | -This signal will reset the device and it must be applied to properly initialize the chip.<br>-Signal is active low. | MCU |
| CSX | I | -Chip selection pin<br>-Low enable. | MCU |
| D/CX (SCL) | I | -Display data/command selection pin in MCU interface.<br>-D/CX='1': display data or parameter.<br>-D/CX='0': command data.<br>-In serial interface, this is used as SCL.<br>-If not used, please fix this pin at VDDI or DGND level. | MCU |
| RDX | I | -Read enable in 8080 MCU parallel interface.<br>-If not used, please fix this pin at VDDI or DGND level. | MCU |
| WRX (D/CX) | I | -Write enable in MCU parallel interface.<br>-In 4-line SPI, this pin is used as D/CX (data/ command selection).<br>-If not used, please fix this pin at VDDI or DGND level. | MCU |
| D[17:0] | I/O | -D[17:0] are used as MCU parallel interface data bus. | MCU |

| | | | |
|---|---|---|---|
| | | -D0 is the serial input/output signal in serial interface mode.<br>-In serial interface, D[17:1] are not used and should be fixed at VDDI or DGND level. | |
| TE | O | -Tearing effect output pin to synchronies MCU to frame rate, activated by S/W command.<br>-If not used, please open this pin. | MCU |
| OSC | O | -Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command.<br>-When this pin is inactive (function OFF), this pin is DGND level.<br>-If not used, please open this pin. | - |

*Note1. When in parallel mode, no use data pin must be connected to "1" or "0".*

*Note2. When CSX="1", there is no influence to the parallel and serial interface.*

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## 6.3 Mode selection pin

| Name | I/O | Description | Connect pin |
|------|-----|-------------|-------------|
| EXTC | I | -During normal operation, please open this pin<br><br>| EXTC | Enable/disable modification of extend command |<br>| 0 | System function command list can be used. |<br>| 1 | All command list can be used. | | Open |
| GM2, GM1, GM0 | I | -Panel resolution selection pins.<br><br>| GM2 | GM1 | GM0 | Selection of panel resolution |<br>| 0 | 0 | 0 | 132RGB x 162 (S1~S396 & G1~G162 output) |<br>| 0 | 1 | 1 | 128RGB x 160 (S7~S390 & G2~G161 output) | | VDDI/DGND |
| SRGB | I | -RGB direction select H/W pin for color filter setting.<br><br>| SRGB | RGB arrangement |<br>| 0 | S1, S2, S3 filter order = 'R', 'G', 'B' |<br>| 1 | S1, S2, S3 filter order = 'B', 'G', 'R' | | VDDI/DGND |
| SMX | I | -Module source output direction H/W selection pin.<br><br>| SMX | Scanning direction of source output | |<br>| | GM= '000' | GM= '011' |<br>| 0 | S1 -> S396 | S7 -> S390 |<br>| 1 | S396 -> S1 | S390 -> S7 | | VDDI/DGND |
| SMY | I | -Module Gate output direction H/W selection pin.<br><br>| SMY | Scanning direction of gate output | |<br>| | GM= '000' | GM= '011' |<br>| 0 | G1 -> G162 | G2 -> G161 |<br>| 1 | G162 -> G1 | G161 -> G2 | | VDDI/DGND |
| LCM | I | -Liquid crystal (LC) type selection pins.<br><br>| LCM | Selection of LC type |<br>| 0 | Normally white LC type |<br>| 1 | Normally black LC type | | VDDI/DGND |
| GS | I | -Gamma curve selection pin.<br><br>| GS | Selection of gamma curve |<br>| 0 | GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8 |<br>| 1 | GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0 | | VDDI/DGND |

| TESEL | I | Input pin to select horizontal line number in TE signal.<br><br>This pin is only for GM[2:0]='000' mode<br><br>TESEL='0' , TE output 162 lines<br><br>TESEL='1' , TE output 160 lines | VDDI/DGND |
|---|---|---|---|

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## 6.4 Driver output pins

| Name | I/O | Description | Connect pin |
|---|---|---|---|
| S1 to S396 | O | - Source driver output pins. | - |
| G1 to G162 | O | - Gate driver output pins. | - |
| VCI1 | I/O | - Hi-Z | - |
| AVDD | I | - Power input pin for analog circuits.<br>- In normal usage, connect it to AVDDO.<br>- AVDD = 5.3V. | AVDDO |
| AVDDO | O | - Output of step-up circuit 1<br>- Connect a capacitor for stabilization. | Capacitor |
| VCL | O | - A power supply pin for generating VCOML.<br>- Connect a capacitor for stabilization. | Capacitor |
| VGH | I | - Power input pin for gate driver circuit.<br>- In normal usage, connect it to VGHO. | VGHO |
| VGHO | O | - Positive output pin of the step-up circuit 2.<br>- Connect a capacitor for stabilization. | Capacitor |
| VGL | I | - Power input pin for gate driver circuit.<br>- Negative output of the step-up circuit 2 is connected inside the driver.<br>- Connect a capacitor for stabilization. | Capacitor |
| VREF | O | - A reference voltage for power system.<br>-This test pin for Driver vender test used. | - |
| GVDD | O | - A power output of grayscale voltage generator.<br>- When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin. | - |
| VCOMH | O | - Positive voltage output of VCOM.<br>- Connect a capacitor for stabilization. | Capacitor |
| VCOML | O | - Negative voltage output of VCOM.<br>- Connect a capacitor for stabilization. | Capacitor |
| VCOM | O | - A power supply for the TFT-LCD common electrode. | Common electrode |
| C11P, C11N | O | - Capacitor connecting pins for step-up circuit 1 (for AVDDO) | Step-up Capacitor |
| C22P, C22N C23P, C23N C41P, C41N | O | - Capacitor connecting pins for step-up circuit 2 and 4 (for VGHO, VGL, VCL) | Step-up Capacitor |

| VDDIO | O | -VDDI voltage output level for monitoring. | - |
|---|---|---|---|
| DGNDO | O | -DGND voltage output level for monitoring. | - |
| VCC | I | -Power input pin for internal digital reference voltage.<br>-In normal usage, connect it to VCCO. | VCCO |
| VCCO | O | -Monitoring pin of internal digital reference voltage.<br>-Connect a capacitor for stabilization. | Capacitor |

### 6.5 Test pins

| Name | I/O | Description | Connect pin |
|---|---|---|---|
| TPI[2]<br>TPI[1] | I | -These test pins for Driver vender test used.<br>-Please connect these pins to DGND. | DGND |
| TPO[8]<br>TPO[7]<br>TPO[6]<br>TPO[5]<br>TPO[4]<br>TPO[3]<br>TPO[2]<br>TPO[1] | O | -These test pins for Driver vender test used.<br>-Please open these pins. | Open |
| Dummy | - | -These pins are dummy (have no function inside).<br>-Can allow signal traces pass through these pads on TFT glass.<br>-Please open these pins. | Open |

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## 7 Driver electrical characteristics

### 7.1 Absolute operation range

| Item | Symbol | Rating | Unit |
|------|--------|--------|------|
| Supply voltage | VDD | -0.3 ~ +4.6 | V |
| Supply voltage (Logic) | VDDI | -0.3 ~ +4.6 | V |
| Supply voltage (Digital) | VCC | -0.3 ~ +1.95 | V |
| Driver supply voltage | VGH-VGL | -0.3 ~ +30.0 | V |
| Logic input voltage range | VIN | 0.3 ~ VDDI +0.3 | V |
| Logic output voltage range | VO | 0.3 ~ VDDI +0.3 | V |
| Operating temperature range | TOPR | -30 ~ +85 | ℃ |
| Storage temperature range | TSTG | -40 ~ +125 | ℃ |

*Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute*

*maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the*

*product within the recommend range.*

### 7.2 DC characteristic

| Parameter | Symbol | Condition | Specification | | | Unit | Related Pins |
|-----------|--------|-----------|-----|-----|-----|------|------|
| | | | Min | Typ | Max | | |
| Power & operation voltage | | | | | | | |
| System voltage | VDD | Operating voltage | 2.6 | 2.75 | 3.3 | V | |
| Interface operation voltage | VDDI | I/O supply voltage | 1.65 | 1.9 | 3.3 | V | |
| Gate driver high voltage | VGH | | 10 | | 15 | V | |
| Gate driver low voltage | VGL | | -12.4 | | -7.5 | V | |
| Gate driver supply voltage | | \| VGH-VGL \| | 17.5 | | 27.5 | V | |
| Input / Output | | | | | | | |
| Logic-high input voltage | VIH | | 0.7VDDI | | VDDI | V | Note 1 |
| Logic-low input voltage | VIL | | VSS | | 0.3VDDI | V | Note 1 |
| Logic-high output voltage | VOH | IOH = -1.0mA | 0.8VDDI | | VDDI | V | Note 1 |
| Logic-low output voltage | VOL | IOL = +1.0mA | VSS | | 0.2VDDI | V | Note 1 |
| Logic-high input current | IIH | VIN = VDDI | | | 1 | uA | Note 1 |

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| Logic-low input current | IIL | VIN = VSS | -1 | | | uA | Note 1 |
|---|---|---|---|---|---|---|---|
| Input leakage current | IIL | IOH = -1.0mA | -0.1 | | +0.1 | uA | Note 1 |
| VCOM voltage | | | | | | | |
| VCOM high voltage | VCOMH | Ccom=12nF | 2.5 | | 5.0 | V | |
| VCOM low voltage | VCOML | Ccom=12nF | -2.4 | | 0.0 | V | |
| VCOM amplitude | VCOMAC | \|VCOMH-VCOML\| | 4.0 | | 6.0 | V | |
| Source driver | | | | | | | |
| Source output range | Vsout | | 0.1 | | AVDD-0.1 | V | |
| Gamma reference voltage | GVDD | | 3.0 | | 5.0 | V | |
| Source output settling time | Tr | Below with 99% precision | | | 20 | us | Note 2 |
| Output offset voltage | Voffset | | | | 35 | mV | Note 3 |

*Notes:*

*1. VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, TA= -30 to 85℃*

*2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.*

*3. The Max. value is between measured point of source output and gamma setting value.*

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## 7.3 Power consumption

VDD=2.8V, VDDI=1.8V, Ta=25℃, Frame rate = 60Hz, the registers setting are IC default setting.

| Operation mode | Inversion mode | Image | Current consumption | | | |
| --- | --- | --- | --- | --- | --- | --- |
| | | | Typical | | Maximum | |
| | | | IDDI (mA) | IDD (mA) | IDDI (mA) | IDD (mA) |
| Normal mode | One Line | Note 1 | 0.01 | 0.5 | 0.02 | 0.7 |
| | | Note 2 | 0.01 | 0.5 | 0.02 | 0.7 |
| Partial + Idle mode (40 lines) | One Line | Note 1 | 0.01 | 0.3 | 0.02 | 0.5 |
| | | Note 2 | 0.01 | 0.3 | 0.02 | 0.5 |
| Sleep-in mode | N/A | N/A | 0.005 | 0.015 | 0.01 | 0.03 |

*Notes:*

*1. All pixels black.*

*2. All pixels white.*

*3. The Current Consumption is DC characteristics of ST7735*

# *ST7735*

## 8 Timing chart

### 8.1 Parallel interface characteristics: 18, 16, 9 or 8-bit bus (8080 series MCU interface)
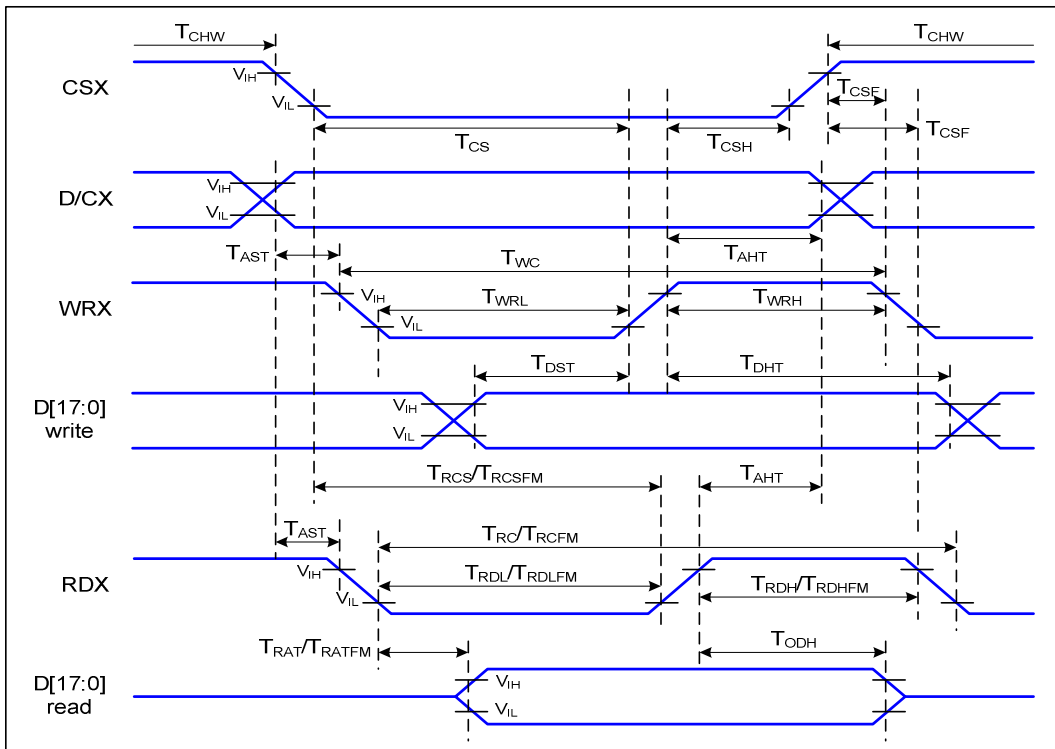


Fig. 8.1.1 Parallel interface timing characteristics (8080 series MCU interface)

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------|--------|-----------|-----|-----|------|-------------|
| D/CX | TAST | Address setup time | 10 | | ns | - |
| | TAHT | Address hold time (Write/Read) | 10 | | ns | |
| CSX | TCHW | Chip select "H" pulse width | 0 | | ns | - |
| | TCS | Chip select setup time (Write) | 15 | | ns | |
| | TRCS | Chip select setup time (Read ID) | 45 | | ns | |
| | TRCSFM | Chip select setup time (Read FM) | 350 | | ns | |
| | TCSF | Chip select wait time (Write/Read) | 10 | | ns | |
| | TCSH | Chip select hold time | 10 | | ns | |
| WRX | TWC | Write cycle | 100 | | ns | |
| | TWRH | Control pulse "H" duration | 30 | | ns | |
| | TWRL | Control pulse "L" duration | 30 | | ns | |
| RDX (ID) | TRC | Read cycle (ID) | 160 | | ns | When read ID data |
| | TRDH | Control pulse "H" duration (ID) | 90 | | ns | |
| | TRDL | Control pulse "L" duration (ID) | 45 | | ns | |
| RDX (FM) | TRCFM | Read cycle (FM) | 450 | | ns | When read from frame memory |
| | TRDHFM | Control pulse "H" duration (FM) | 150 | | ns | |
| | TRDLFM | Control pulse "L" duration (FM) | 150 | | ns | |

| D[17:0] | TDST | Data setup time | 10 | | ns | For CL=30pF |
|---|---|---|---|---|---|---|
| | TDHT | Data hold time | 10 | | ns | |
| | TRAT | Read access time (ID) | | 40 | ns | |
| | TRATFM | Read access time (FM) | | 40 | ns | |
| | TODH | Output disable time | | 80 | ns | |

Table 8.1.1 Parallel Interface Characteristics

*Note: VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 ℃*
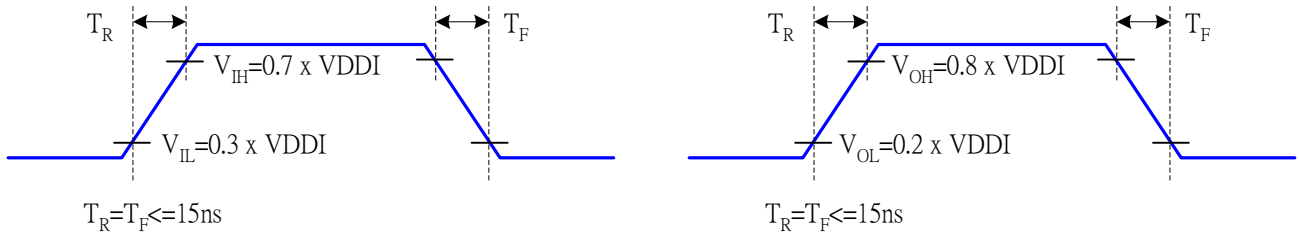


Fig. 8.1.2 Rising and falling timing for input and output signal
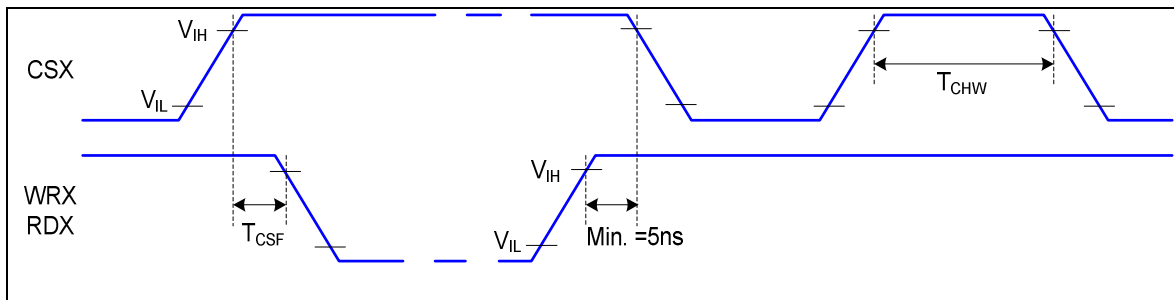


Fig. 8.1.3 Chip selection (CSX) timing
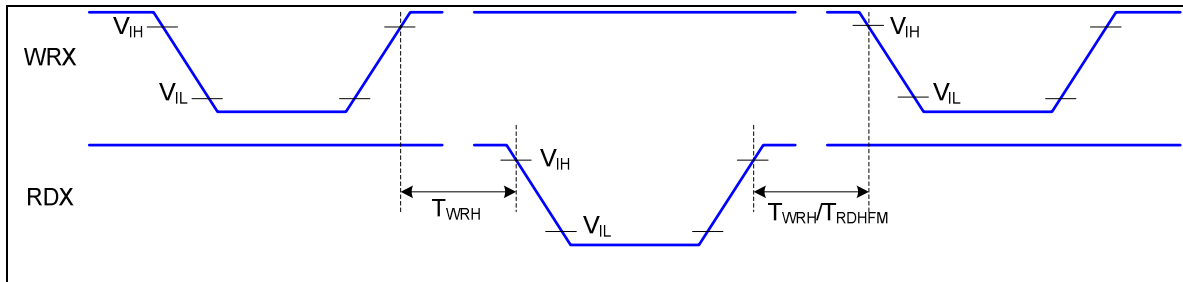


Fig. 8.1.4 Write-to-read and read-to-write timing

*Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30%*

*and 70% of VDDI for Input signals.*

## 8.2 Serial interface characteristics (3-line serial)



Fig. 8.2.1 3-line serial interface timing

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------|--------|-----------|-----|-----|------|-------------|
| CSX | TCSS | Chip select setup time (write) | 15 | | ns | |
| | TCSH | Chip select hold time (write) | 15 | | ns | |
| | TCSS | Chip select setup time (read) | 60 | | ns | |
| | TSCC | Chip select hold time (read) | 65 | | ns | |
| | TCHW | Chip select "H" pulse width | 40 | | ns | |
| SCL | TSCYCW | Serial clock cycle (Write) | 66 | | ns | |
| | TSHW | SCL "H" pulse width (Write) | 30 | | ns | |
| | TSLW | SCL "L" pulse width (Write) | 30 | | ns | |
| | TSCYCR | Serial clock cycle (Read) | 150 | | ns | |
| | TSHR | SCL "H" pulse width (Read) | 60 | | ns | |
| | TSLR | SCL "L" pulse width (Read) | 60 | | ns | |
| SDA (DIN) (DOUT) | TSDS | Data setup time | 10 | | ns | For maximum CL=30pF For minimum CL=8pF |
| | TSDH | Data hold time | 10 | | ns | |
| | TACC | Access time | 10 | 50 | ns | |
| | TOH | Output disable time | | 50 | ns | |

Table 8.2.1 3-line Serial Interface Characteristics

*Note 1: VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 ℃*

*Note 2: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30%*

*and 70% of VDDI for Input signals.*

### 8.3 Serial interface characteristics (4-line serial)



Fig. 8.3.1 4-line serial interface timing

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | TCSS | Chip select setup time (write) | 15 | | ns | |
| | TCSH | Chip select hold time (write) | 15 | | ns | |
| | TCSS | Chip select setup time (read) | 60 | | ns | |
| | TSCC | Chip select hold time (read) | 65 | | ns | |
| | TCHW | Chip select "H" pulse width | 40 | | ns | |
| SCL | TSCYCW | Serial clock cycle (Write) | 66 | | ns | -write command & data ram |
| | TSHW | SCL "H" pulse width (Write) | 30 | | ns | |
| | TSLW | SCL "L" pulse width (Write) | 30 | | ns | |
| | TSCYCR | Serial clock cycle (Read) | 150 | | ns | -read command & data ram |
| | TSHR | SCL "H" pulse width (Read) | 60 | | ns | |
| | TSLR | SCL "L" pulse width (Read) | 60 | | ns | |
| D/CX | TDCS | D/CX setup time | | 0 | ns | |
| | TDCH | D/CX hold time | 10 | | ns | |
| SDA (DIN) (DOUT) | TSDS | Data setup time | 10 | | ns | For maximum CL=30pF For minimum CL=8pF |
| | TSDH | Data hold time | 10 | | ns | |
| | TACC | Access time | 10 | 50 | ns | |
| | TOH | Output disable time | | 50 | ns | |

Table 8.3.1 4-line Serial Interface Characteristics

*Note 1: VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 ℃*

*Note 2: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30%*

*and 70% of VDDI for Input signals.*

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## 9 Function description

### 9.1 Interface type selection

The selection of given interfaces are done by setting IM2, IM1, and IM0 pins as shown in following table.

| IM2 | IM1 | IM0 | Interface | Read back selection |
|-----|-----|-----|-----------|---------------------|
| 0 | - | - | 3-line serial interface | Via the read instruction |
| 1 | 0 | 0 | 8080 MCU 8-bit parallel | RDX strobe (8-bit read data and 8-bit read parameter) |
| 1 | 0 | 1 | 8080 MCU 16-bit parallel | RDX strobe (16-bit read data and 8-bit read parameter) |
| 1 | 1 | 0 | 8080 MCU 9-bit parallel | RDX strobe (9-bit read data and 8-bit read parameter) |
| 1 | 1 | 1 | 8080 MCU 18-bit parallel | RDX strobe (18-bit read data and 8-bit read parameter) |

Table 9.1.1 Selection of MCU interface

| IM2 | IM1 | IM0 | Interface | RDX | WRX | D/CX | Read back selection |
|-----|-----|-----|-----------|-----|-----|------|---------------------|
| 0 | - | - | 3-line serial | Note1 | Note1 | SCL | D[17:1]: unused, D0: SDA |
| 1 | 0 | 0 | 8080 8-bit parallel | RDX | WRX | D/CX | D[17:8]: unused, D7-D0: 8-bit data |
| 1 | 0 | 1 | 8080 16-bit parallel | RDX | WRX | D/CX | D[17:16]: unused, D15-D0: 16-bit data |
| 1 | 1 | 0 | 8080 9-bit parallel | RDX | WRX | D/CX | D[17:9]: unused, D8-D0: 9-bit data |
| 1 | 1 | 1 | 8080 18-bit parallel | RDX | WRX | D/CX | D17-D0: 18-bit data |

Table 9.1.2 Pin connection according to various MCU interface

*Note1: Unused pins can be open, or connected to DGND or VDDI.*

### 9.2 8080-series MCU parallel interface

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command. The interface functions of 8080-series parallel interface are given in following table.

| IM2 | IM1 | IM0 | Interface | D/CX | RDX | WRX | Read back selection |
|-----|-----|-----|-----------|------|-----|-----|---------------------|
| 1 | 0 | 0 | 8-bit parallel | 0 | 1 | ↑ | Write 8-bit command (D7 to D0) |
| | | | | 1 | 1 | ↑ | Write 8-bit display data or 8-bit parameter (D7 to D0) |
| | | | | 1 | ↑ | 1 | Read 8-bit display data (D7 to D0) |
| | | | | 1 | ↑ | 1 | Read 8-bit parameter or status (D7 to D0) |
| 1 | 0 | 1 | 16-bit parallel | 0 | 1 | ↑ | Write 8-bit command (D7 to D0) |
| | | | | 1 | 1 | ↑ | Write 16-bit display data or 8-bit parameter (D15 to D0) |
| | | | | 1 | ↑ | 1 | Read 16-bit display data (D15 to D0) |
| | | | | 1 | ↑ | 1 | Read 8-bit parameter or status (D7 to D0) |
| 1 | 1 | 0 | 9-bit parallel | 0 | 1 | ↑ | Write 8-bit command (D7 to D0) |
| | | | | 1 | 1 | ↑ | Write 9-bit display data or 8-bit parameter (D8 to D0) |
| | | | | 1 | ↑ | 1 | Read 9-bit display data (D8 to D0) |
| | | | | 1 | ↑ | 1 | Read 8-bit parameter or status (D7 to D0) |
| 1 | 1 | 1 | 18-bit parallel | 0 | 1 | ↑ | Write 8-bit command (D7 to D0) |
| | | | | 1 | 1 | ↑ | Write 18-bit display data or 8-bit parameter (D17 to D0) |
| | | | | 1 | ↑ | 1 | Read 18-bit display data (D17 to D0) |
| | | | | 1 | ↑ | 1 | Read 8-bit parameter or status (D7 to D0) |

Table 9.2.1 The function of 8080-series parallel interface

*Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh*

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## 9.2.1    Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').



The host starts to control D[17:0] lines when there is a falling edge of the WRX.

The display writes D[17:0] lines when there is a rising edge of WRX.

The host stops to control D[17:0] lines.
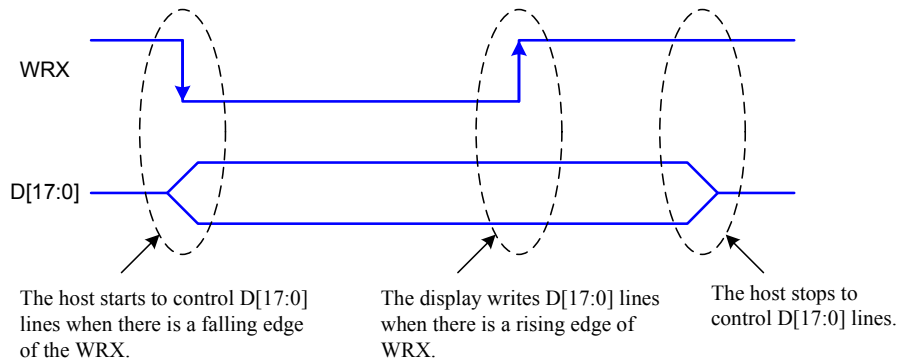
Fig. 9.2.1 8080-series WRX protocol

*Note: WRX is an unsynchronized signal (It can be stopped).*



CMD: write command code
PA: parameter or display data

Signals on D[17:0], D/CX, R/WX, E pins during CSX=1 are ignored.
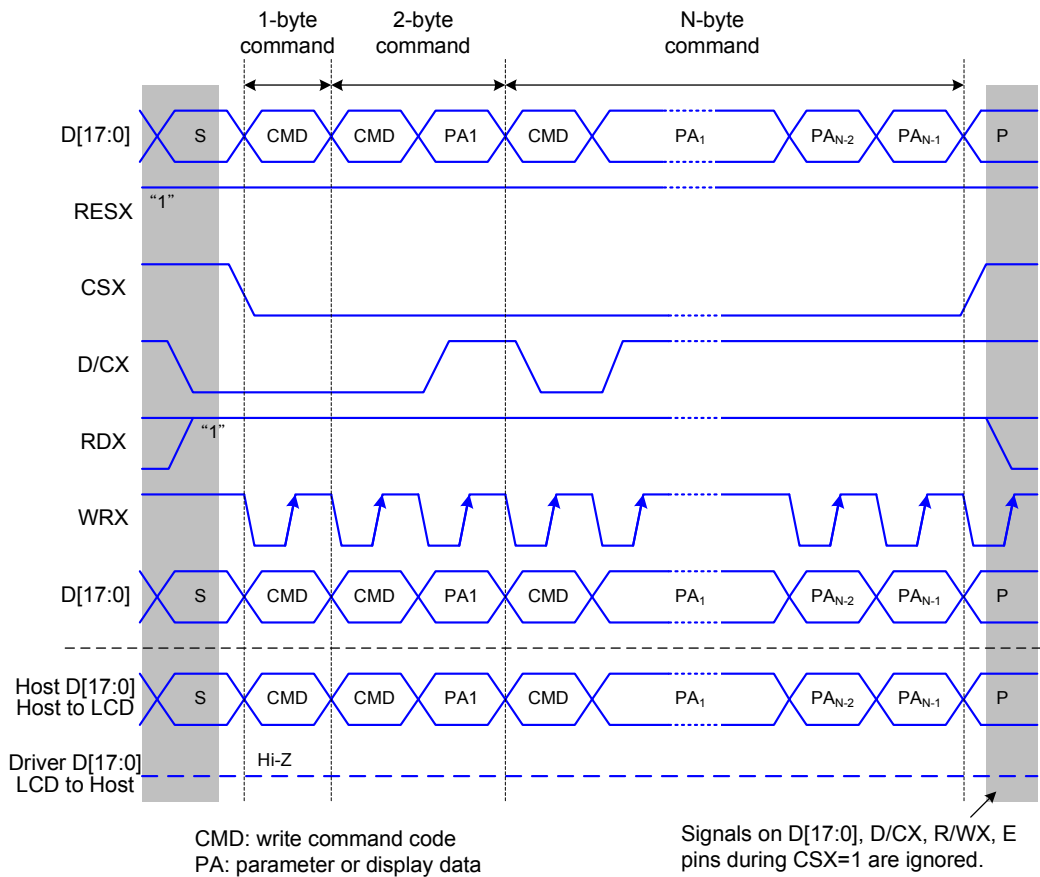
Fig. 9.2.2 8080-series parallel bus protocol, write to register or display RAM

### 9.2.2    Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



The driver starts to control D[17:0] lines when there is a falling edge of the RDX.

The host read D[17:0] lines when there is a rising edge of RDX.

The driver stops to control D[17:0] lines.
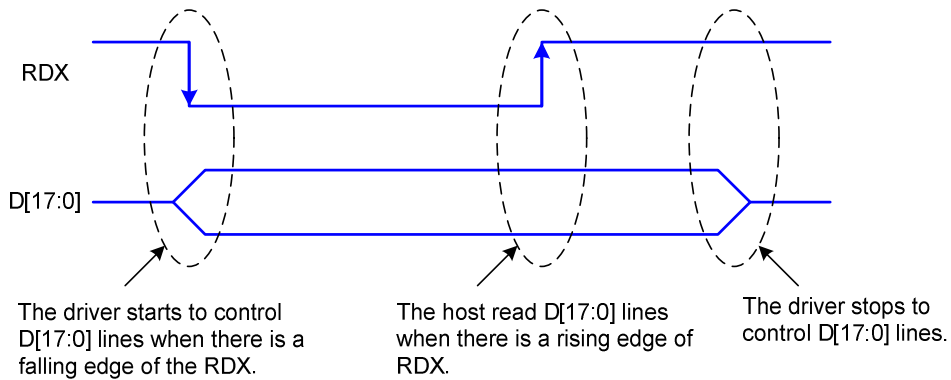
Fig. 9.2.3 8080-series RDX protocol

*Note: RDX is an unsynchronized signal (It can be stopped).*



CMD: write command code
PA: parameter or display data

Signals on D[17:0], D/CX, R/WX, E pins during CSX=1 are ignored.
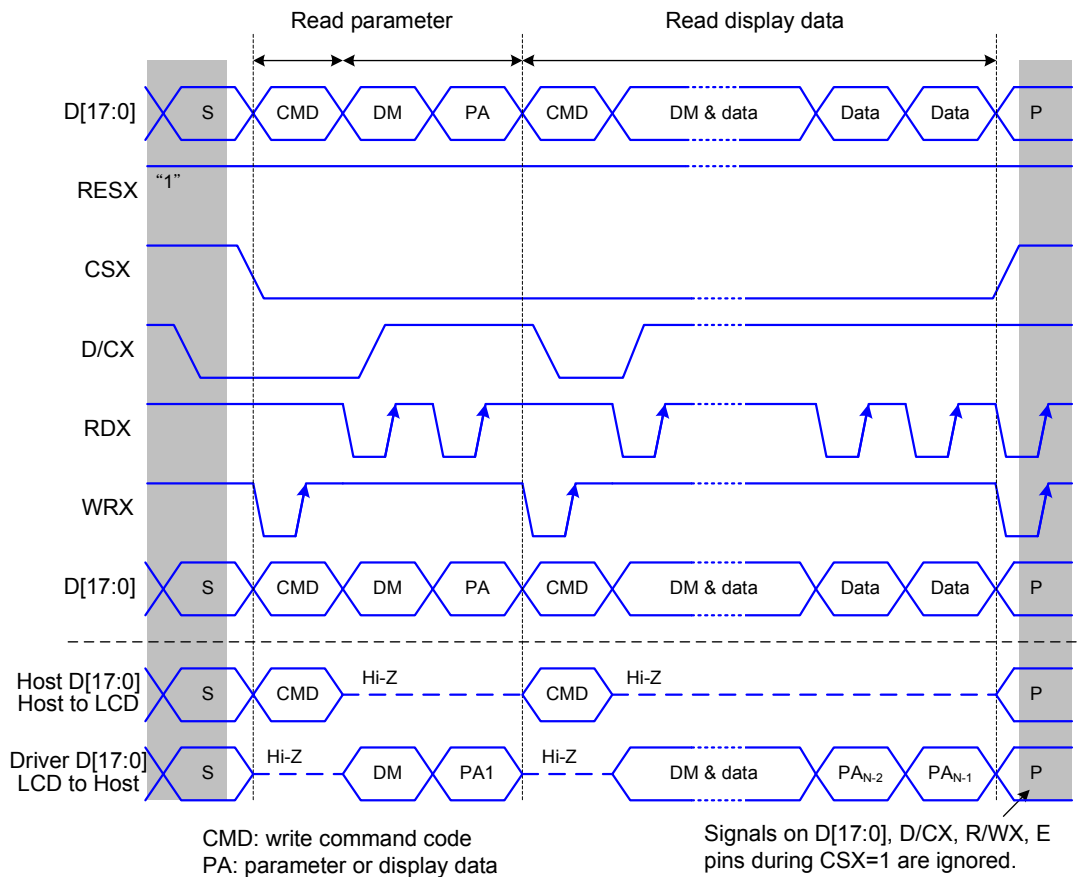
Fig. 9.2.4 8080-series parallel bus protocol, read data from register or display RAM

### 9.3 Serial interface

The selection of this interface is done by IM2. See the Table 9.3.1.

| IM2 | SPI4W | Interface | Read back selection |
|---|---|---|---|
| 0 | 0 | 3-line serial interface | Via the read instruction (8-bit, 24-bit and 32-bit read parameter) |
| 0 | 1 | 4-line serial interface | Via the read instruction (8-bit, 24-bit and 32-bit read parameter) |

Table 9.3.1 Selection of serial interface

The serial interface is either 3-line/9-bit or 4-line/8-bit bi-directional interface for communication between the micro controller and the LCD driver. The 3-line serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-line serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

### 9.3.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-line serial data packet contains a control bit D/CX and a transmission byte. In 4-line serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is "low", the transmission byte is interpreted as a command byte. If D/CX is "high", the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.
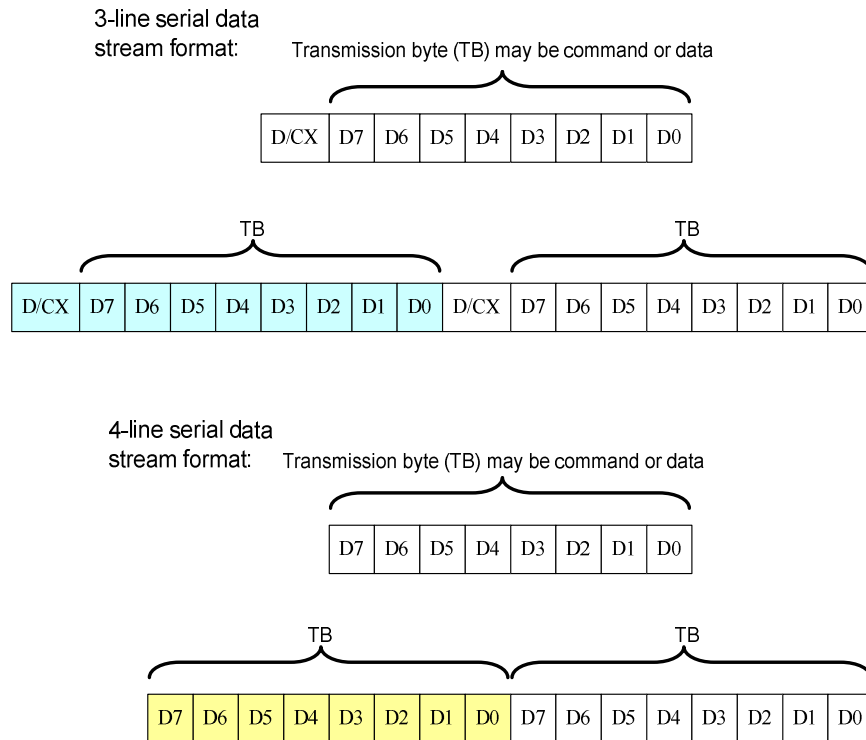


Fig. 9.3.1 Serial interface data stream format

When CSX is "high", SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Fig 9.3.2). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX='0') or parameter/RAM data (D/CX='1'). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

CSX can be "H" between parameter/command and parameter/command SCL, and SDA during CSX="H" is ignored.
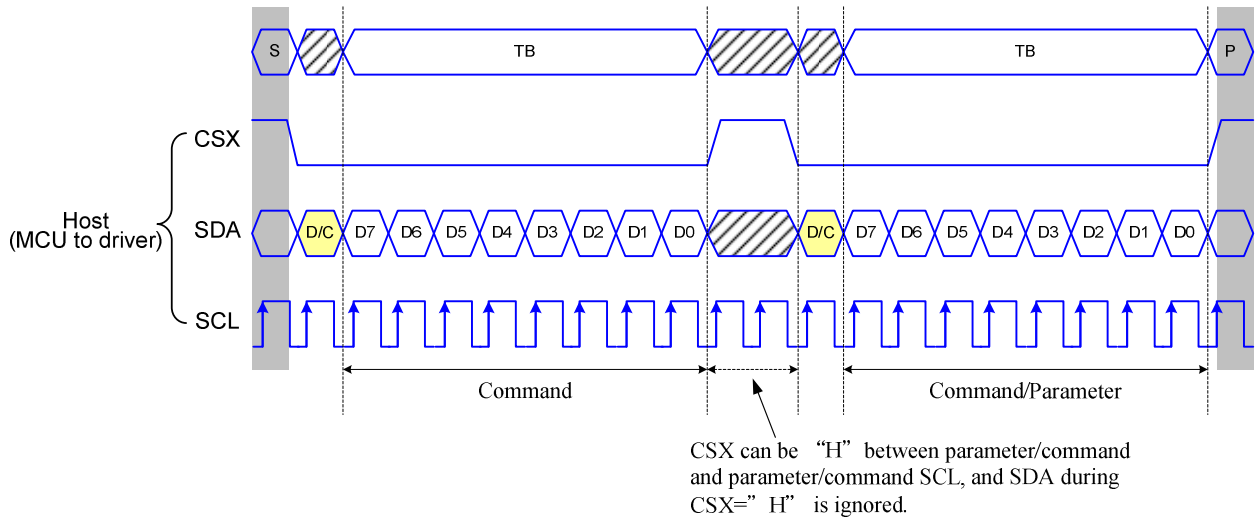
Fig. 9.3.2 3-line serial interface write protocol (write to register with control bit in transmission)



CSX can be "H" between parameter/command and parameter/command SCL, and SDA during CSX="H" is ignored.
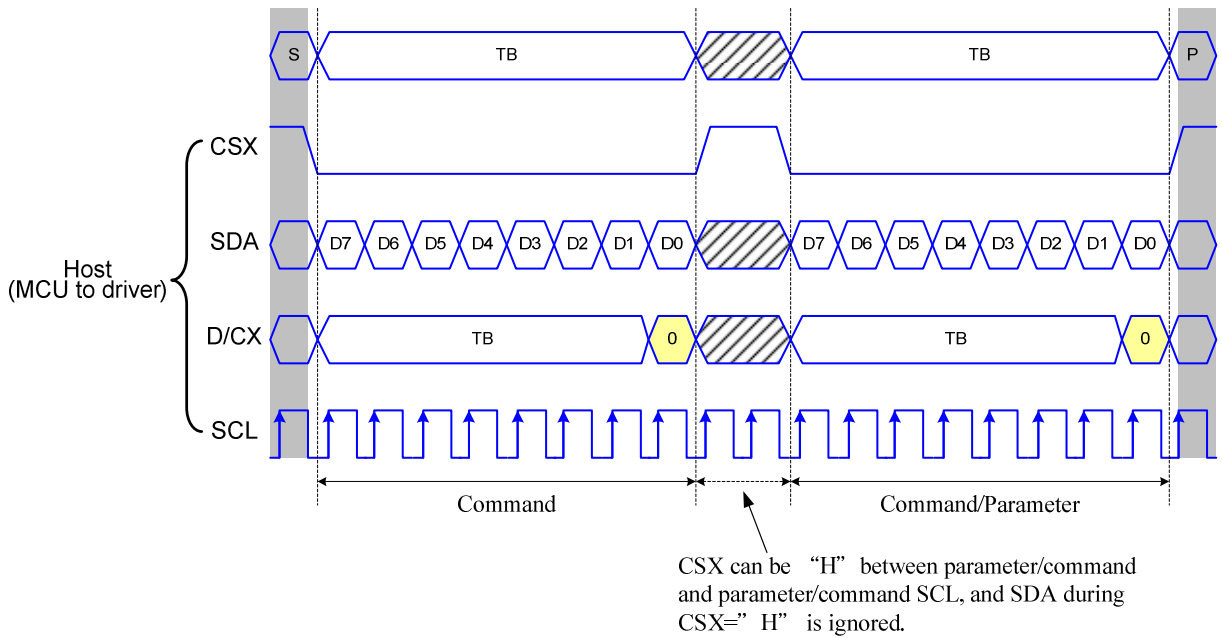
Fig. 9.3.3 4-line serial interface write protocol (write to register with control bit in transmission)

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### 9.3.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

### 9.3.3 3-line serial protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):
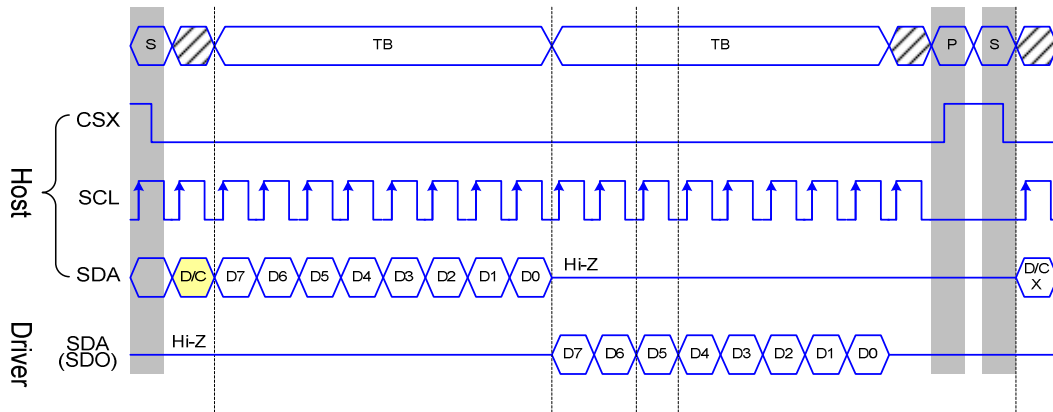
3-line serial protocol (for RDDID command: 24-bit read)
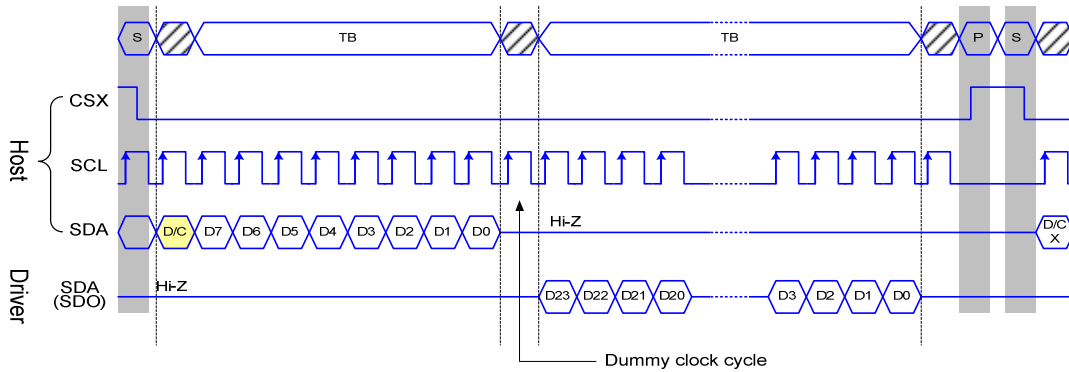
3-line Serial Protocol (for RDDST command: 32-bit read)
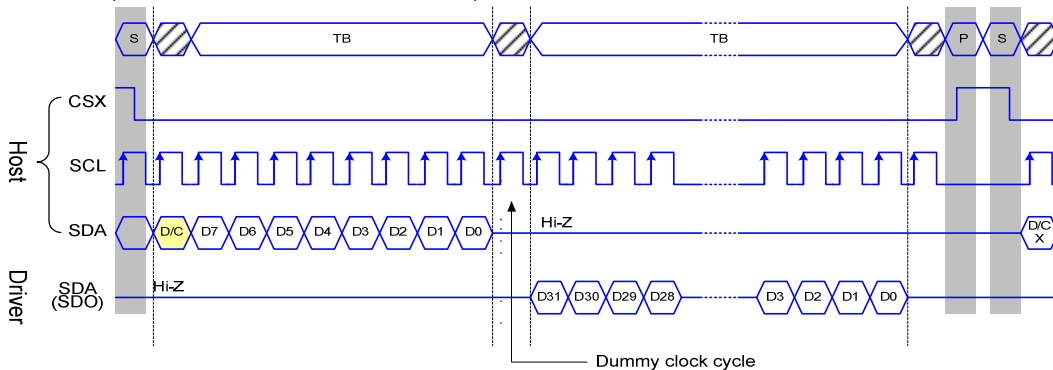


Fig. 9.3.4 3-line serial interface read protocol

### 9.3.4    4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):
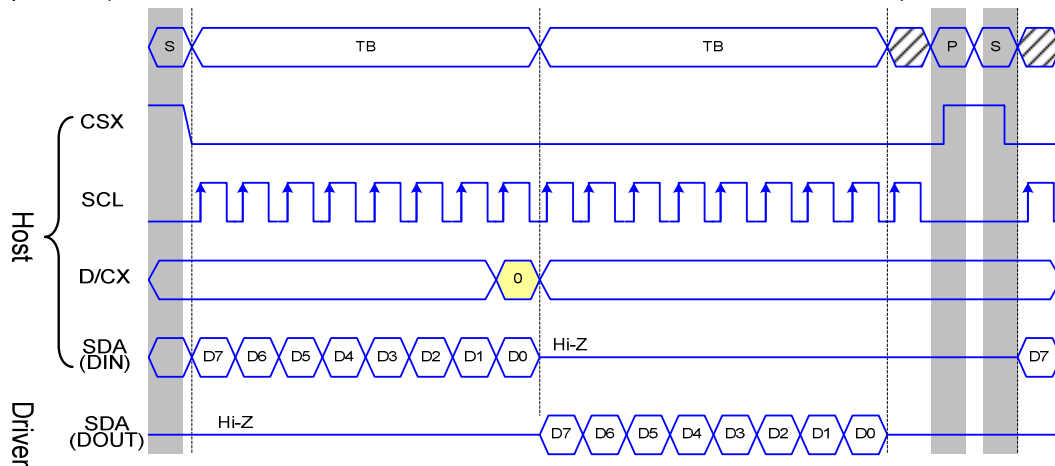


4-line serial protocol (for RDDID command: 24-bit read)
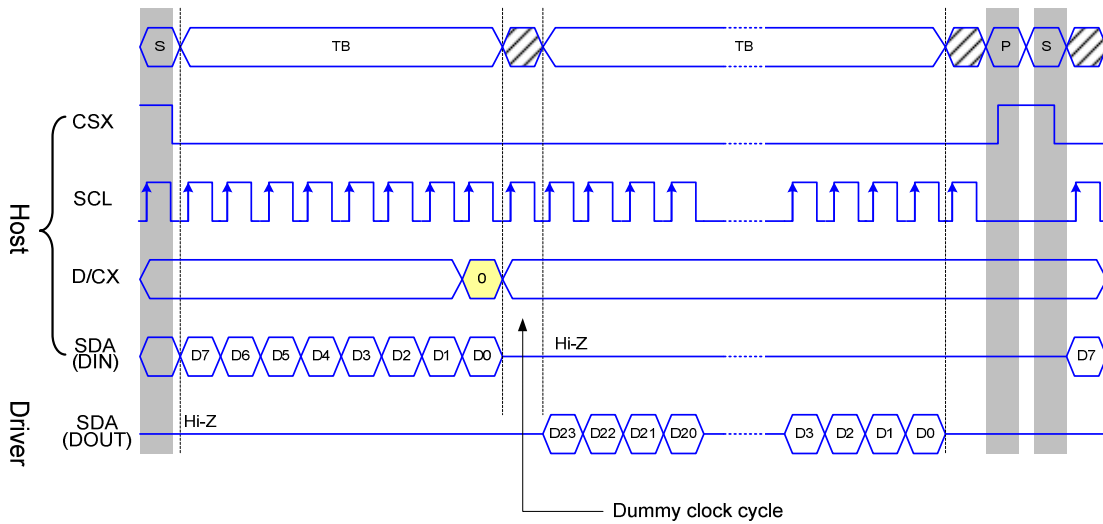


4-line Serial Protocol (for RDDST command: 32-bit read)
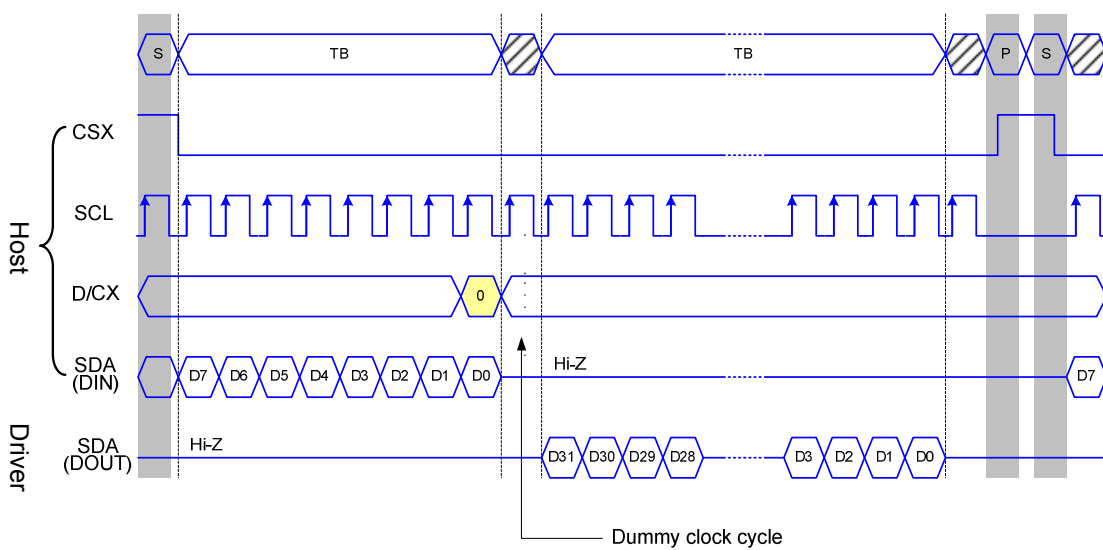


Fig. 9.3.5 4-line serial interface read protocol

### 9.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example
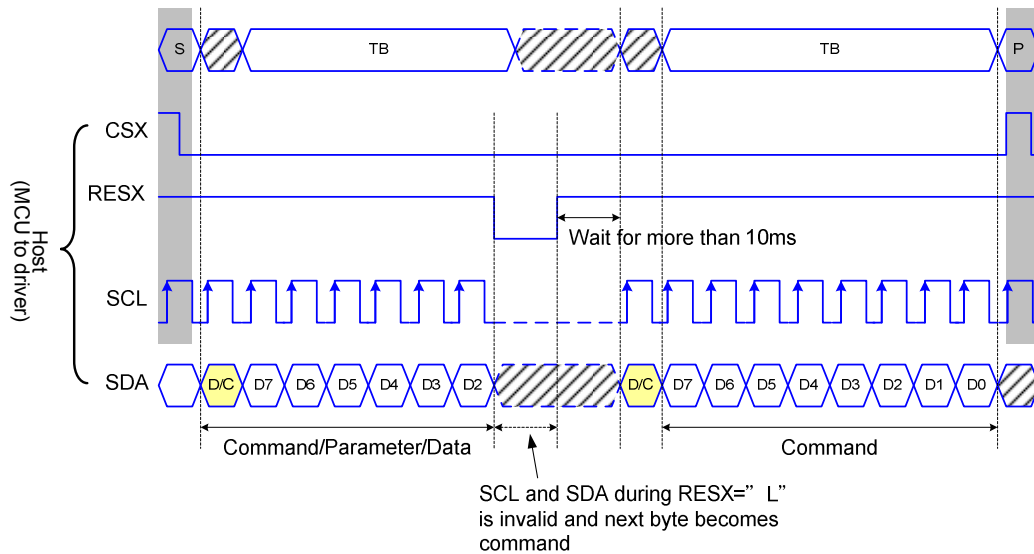


Fig. 9.4.1 Serial bus protocol, write mode － interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example
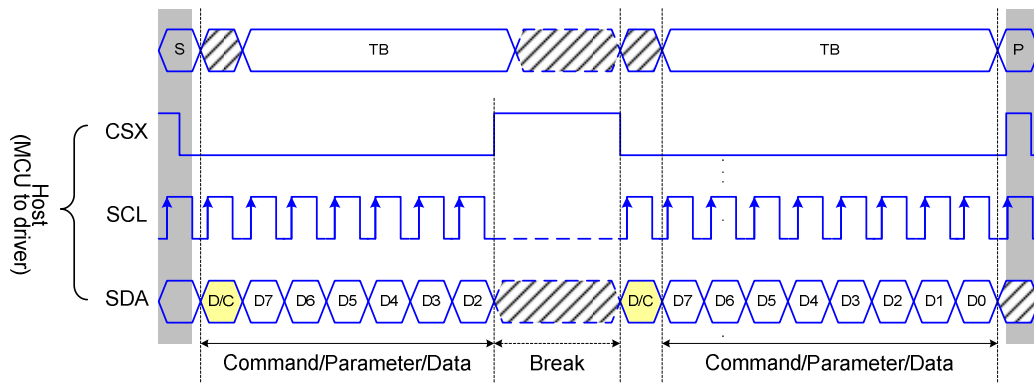


Fig. 9.4.2 Serial bus protocol, write mode － interrupted by CSX

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.
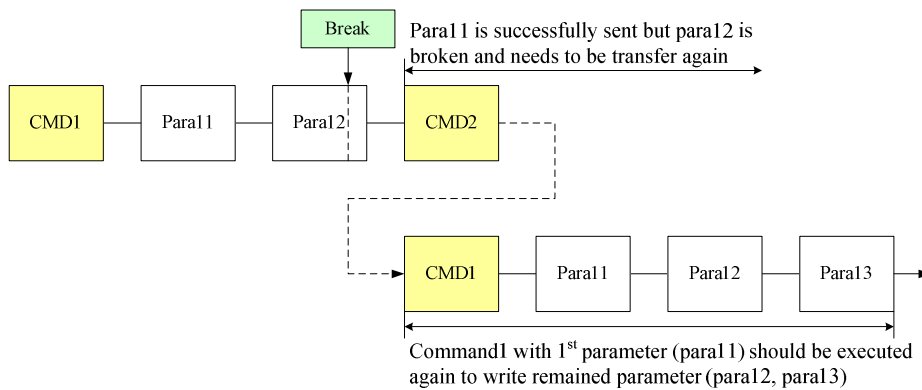
Fig. 9.4.3 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.
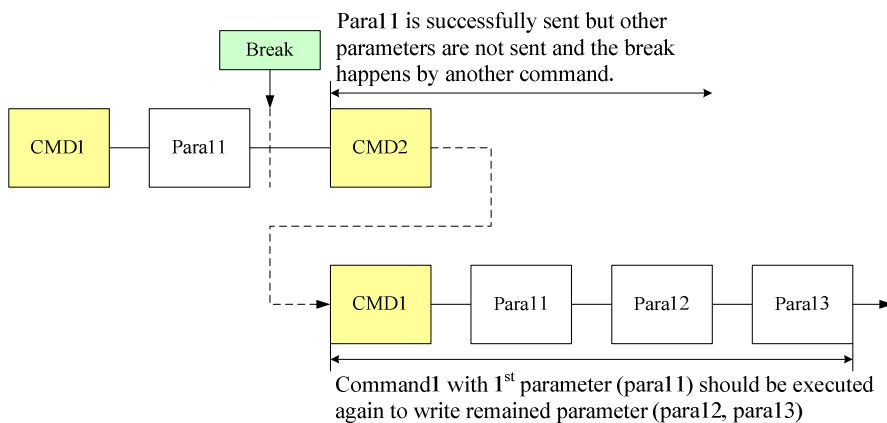


Fig. 9.4.4 Write interrupts recovery (both serial and parallel Interface)

### 9.5 Data transfer pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

#### 9.5.1 Serial interface pause
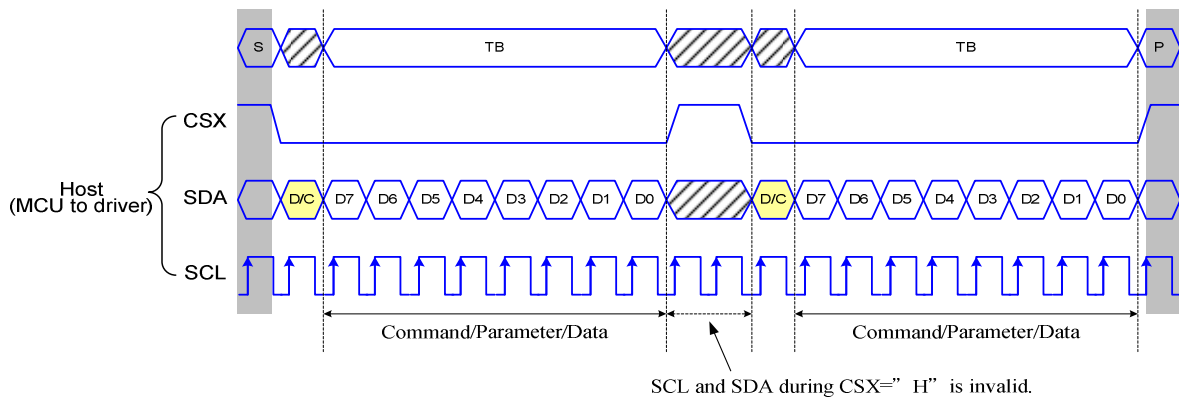


Fig. 9.5.1 Serial interface pause protocol (pause by CSX)

#### 9.5.2 Parallel interface pause
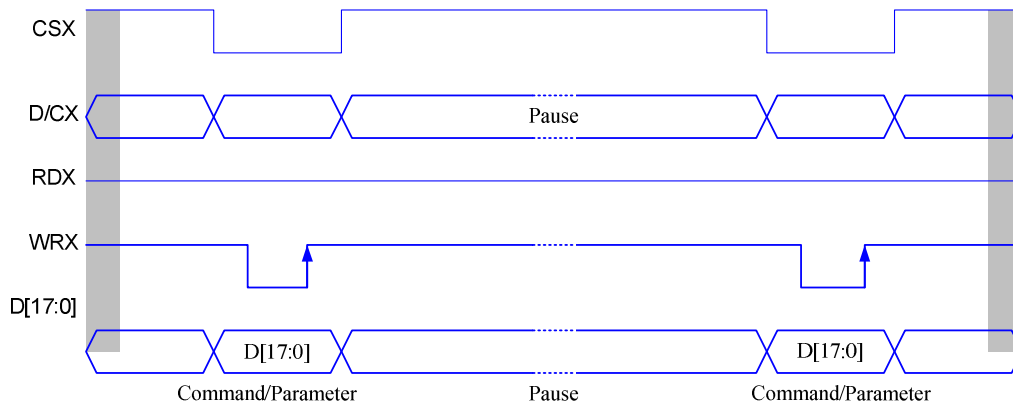


Fig. 9.5.2 Parallel bus pause protocol (paused by CSX)

## 9.6 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

### 9.6.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.

**Start**                                            **Stop**

| Start frame Memory write | Frame 1 Image data | Frame 2 Image data | Frame 3 Image data | ------- | Any command |
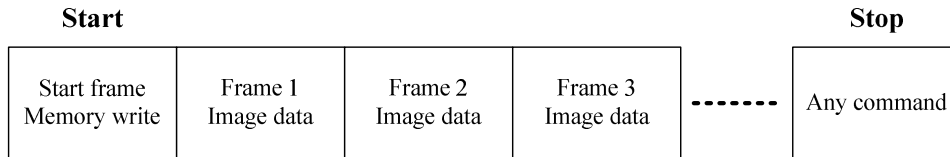
### 9.6.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.

**Start**

| Start frame Memory write | Frame 1 Image data | Any command | Start frame Memory write | Frame 2 Image data | Any command |

**Stop**

| Any command |
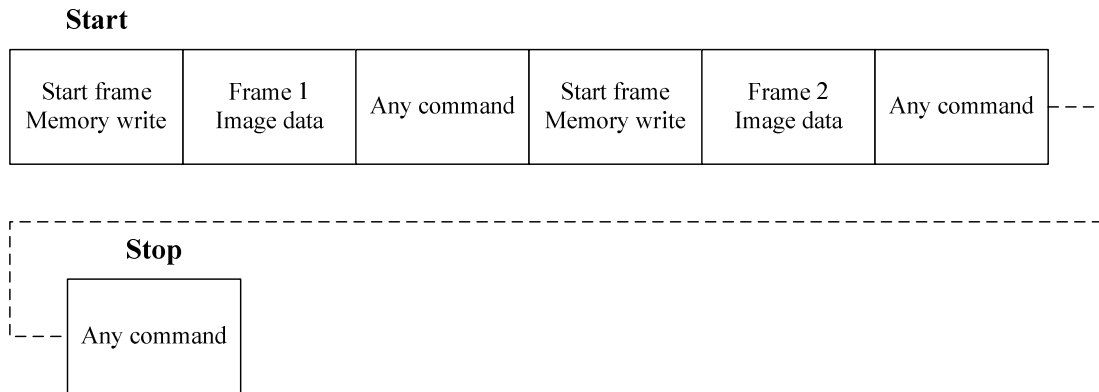
*Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.*

*Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in*

    *the frame memory.*

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## 9.7 Data Color Coding

### 9.7.1 8-bit Parallel Interface (IM2, IM1, IM0= "100")

Different display data formats are available for three Colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

### 9.7.2 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= "03h"
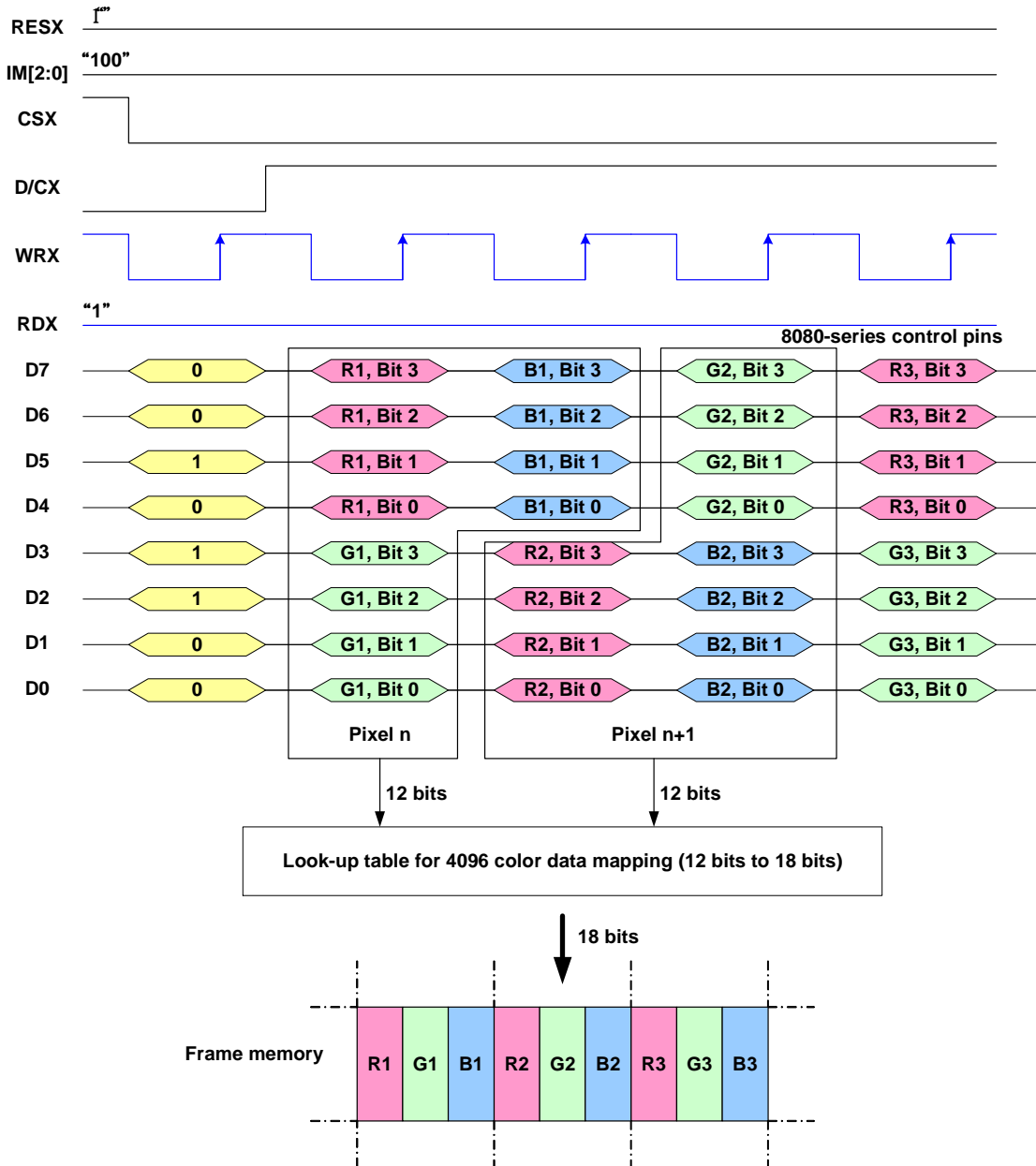


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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### 9.7.3 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 2-byte
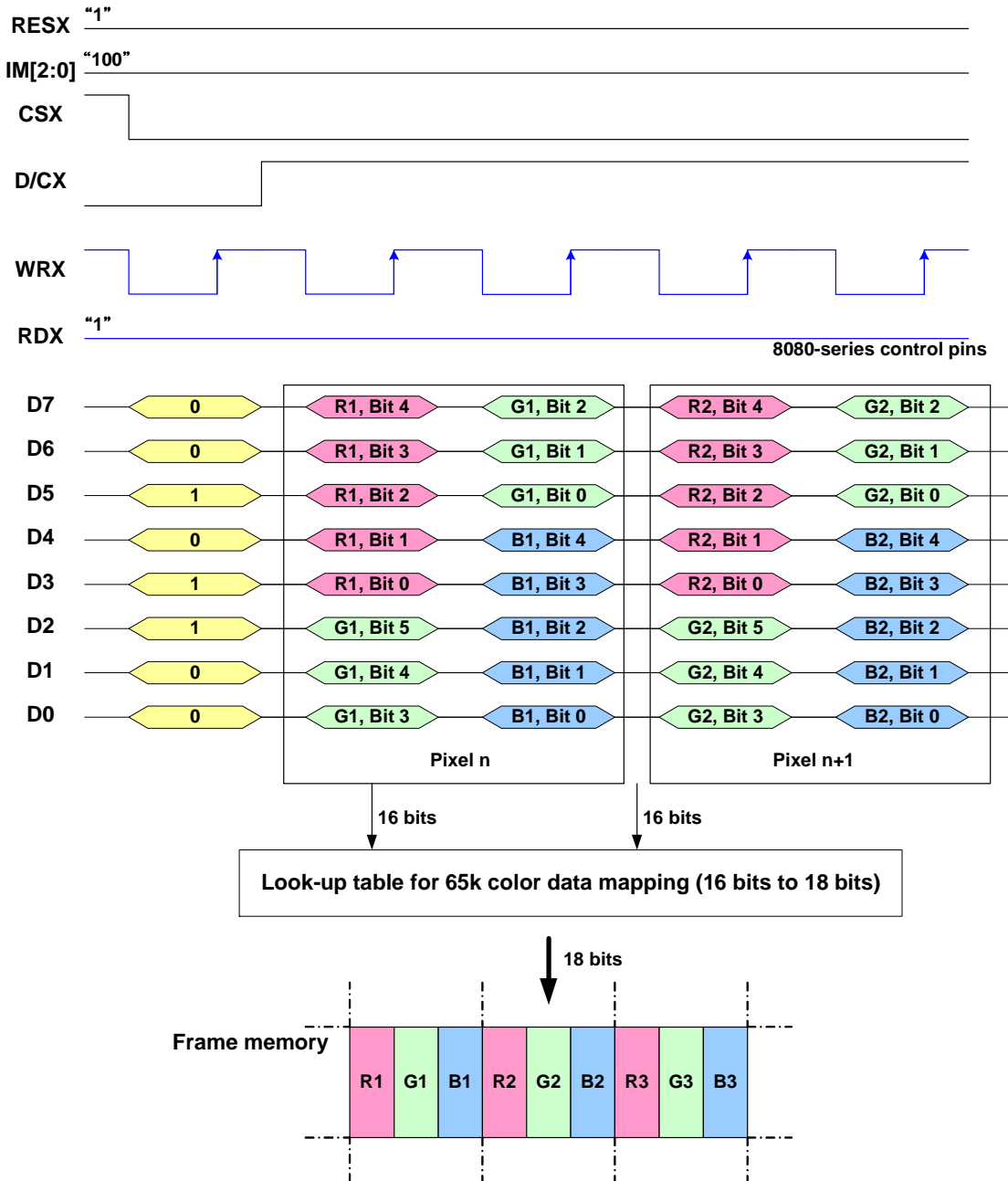
| | | | |
|---|---|---|---|
| RESX | "1" | | |
| IM[2:0] | "100" | | |
| CSX | | | |
| D/CX | | | |
| WRX | | | |
| RDX | "1" | | 8080-series control pins |

| | | Pixel n | | Pixel n+1 | |
|---|---|---|---|---|---|
| D7 | 0 | R1, Bit 4 | G1, Bit 2 | R2, Bit 4 | G2, Bit 2 |
| D6 | 0 | R1, Bit 3 | G1, Bit 1 | R2, Bit 3 | G2, Bit 1 |
| D5 | 1 | R1, Bit 2 | G1, Bit 0 | R2, Bit 2 | G2, Bit 0 |
| D4 | 0 | R1, Bit 1 | B1, Bit 4 | R2, Bit 1 | B2, Bit 4 |
| D3 | 1 | R1, Bit 0 | B1, Bit 3 | R2, Bit 0 | B2, Bit 3 |
| D2 | 1 | G1, Bit 5 | B1, Bit 2 | G2, Bit 5 | B2, Bit 2 |
| D1 | 0 | G1, Bit 4 | B1, Bit 1 | G2, Bit 4 | B2, Bit 1 |
| D0 | 0 | G1, Bit 3 | B1, Bit 0 | G2, Bit 3 | B2, Bit 0 |

16 bits          16 bits

**Look-up table for 65k color data mapping (16 bits to 18 bits)**

18 bits

**Frame memory**  R1 G1 B1 R2 G2 B2 R3 G3 B3

Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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### 9.7.4 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= "06h"

There is 1 pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

#### 9.7.5 16-Bit Parallel Interface (IM2,IM1, IM0= "101")

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

#### 9.7.6 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= "03h"

There is 1 pixel (3 sub-pixels) per 1 byte

| | | Pixel n | Pixel n+1 | Pixel n+2 | Pixel n+3 |
|---|---|---|---|---|---|
| RESX | "1" | | | | |
| IM[2:0] | "101" | | | | |
| CSX | | | | | |
| D/CX | | | | | |
| WRX | | | | | |
| RDX | "1" | | 8080-series control pins | | |
| D15 | - | - | - | - | - |
| D14 | - | - | - | - | - |
| D13 | - | - | - | - | - |
| D12 | - | - | - | - | - |
| D11 | - | R1, Bit 3 | R2, Bit 3 | R3, Bit 3 | R4, Bit 3 |
| D10 | - | R1, Bit 2 | R2, Bit 2 | R3, Bit 2 | R4, Bit 2 |
| D9 | - | R1, Bit 1 | R2, Bit 1 | R3, Bit 1 | R4, Bit 1 |
| D8 | - | R1, Bit 0 | R2, Bit 0 | R3, Bit 0 | R4, Bit 0 |
| D7 | 0 | G1, Bit 3 | G2, Bit 3 | G3, Bit 3 | G4, Bit 3 |
| D6 | 0 | G1, Bit 2 | G2, Bit 2 | G3, Bit 2 | G4, Bit 2 |
| D5 | 1 | G1, Bit 1 | G2, Bit 1 | G3, Bit 1 | G4, Bit 1 |
| D4 | 0 | G1, Bit 0 | G2, Bit 0 | G3, Bit 0 | G4, Bit 0 |
| D3 | 1 | B1, Bit 3 | B2, Bit 3 | B3, Bit 3 | B4, Bit 3 |
| D2 | 1 | B1, Bit 2 | B2, Bit 2 | B3, Bit 2 | B4, Bit 2 |
| D1 | 0 | B1, Bit 1 | B2, Bit 1 | B3, Bit 1 | B4, Bit 1 |
| D0 | 0 | B1, Bit 0 | B2, Bit 0 | B3, Bit 0 | B4, Bit 0 |

12 bits → 12 bits →

**Look-up table for 4096 color data mapping (12 bits to 18 bits)**

18 bits ↓

**Frame memory** | R1 | G1 | B1 | R2 | G2 | B2 | R3 | G3 | B3 |

*Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2: 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.*

### 9.7.7 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 1 byte



**Look-up table for 65k color data mapping (16 bits to 18 bits)**

**Frame memory** R1 G1 B1 R2 G2 B2 R3 G3 B3
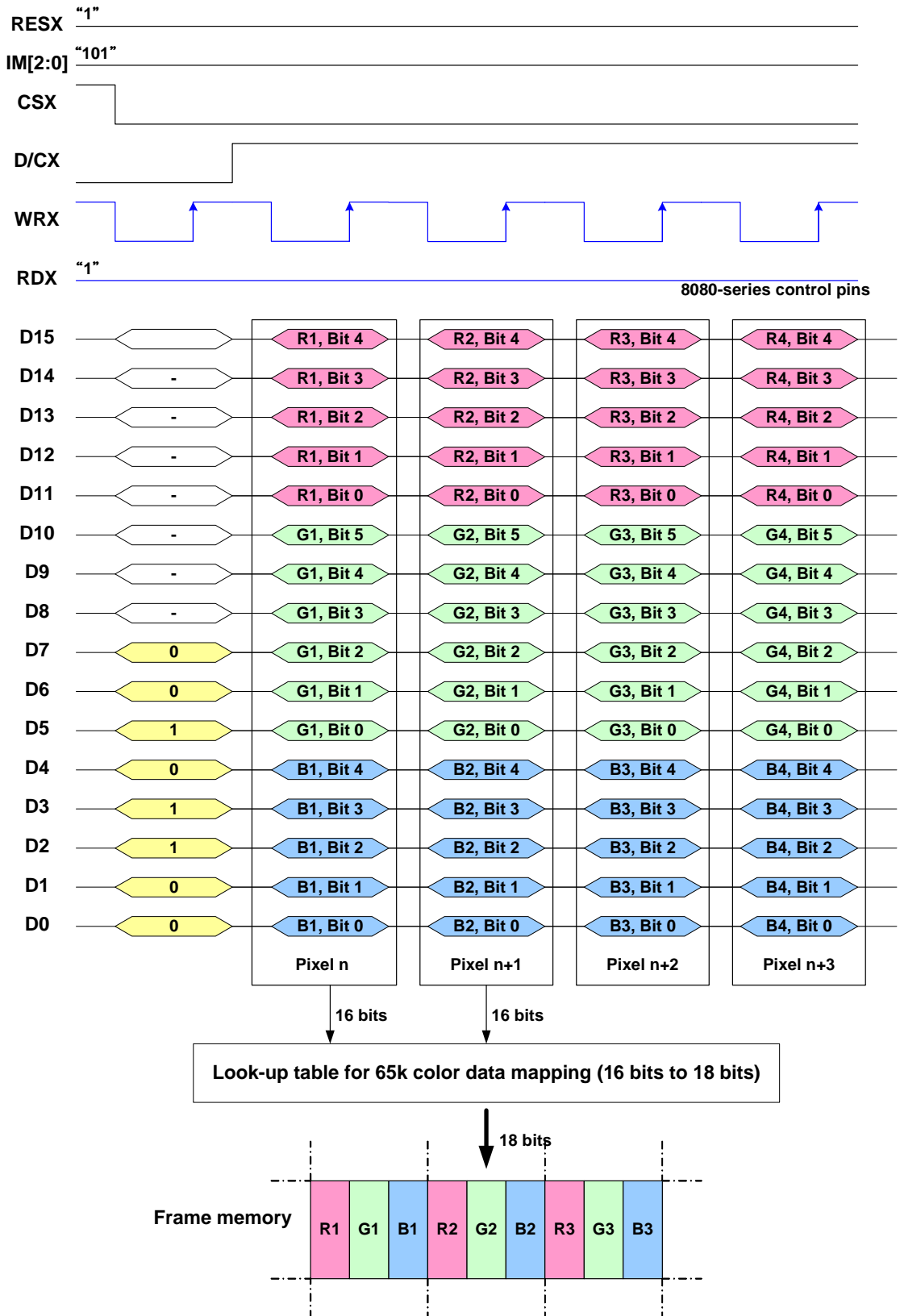
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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### 9.7.8    16-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= "06h"

There are 2 pixels (6 sub-pixels) per 3 bytes
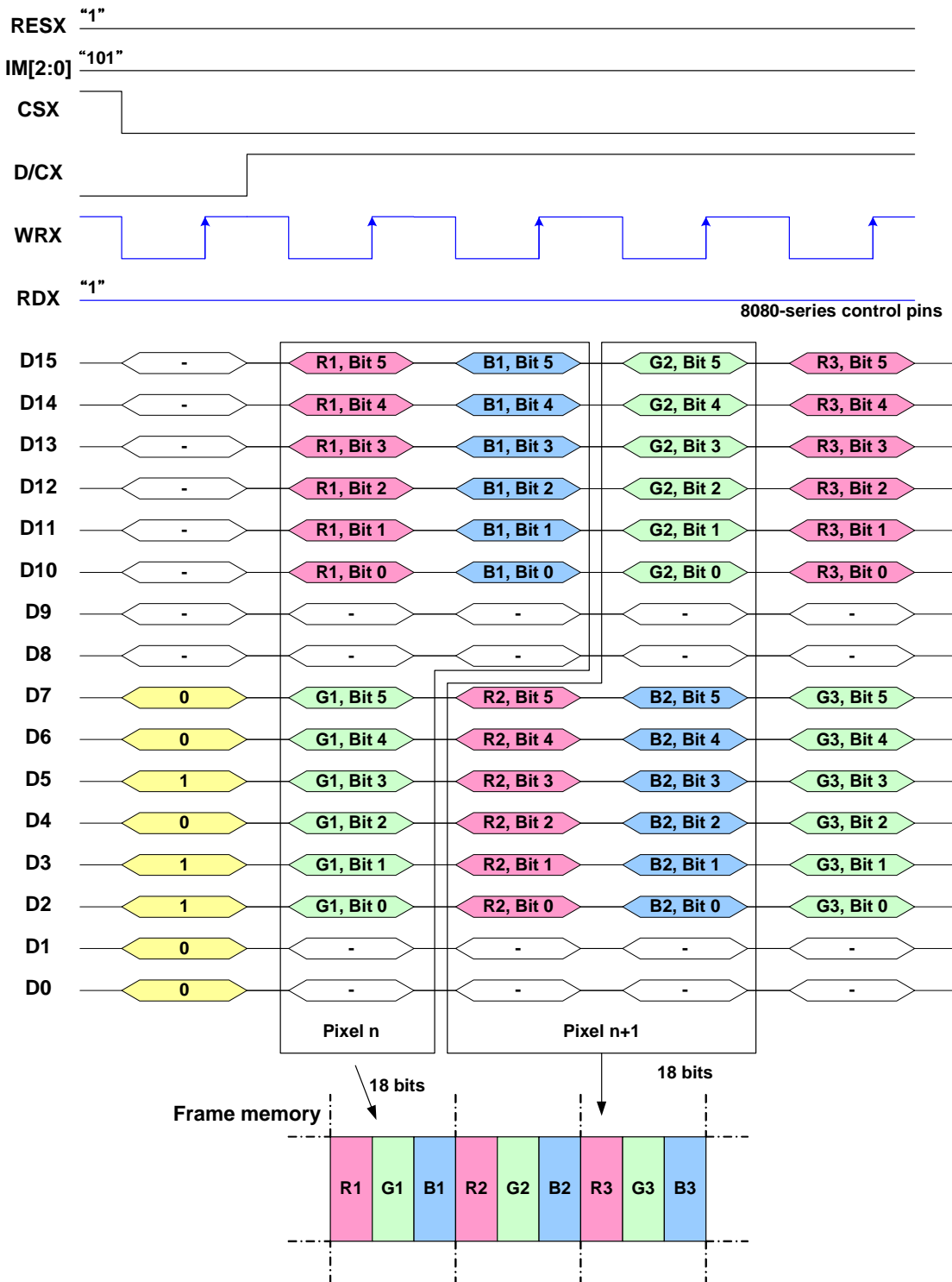


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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### 9.7.9 9-Bit Parallel Interface (IM2, IM1, IM0="110")

Different display data formats are available for three colors depth supported by listed below.
-262k colors, RGB 6,6,6-bit input

### 9.7.10 Write 9-bit data for RGB 6-6-6-bit input (262k-color)

There is 1 pixel (6 sub-pixels) per 3 bytes
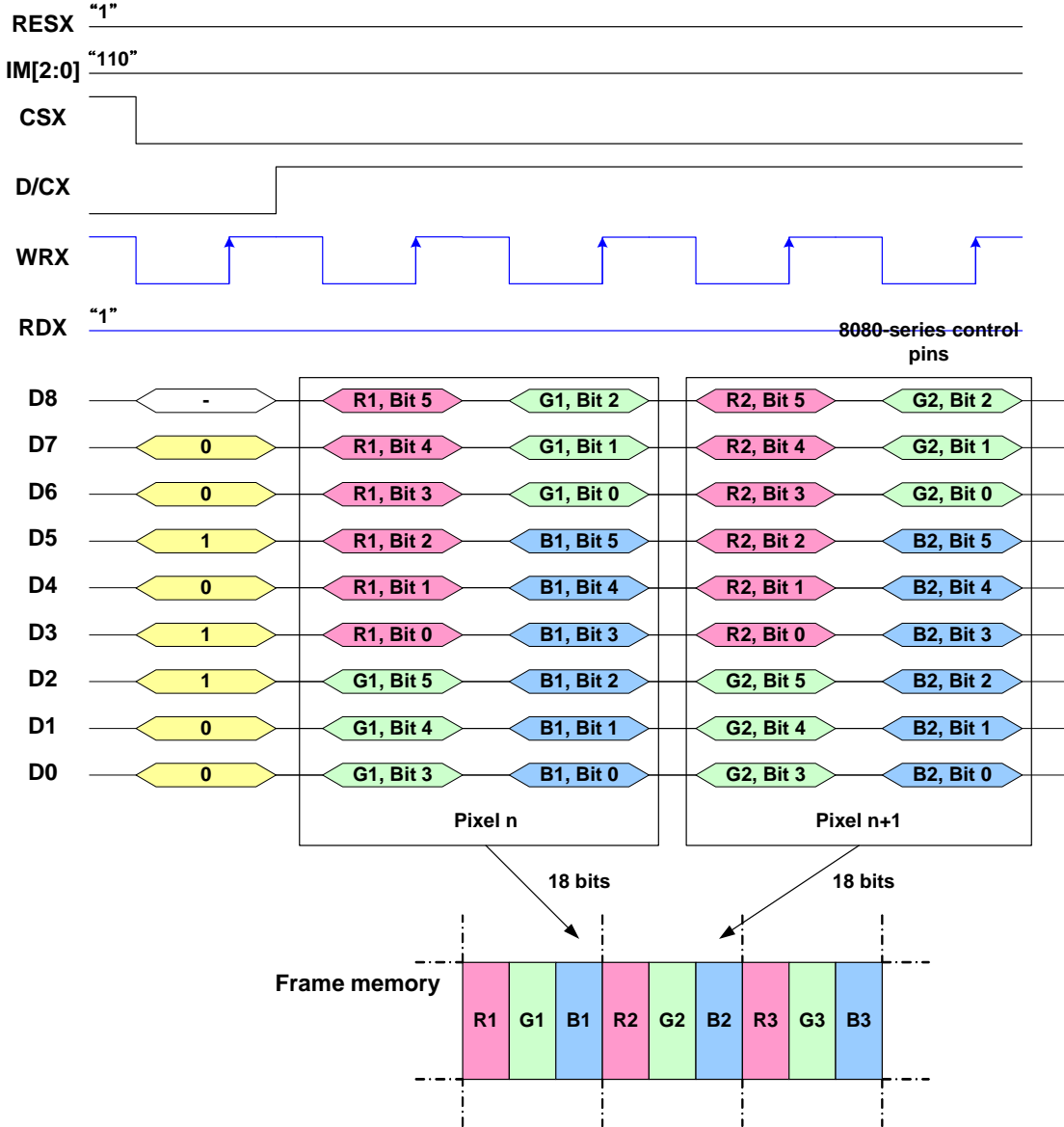


*Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.*

*Note 3: '-' = Don't care - Can be set to '0' or '1'*

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### 9.7.11 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

### 9.7.12 18-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

There is 1 pixel (3 sub-pixels) per 1 byte
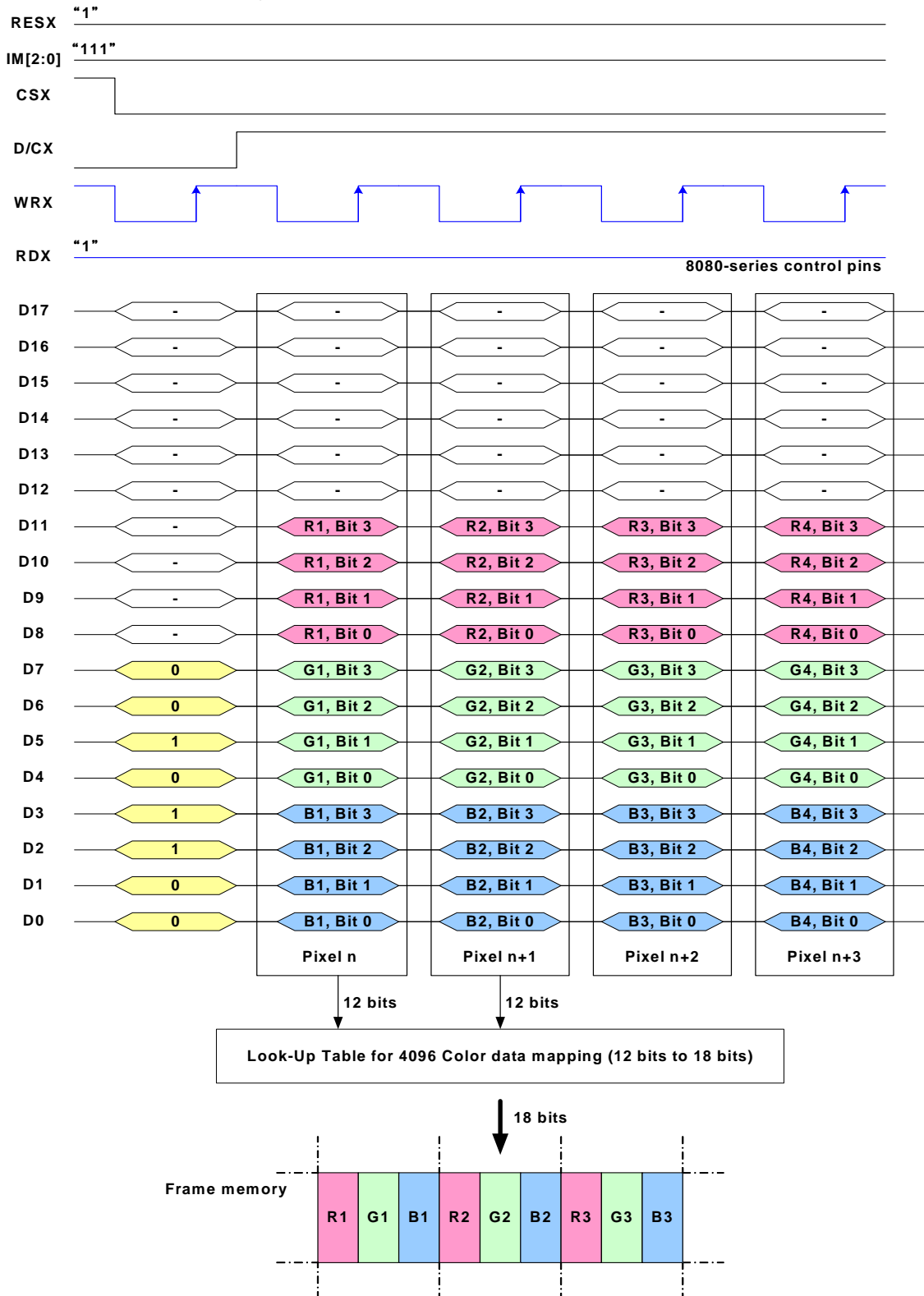


*Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2: 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.*

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### 9.7.13  18-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

There is 1 pixel (3 sub-pixels) per 1 byte

| | Pixel n | Pixel n+1 | Pixel n+2 | Pixel n+3 |
|---|---|---|---|---|
| RESX "1" | | | | |
| IM[2:0] "111" | | | | |
| CSX | | | | |
| D/CX | | | | |
| WRX | | | | |
| RDX "1" | | 8080-series control pins | | |
| D17 | - | - | - | - | - |
| D16 | - | - | - | - | - |
| D15 | - | R1, Bit 4 | R2, Bit 4 | R3, Bit 4 | R4, Bit 4 |
| D14 | - | R1, Bit 3 | R2, Bit 3 | R3, Bit 3 | R4, Bit 3 |
| D13 | - | R1, Bit 2 | R2, Bit 2 | R3, Bit 2 | R4, Bit 2 |
| D12 | - | R1, Bit 1 | R2, Bit 1 | R3, Bit 1 | R4, Bit 1 |
| D11 | - | R1, Bit 0 | R2, Bit 0 | R3, Bit 0 | R4, Bit 0 |
| D10 | - | G1, Bit 5 | G2, Bit 5 | G3, Bit 5 | G4, Bit 5 |
| D9 | - | G1, Bit 4 | G2, Bit 4 | G3, Bit 4 | G4, Bit 4 |
| D8 | - | G1, Bit 3 | G2, Bit 3 | G3, Bit 3 | G4, Bit 3 |
| D7 | 0 | G1, Bit 2 | G2, Bit 2 | G3, Bit 2 | G4, Bit 2 |
| D6 | 0 | G1, Bit 1 | G2, Bit 1 | G3, Bit 1 | G4, Bit 1 |
| D5 | 1 | G1, Bit 0 | G2, Bit 0 | G3, Bit 0 | G4, Bit 0 |
| D4 | 0 | B1, Bit 4 | B2, Bit 4 | B3, Bit 4 | B4, Bit 4 |
| D3 | 1 | B1, Bit 3 | B2, Bit 3 | B3, Bit 3 | B4, Bit 3 |
| D2 | 1 | B1, Bit 2 | B2, Bit 2 | B3, Bit 2 | B4, Bit 2 |
| D1 | 0 | B1, Bit 1 | B2, Bit 1 | B3, Bit 1 | B4, Bit 1 |
| D0 | 0 | B1, Bit 0 | B2, Bit 0 | B3, Bit 0 | B4, Bit 0 |

16 bits        16 bits

**Look-up table for 65k color data mapping (16 bits to 18 bits)**

18 bits

**Frame memory** | R1 | G1 | B1 | R2 | G2 | B2 | R3 | G3 | B3 |

Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

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## 9.7.14 18-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 1 byte

| | | Pixel n | Pixel n+1 | Pixel n+2 | Pixel n+3 |
|---|---|---|---|---|---|
| RESX | "1" | | | | |
| IM[2:0] | "111" | | | | |
| CSX | | | | | |
| D/CX | | | | | |
| WRX | | | | | |
| RDX | "1" | | | 8080-series control pins | |
| D17 | - | R1, Bit 5 | R2, Bit 5 | R3, Bit 5 | R4, Bit 5 |
| D16 | - | R1, Bit 4 | R2, Bit 4 | R3, Bit 4 | R4, Bit 4 |
| D15 | - | R1, Bit 3 | R2, Bit 3 | R3, Bit 3 | R4, Bit 3 |
| D14 | - | R1, Bit 2 | R2, Bit 2 | R3, Bit 2 | R4, Bit 2 |
| D13 | - | R1, Bit 1 | R2, Bit 1 | R3, Bit 1 | R4, Bit 1 |
| D12 | - | R1, Bit 0 | R2, Bit 0 | R3, Bit 0 | R4, Bit 0 |
| D11 | - | G1, Bit 5 | G2, Bit 5 | G3, Bit 5 | G4, Bit 5 |
| D10 | - | G1, Bit 4 | G2, Bit 4 | G3, Bit 4 | G4, Bit 4 |
| D9 | - | G1, Bit 3 | G2, Bit 3 | G3, Bit 3 | G4, Bit 3 |
| D8 | - | G1, Bit 2 | G2, Bit 2 | G3, Bit 2 | G4, Bit 2 |
| D7 | 0 | G1, Bit 1 | G2, Bit 1 | G3, Bit 1 | G4, Bit 1 |
| D6 | 0 | G1, Bit 0 | G2, Bit 0 | G3, Bit 0 | G4, Bit 0 |
| D5 | 1 | B1, Bit 5 | B2, Bit 5 | B3, Bit 5 | B4, Bit 5 |
| D4 | 0 | B1, Bit 4 | B2, Bit 4 | B3, Bit 4 | B4, Bit 4 |
| D3 | 1 | B1, Bit 3 | B2, Bit 3 | B3, Bit 3 | B4, Bit 3 |
| D2 | 1 | B1, Bit 2 | B2, Bit 2 | B3, Bit 2 | B4, Bit 2 |
| D1 | 0 | B1, Bit 1 | B2, Bit 1 | B3, Bit 1 | B4, Bit 1 |
| D0 | 0 | B1, Bit 0 | B2, Bit 0 | B3, Bit 0 | B4, Bit 0 |

18 bits  18 bits

Frame memory | R1 | G1 | B1 | R2 | G2 | B2 | R3 | G3 | B3 |

Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

### 9.7.15 3-line serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

### 9.7.16 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



Note 1: Pixel data with the 12-bit color depth information
Note 2: The most significant bits are: Rx3, Gx3 and Bx3
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

### 9.7.17 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"
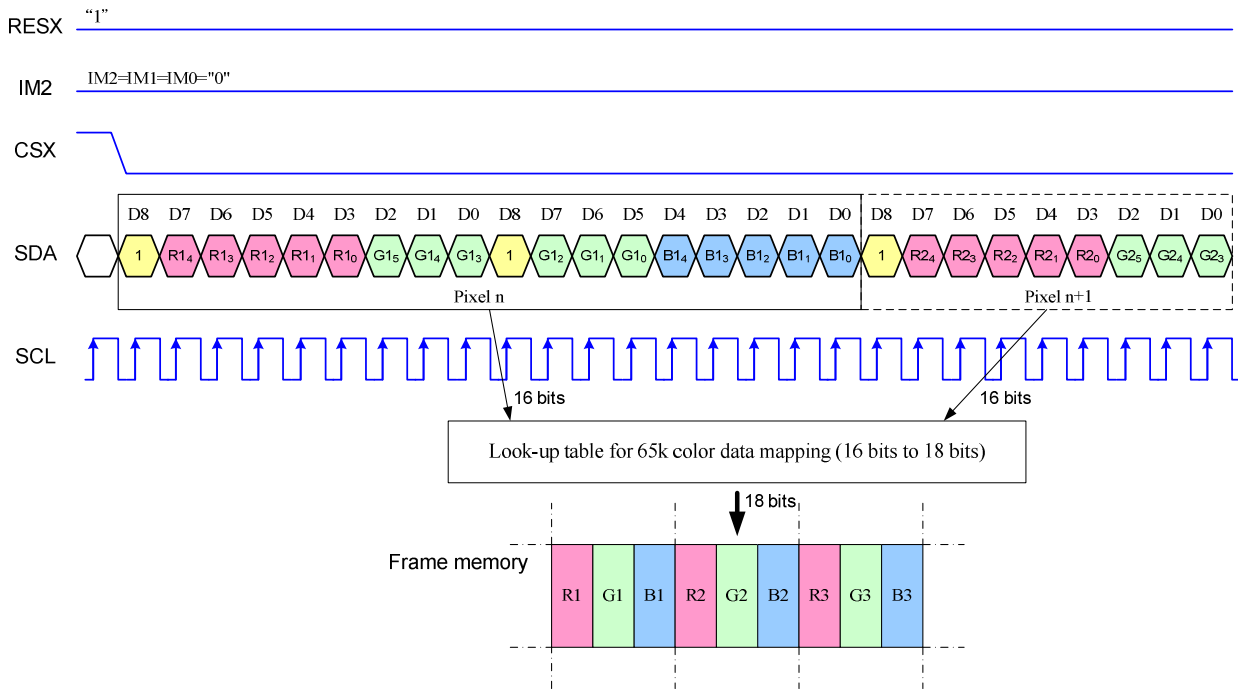


Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

### 9.7.18 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



*Note 1: Pixel data with the 18-bit color depth information*
*Note 2: The most significant bits are: Rx5, Gx5 and Bx5*
*Note 3: The least significant bits are: Rx0, Gx0 and Bx0*

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### 9.7.19 4-line serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

### 9.7.20 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"
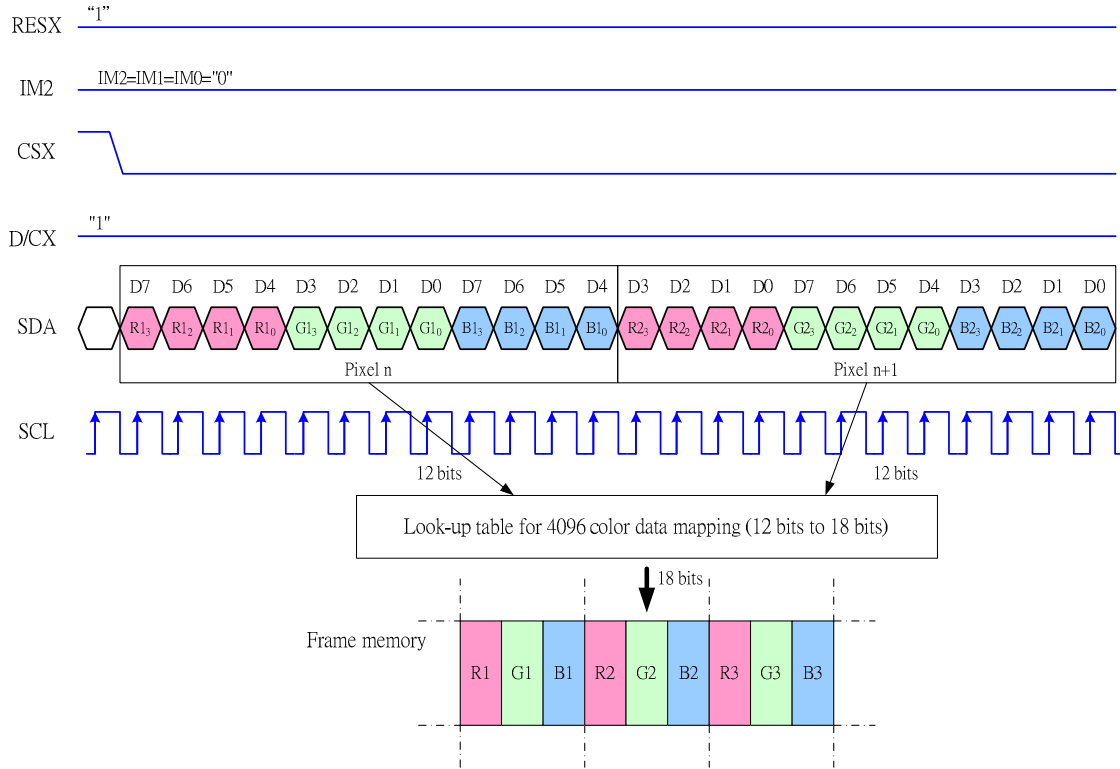


Note 1: Pixel data with the 12-bit color depth information
Note 2: The most significant bits are: Rx3, Gx3 and Bx3
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

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**9.7.21 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"**
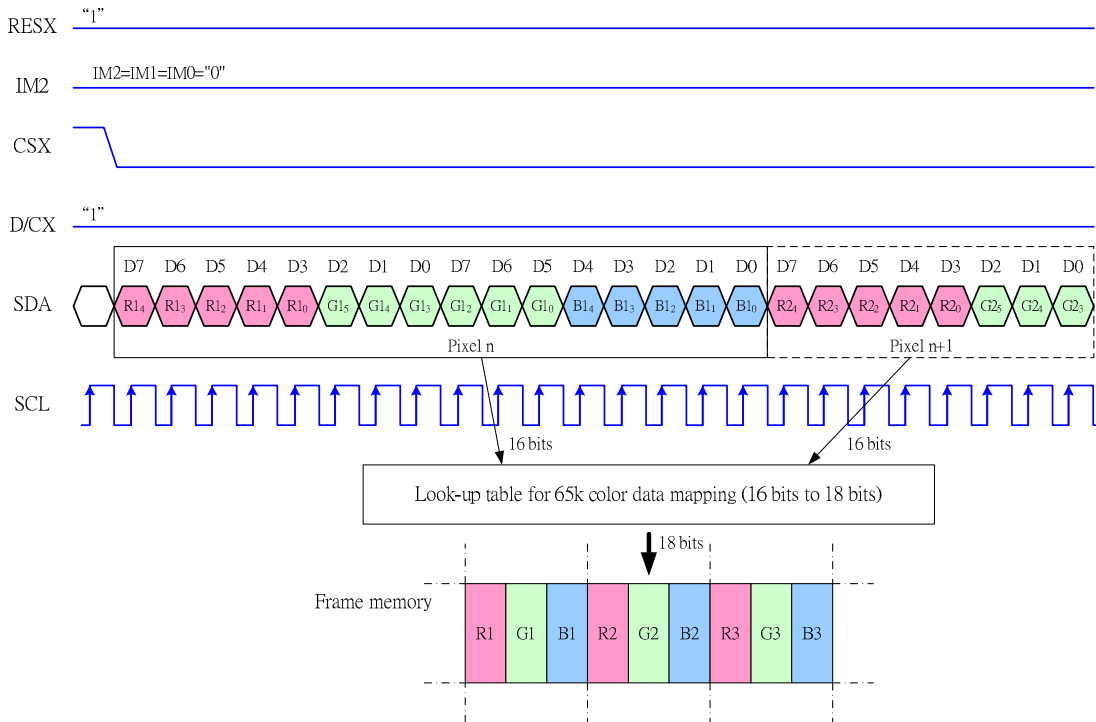


*Note 1: Pixel data with the 16-bit color depth information*
*Note 2: The most significant bits are: Rx4, Gx5 and Bx4*
*Note 3: The least significant bits are: Rx0, Gx0 and Bx0*

### 9.7.22 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"
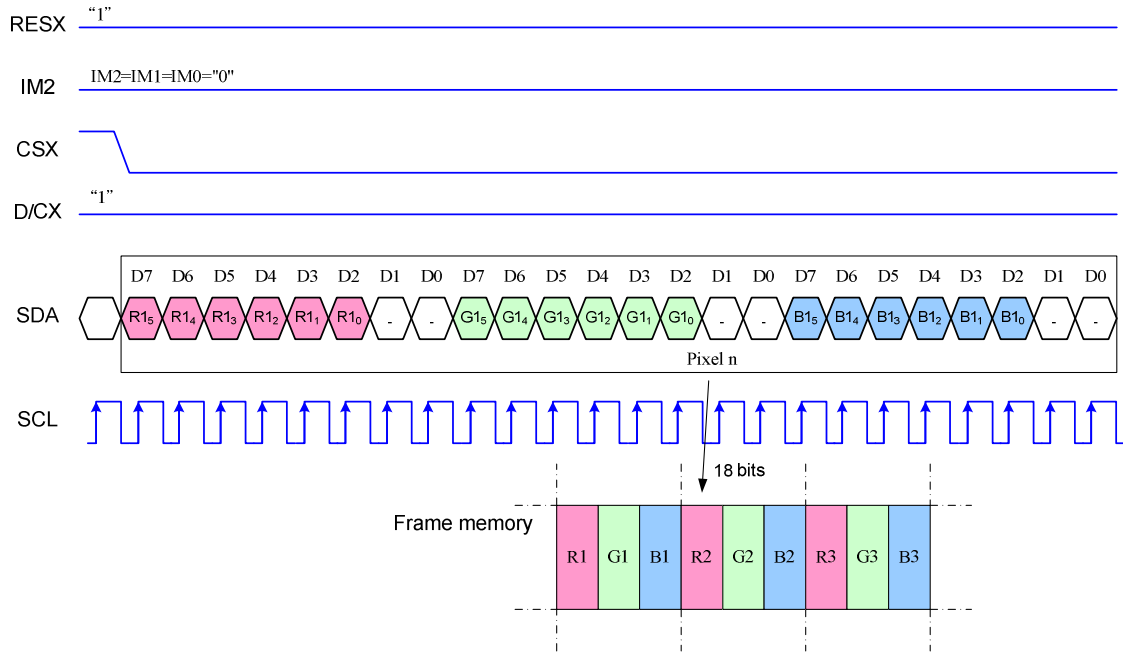


Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

## 9.8 Display Data RAM

### 9.8.1 Configuration (GM[2:0] = "000")

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bit memory allows storing on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.
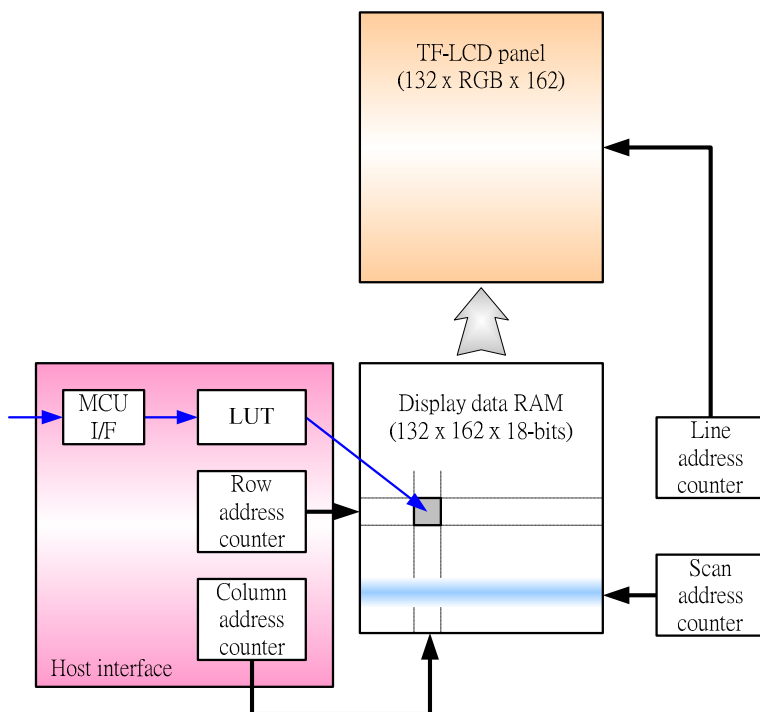


Fig. 9.8.1 Display data RAM organization

### 9.8.2 Memory to Display Address Mapping

### 9.8.2.1 When using 128RGB x 160 resolution (GM[2:0] = "011", SMX=SMY=SRGB= '0')

| Gate Out | Source Out | | S7 | S8 | S9 | S10 | S11 | S12 | -------- | S385 | S386 | S387 | S388 | S389 | S390 | SA | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RA | | RGB=0 | | RGB=1 | RGB=0 | | RGB=1 | RGB Order | RGB=0 | | RGB=1 | RGB=0 | | RGB=1 | | |
| | MY='0' | MY='1' | | | | | | | | | | | | | | ML='0' | ML='1' |
| 2 | 0 | 159 | R0 | G0 | B0 | R1 | G1 | B1 | -------- | R126 | G126 | B126 | R127 | G127 | B127 | 0 | 159 |
| 3 | 1 | 158 | | | | | | | -------- | | | | | | | 1 | 158 |
| 4 | 2 | 157 | | | | | | | -------- | | | | | | | 2 | 157 |
| 5 | 3 | 156 | | | | | | | -------- | | | | | | | 3 | 156 |
| 6 | 4 | 155 | | | | | | | -------- | | | | | | | 4 | 155 |
| 7 | 5 | 154 | | | | | | | -------- | | | | | | | 5 | 154 |
| 8 | 6 | 153 | | | | | | | -------- | | | | | | | 6 | 153 |
| 9 | 7 | 152 | | | | | | | -------- | | | | | | | 7 | 152 |
| I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I |
| I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I |
| I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I |
| I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I |
| I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I | I |
| 154 | 152 | 7 | | | | | | | -------- | | | | | | | 152 | 7 |
| 155 | 153 | 6 | | | | | | | -------- | | | | | | | 153 | 6 |
| 156 | 154 | 5 | | | | | | | -------- | | | | | | | 154 | 5 |
| 157 | 155 | 4 | | | | | | | -------- | | | | | | | 155 | 4 |
| 158 | 156 | 3 | | | | | | | -------- | | | | | | | 156 | 3 |
| 159 | 157 | 2 | | | | | | | -------- | | | | | | | 157 | 2 |
| 160 | 158 | 1 | | | | | | | -------- | | | | | | | 158 | 1 |
| 161 | 159 | 0 | | | | | | | -------- | | | | | | | 159 | 0 |
| | CA | MX='0' | 0 | | | 1 | | | -------- | 126 | | | 127 | | | | |
| | | MX='1' | 127 | | | 126 | | | -------- | 1 | | | 0 | | | | |

Pixel 1 | Pixel 2 | -------- | Pixel 127 | Pixel 128

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

### 9.8.2.2 When using 132RGB x 162 resolution (GM[2:0] = "000", SMX=SMY=SRGB= '0')
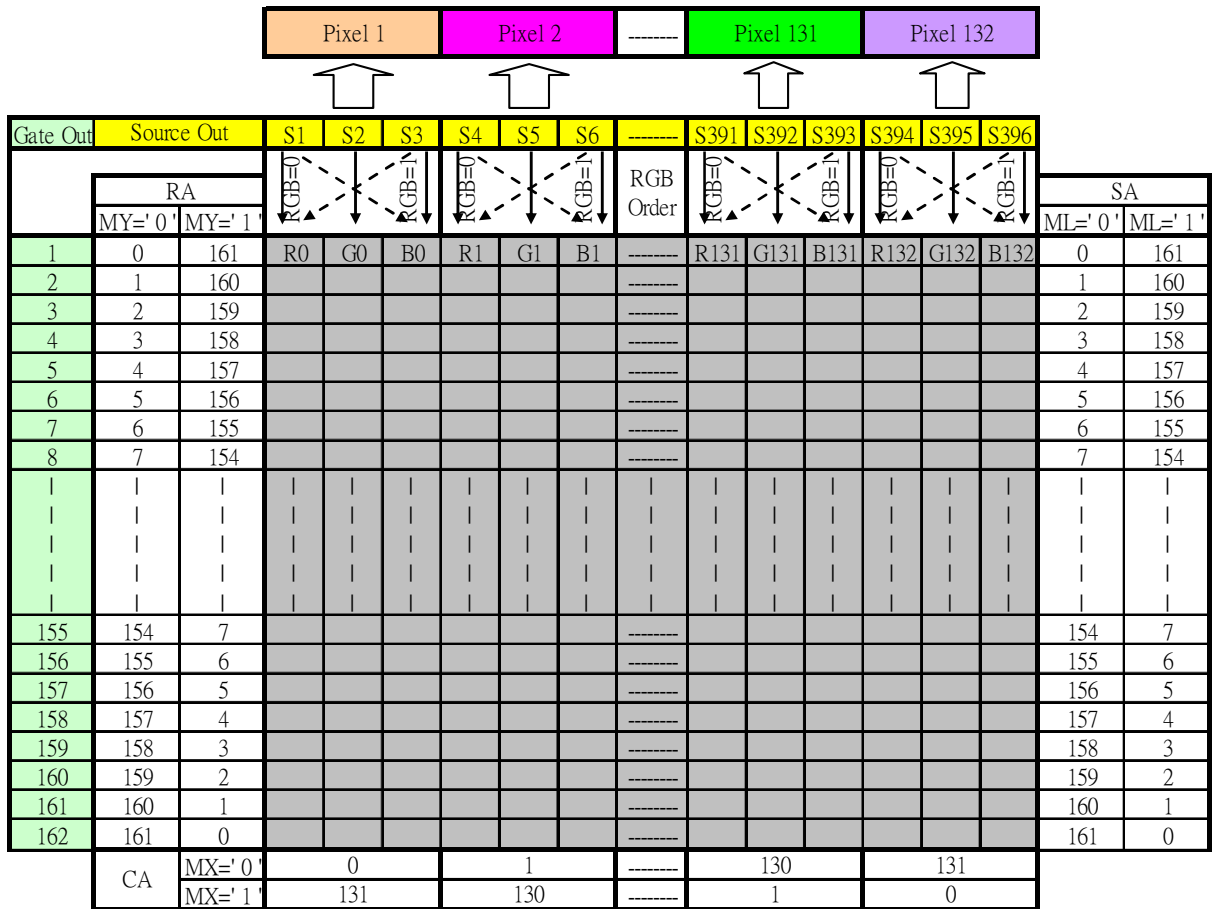
| | | Pixel 1 | | | Pixel 2 | | | -------- | Pixel 131 | | | Pixel 132 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Gate Out | Source Out | | S1 | S2 | S3 | S4 | S5 | S6 | -------- | S391 | S392 | S393 | S394 | S395 | S396 | SA | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RA | | | | | | | | RGB Order | | | | | | | SA | |
| | MY='0' | MY='1' | | | | | | | | | | | | | | ML='0' | ML='1' |
| 1 | 0 | 161 | R0 | G0 | B0 | R1 | G1 | B1 | -------- | R131 | G131 | B131 | R132 | G132 | B132 | 0 | 161 |
| 2 | 1 | 160 | | | | | | | -------- | | | | | | | 1 | 160 |
| 3 | 2 | 159 | | | | | | | -------- | | | | | | | 2 | 159 |
| 4 | 3 | 158 | | | | | | | -------- | | | | | | | 3 | 158 |
| 5 | 4 | 157 | | | | | | | -------- | | | | | | | 4 | 157 |
| 6 | 5 | 156 | | | | | | | -------- | | | | | | | 5 | 156 |
| 7 | 6 | 155 | | | | | | | -------- | | | | | | | 6 | 155 |
| 8 | 7 | 154 | | | | | | | -------- | | | | | | | 7 | 154 |
| \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| |
| 155 | 154 | 7 | | | | | | | -------- | | | | | | | 154 | 7 |
| 156 | 155 | 6 | | | | | | | -------- | | | | | | | 155 | 6 |
| 157 | 156 | 5 | | | | | | | -------- | | | | | | | 156 | 5 |
| 158 | 157 | 4 | | | | | | | -------- | | | | | | | 157 | 4 |
| 159 | 158 | 3 | | | | | | | -------- | | | | | | | 158 | 3 |
| 160 | 159 | 2 | | | | | | | -------- | | | | | | | 159 | 2 |
| 161 | 160 | 1 | | | | | | | -------- | | | | | | | 160 | 1 |
| 162 | 161 | 0 | | | | | | | -------- | | | | | | | 161 | 0 |
| | CA | MX='0' | 0 | | | 1 | | | -------- | 130 | | | 131 | | | | |
| | | MX='1' | 131 | | | 130 | | | -------- | 1 | | | 0 | | | | |

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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### 9.8.3   Normal Display On or Partial Mode On

### 9.8.3.1  When using 128RGB x 160 resolution (GM[2:0] = "011")

In this mode, the content of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')
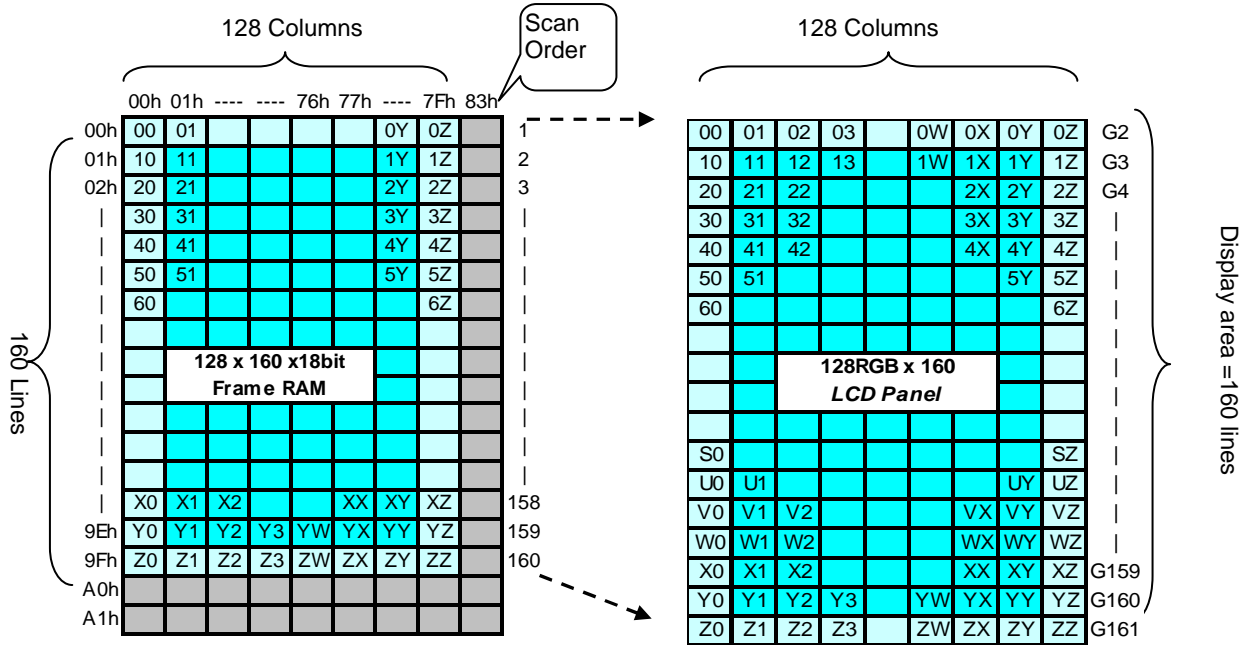


2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MV=ML='0' ,SMX=SMY='0')

# ST7735
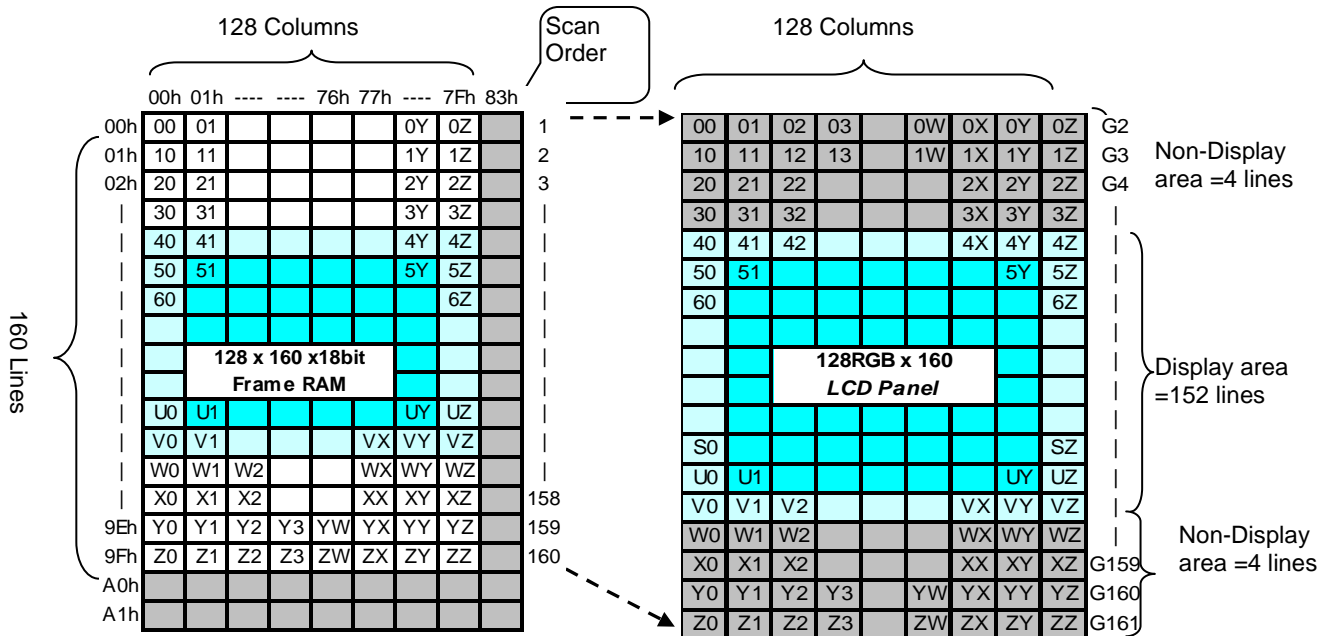
## 9.8.3.2 When using 132RGB x 162 resolution (GM[2:0] = "000")

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0)

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')
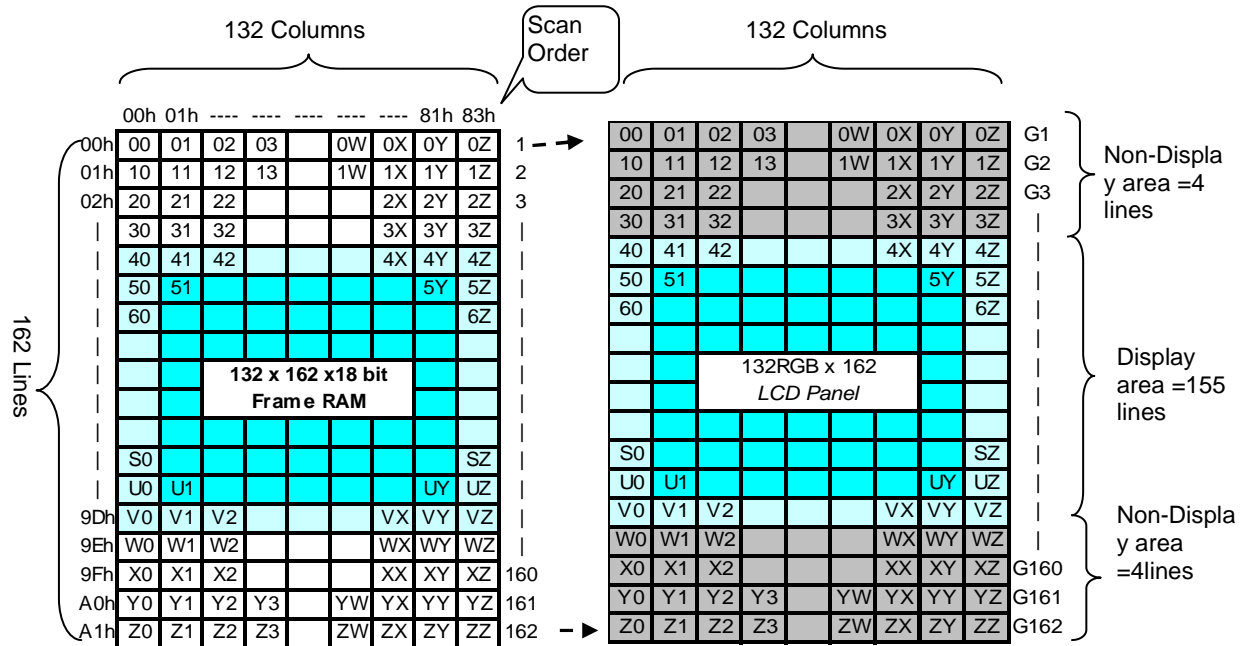


2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Dh, MX=MV=ML='0' ,SMX=SMY='0')
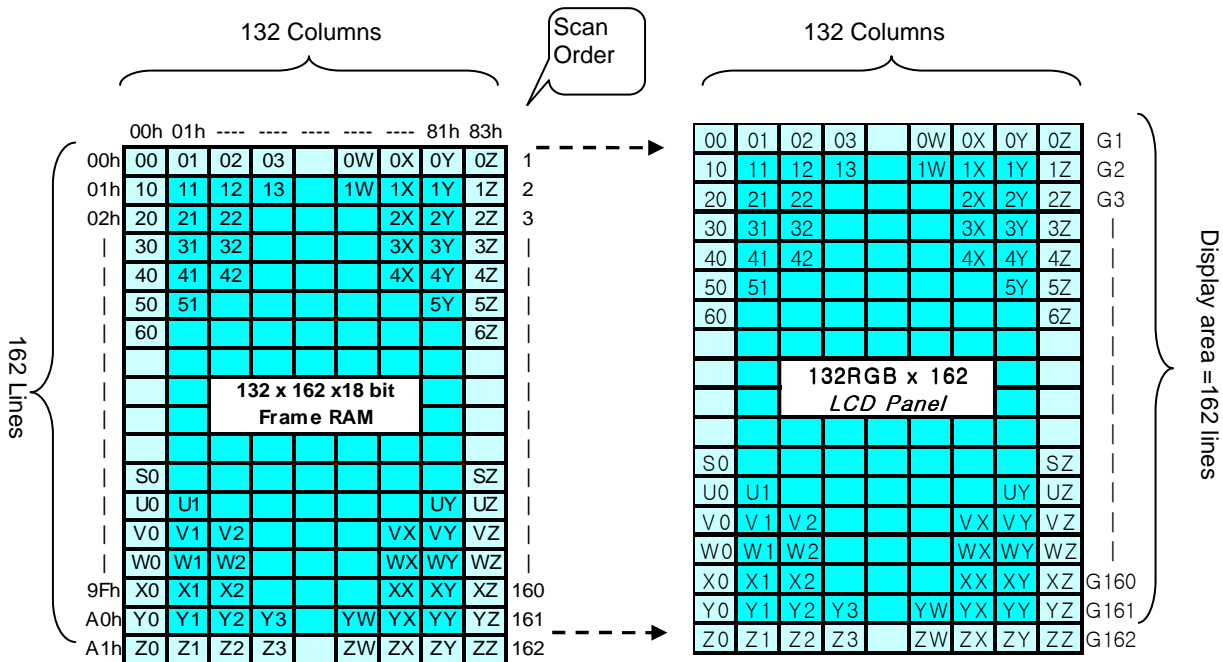
## 9.9 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.
Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET and MADCTL" (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.10 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.10 below

| Condition | Column Counter | Row Counter |
|---|---|---|
| When RAMWR/RAMRD command is accepted | Return to "Start Column (XS)" | Return to "Start Row (YS)" |
| Complete Pixel Read / Write action | Increment by 1 | No change |
| The Column counter value is larger than "End Column (XE)" | Return to "Start Column (XS)" | Increment by 1 |
| The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)" | Return to "Start Column (XS)" | Return to "Start Row (YS)" |

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## 9.10 Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.
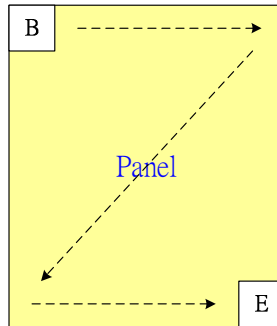


Fig. 9.10.1 Data streaming order

### 9.10.1　When 128RGBx160 (GM= "011")

| MV | MX | MY | CASET | RASET |
|----|----|----|-------|-------|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Row Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (159-Physical Row Pointer) |
| 0 | 1 | 0 | Direct to (127-Physical Column Pointer) | Direct to Physical Row Pointer |
| 0 | 1 | 1 | Direct to (127-Physical Column Pointer) | Direct to (159-Physical Row Pointer) |
| 1 | 0 | 0 | Direct to Physical Row Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (159-Physical Row Pointer) | Direct to Physical Column Pointer |
| 1 | 1 | 0 | Direct to Physical Row Pointer | Direct to (127-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (159-Physical Row Pointer) | Direct to (127-Physical Column Pointer) |

### 9.10.2　When 132RGBx162 (GM= "000")

| MV | MX | MY | CASET | RASET |
|----|----|----|-------|-------|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Row Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (161-Physical Row Pointer) |
| 0 | 1 | 0 | Direct to (131-Physical Column Pointer) | Direct to Physical Row Pointer |
| 0 | 1 | 1 | Direct to (131-Physical Column Pointer) | Direct to (161-Physical Row Pointer) |
| 1 | 0 | 0 | Direct to Physical Row Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (161-Physical Row Pointer) | Direct to Physical Column Pointer |
| 1 | 1 | 0 | Direct to Physical Row Pointer | Direct to (131-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (161-Physical Row Pointer) | Direct to (131-Physical Column Pointer) |

*Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is*

| D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

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### 9.10.3 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

| Display Data Direction | MADCTL Parameter | | | Image in the Host (MPU) | Image in the Driver (DDRAM) |
|---|---|---|---|---|---|
| | MV | MX | MY | | |
| Normal | 0 | 0 | 0 | | |
| Y-Mirror | 0 | 0 | 1 | | |
| X-Mirror | 0 | 1 | 0 | | |
| X-Mirror Y-Mirror | 0 | 1 | 1 | | |
| X-Y Exchange | 1 | 0 | 0 | | |
| X-Y Exchange Y-Mirror | 1 | 0 | 1 | | |
| X-Y Exchange X-Mirror | 1 | 1 | 0 | | |
| X-Y Exchange X-Mirror Y-Mirror | 1 | 1 | 1 | | |

### 9.11 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

#### 9.11.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:
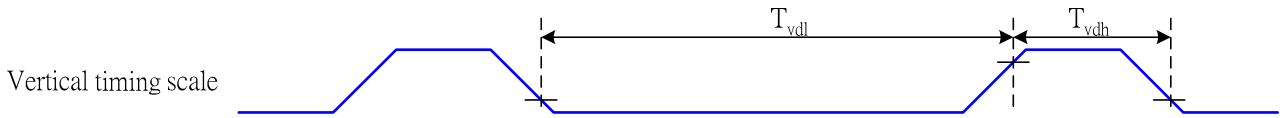


tvdh= The LCD display is not updated from the Frame Memory
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.
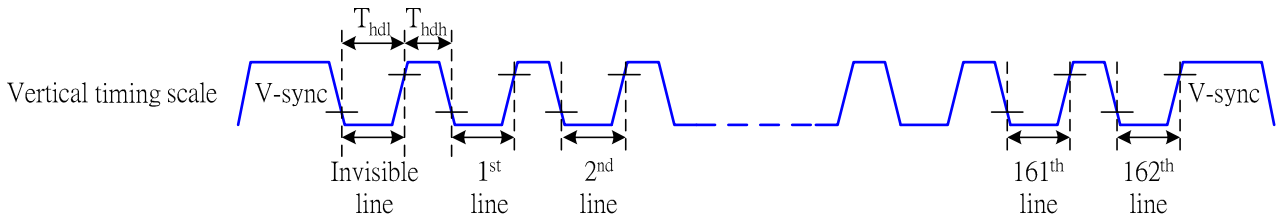


thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)
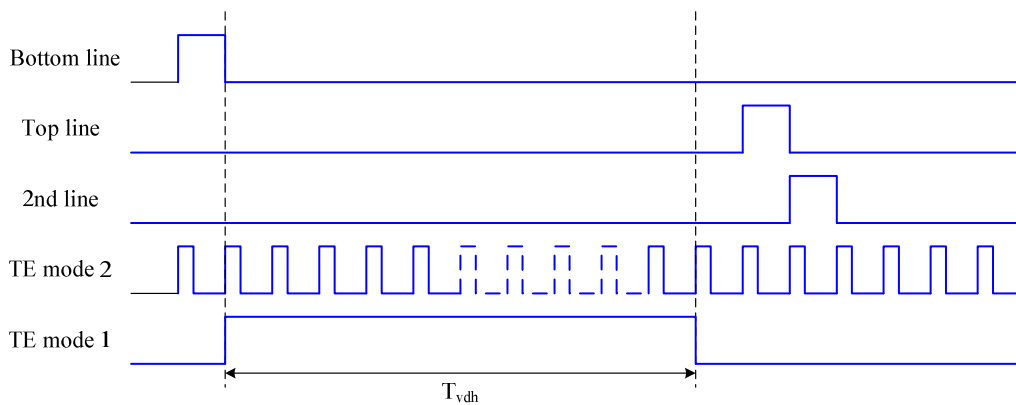


*Note: During Sleep In Mode, the Tearing Output Pin is active Low.*

### 9.11.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:
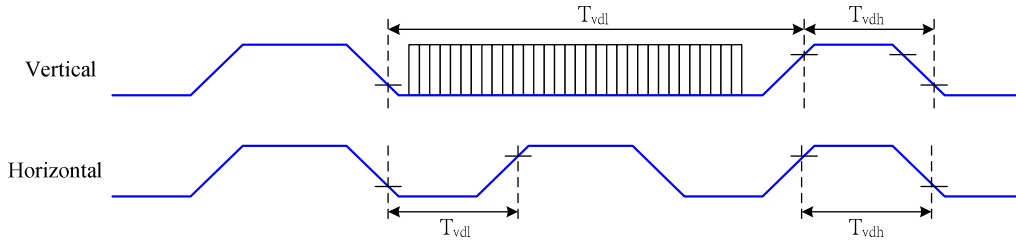


Table 9.11.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

| Symbol | Parameter | min | max | unit | description |
|--------|-----------|-----|-----|------|-------------|
| tvdl | Vertical Timing Low Duration | 13 | - | ms | |
| tvdh | Vertical Timing High Duration | 1000 | - | µs | |
| thdl | Horizontal Timing Low Duration | 33 | - | µs | |
| thdh | Horizontal Timing Low Duration | 25 | 500 | µs | |

*Note: The timings in Table 9.10.1 apply when MADCTL ML=0 and ML=1*

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.
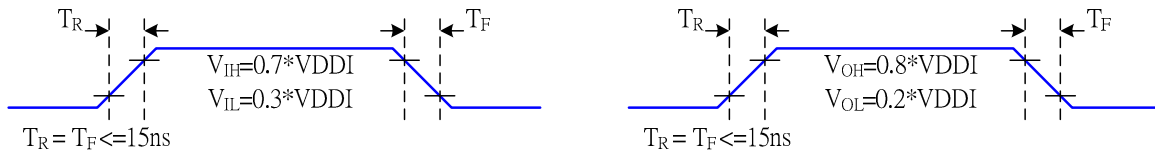


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

### 9.11.3  Example 1: MPU Write is faster than panel read

MCU to memory

1st  162nd  time

TE output signal

time

Memory to LCD

time

1st  162nd

Image on LCD  a  b  c  d
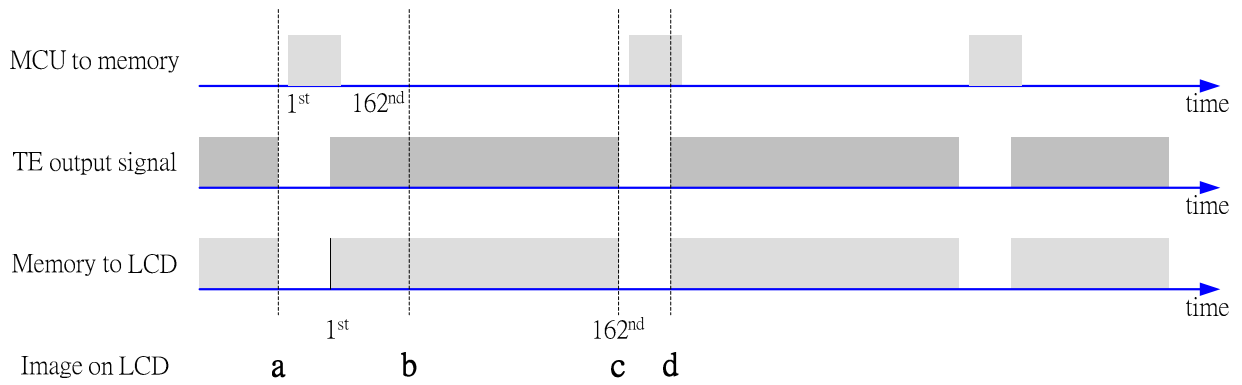
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

Data to be sent

Image on LCD

a  b  c  d
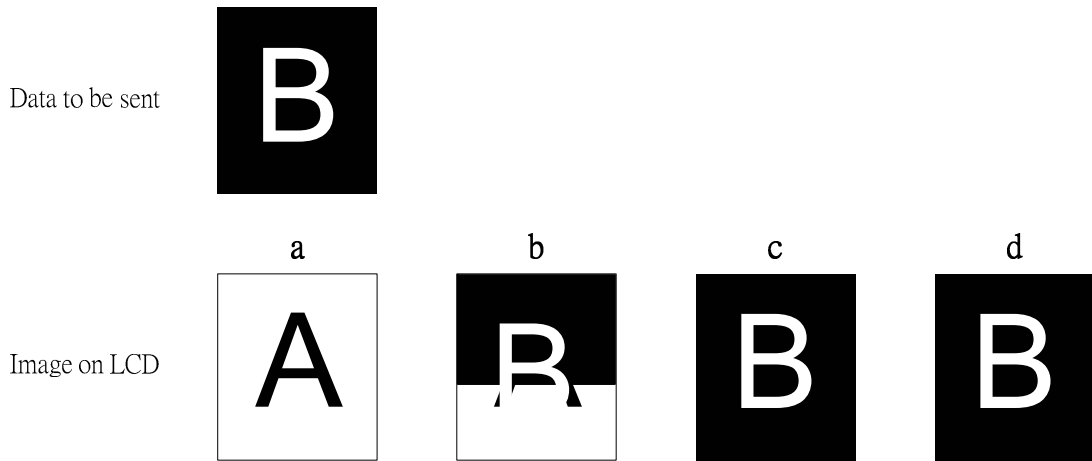
### 9.11.4   Example 2: MPU write is slower than panel read
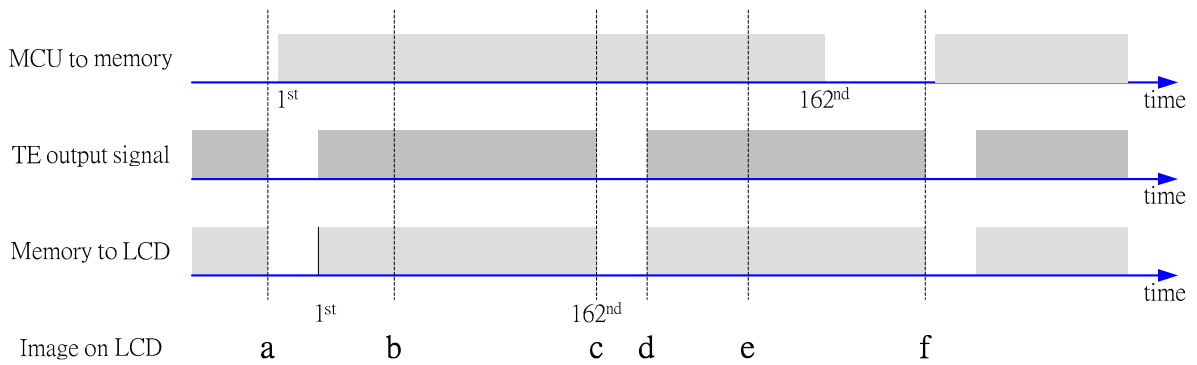


The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.
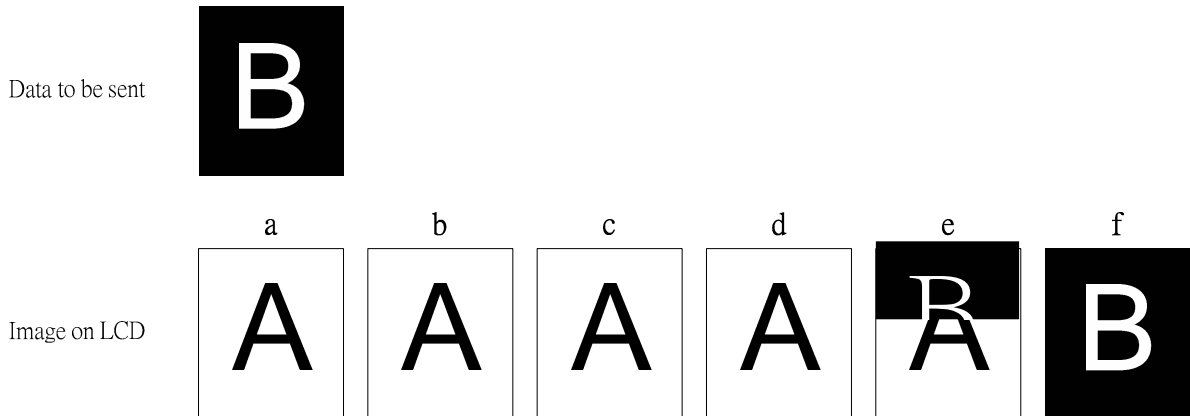
## 9.12 Power ON/OFF Sequence

VDD must be powered on before the VDDI.

VDDI must be powered off before the VDD.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

*Note 1: There will be no damage to the display module if the power sequences are not met.*

*Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*

*Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*

*Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*

The power on/off sequence is illustrated below
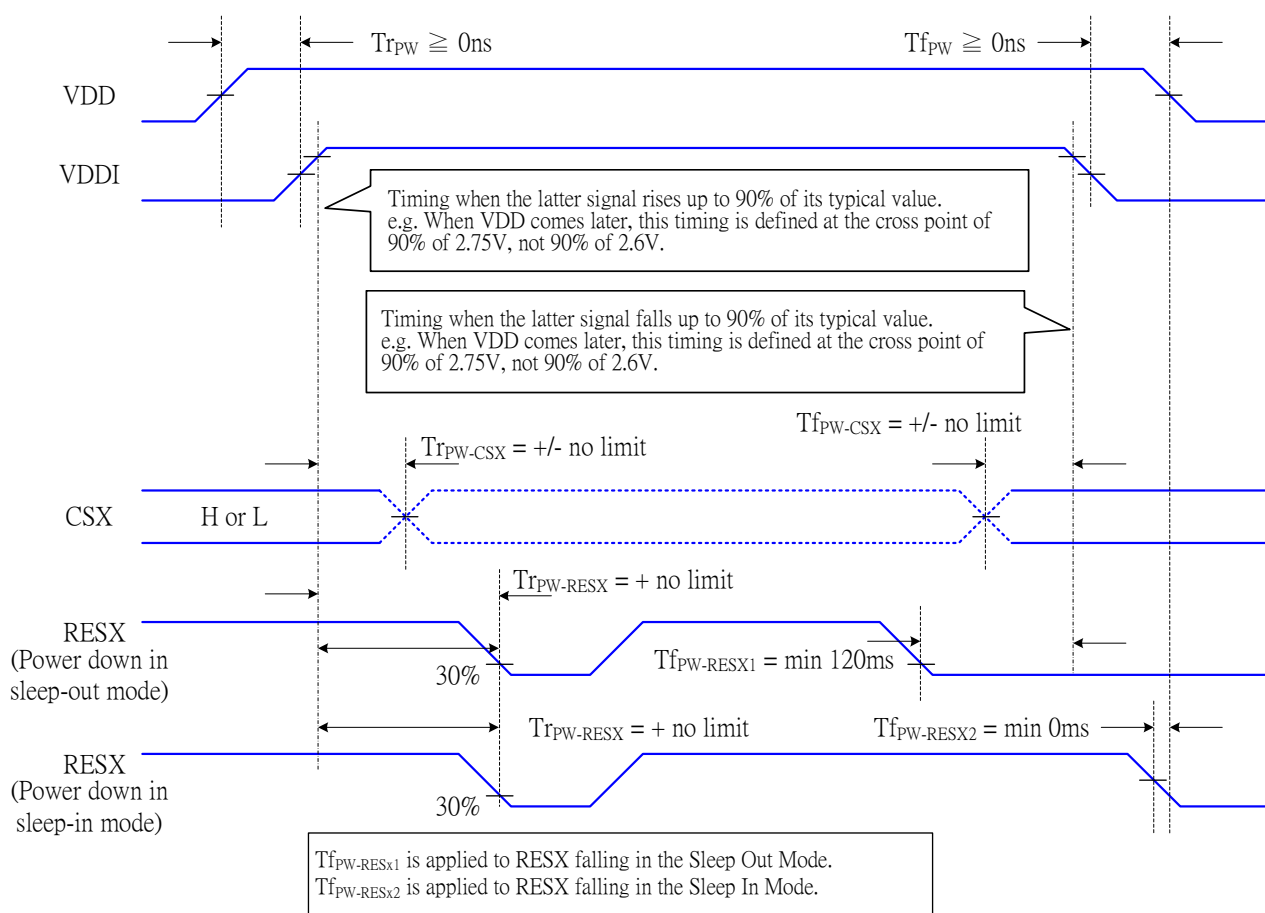


### 9.12.1  Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

### 9.13 Power Level Definition

### 9.13.1  Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.
In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.
In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode
In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode
In this mode, both VDD and VDDI are removed.

*Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.*

**9.13.2  Power Flow Chart**

Normal display mode on = NOR ON
Partial display mode on = PTL ON
Idle mode off = IDM OFF
Idle mode on = IDM ON
Sleep out = SLP OUT
Sleep in = SLP IN

Power on sequence
HW reset
SW reset

NOR ON

PTL ON

SLP IN

Sleep out
Normal display mode on
Idle mode off

SLP OUT

Sleep in
Normal display mode on
Idle mode off

NOR ON

PTL ON

IDM ON        IDM OFF

IDM ON        IDM OFF

Sleep out
Normal display mode on
Idle mode on

SLP IN

SLP OUT

Sleep in
Normal display mode on
Idle mode on

SLP IN

Sleep out
Partial display mode on
Idle mode off

SLP OUT

Sleep in
Partial display mode on
Idle mode off

IDM ON        IDM OFF

IDM ON        IDM OFF

PTL ON

NOR ON

SLP IN

Sleep out
Partial display mode on
Idle mode on

SLP OUT

Sleep in
Partial display mode on
Idle mode on

PTL ON

NOR ON

Sleep out        Sleep in

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**9.14 Reset Table**

**9.14.1   Reset Table (Default Value, GM[2:0]="011", 128RGB x 160)**

| Item | After Power On | After H/W Reset | After S/W Reset |
|---|---|---|---|
| Frame memory | Random | No Change | No Change |
| Sleep In/Out | In | In | In |
| Display On/Off | Off | Off | Off |
| Display mode (normal/partial) | Normal | Normal | Normal |
| Display Inversion On/Off | Off | Off | Off |
| Display Idle Mode On/Off | Off | Off | Off |
| Column: Start Address (XS) | 0000h | 0000h | 0000h |
| Column: End Address (XE) | 007Fh | 007Fh | 007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1) |
| Row: Start Address (YS) | 0000h | 0000h | 0000h |
| Row: End Address (YE) | 009Fh | 009Fh | 009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1) |
| Gamma setting | GC0 | GC0 | GC0 |
| RGB for 4k and 65k Color Mode | See Section 9.17 | See Section 9.17 | No Change |
| Partial: Start Address (PSL) | 0000h | 0000h | 0000h |
| Partial: End Address (PEL) | 009Fh | 009Fh | 009Fh |
| Tearing: On/Off | Off | Off | Off |
| Tearing Effect Mode (*1) | 0 (Mode1) | 0 (Mode1) | 0 (Mode1) |
| Memory Data Access Control (MY/MX/MV/ML/RGB) | 0/0/0/0/0 | 0/0/0/0/0 | No Change |
| Interface Pixel Color Format | 6 (18-Bit/Pixel) | 6 (18-Bit/Pixel) | No Change |
| RDDPM | 08h | 08h | 08h |
| RDDMADCTL | 00h | 00h | No Change |
| RDDCOLMOD | 6 (18-Bit/Pixel) | 6 (18-Bit/Pixel) | No Change |
| RDDIM | 00h | 00h | 00h |
| RDDSM | 00h | 00h | 00h |
| RDDSDR | 00h | 00h | 00h |
| ID2 | NV value | NV value | NV value |
| ID3 | NV value | NV value | NV value |

*Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only*

### 9.14.2 Reset Table (GM[2:0]= "000", 132RGB x 162)

| Item | After Power On | After H/W Reset | After S/W Reset |
|---|---|---|---|
| Frame memory | Random | No Change | No Change |
| Sleep In/Out | In | In | In |
| Display On/Off | Off | Off | Off |
| Display mode (normal/partial) | Normal | Normal | Normal |
| Display Inversion On/Off | Off | Off | Off |
| Display Idle Mode On/Off | Off | Off | Off |
| Column: Start Address (XS) | 0000h | 0000h | 0000h |
| Column: End Address (XE) | 0083h | 0083h | 0083h (131d) (when MV=0) 00A1h (161d) (when MV=1) |
| Row: Start Address (YS) | 0000h | 0000h | 0000h |
| Row: End Address (YE) | 00A1h | 00A1h | 00A1h (161d) (when MV=0) 0083h (131d) (when MV=1) |
| Gamma setting | GC0 | GC0 | GC0 |
| RGB for 4k and 65k Color Mode | See Section 9.17 | See Section 9.17 | No Change |
| Partial: Start Address (PSL) | 0000h | 0000h | 0000h |
| Partial: End Address (PEL) | 00A1h | 00A1h | 00A1h |
| Tearing: On/Off | Off | Off | Off |
| Tearing Effect Mode (*1) | 0 (Mode1) | 0 (Mode1) | 0 (Mode1) |
| Memory Data Access Control (MY/MX/MV/ML/RGB) | 0/0/0/0/0 | 0/0/0/0/0 | No Change |
| Interface Pixel Color Format | 6 (18-Bit/Pixel) | 6 (18-Bit/Pixel) | No Change |
| RDDPM | 08h | 08h | 08h |
| RDDMADCTL | 00h | 00h | No Change |
| RDDCOLMOD | 6 (18-Bit/Pixel) | 6 (18-Bit/Pixel) | No Change |
| RDDIM | 00h | 00h | 00h |
| RDDSM | 00h | 00h | 00h |
| RDDSDR | 00h | 00h | 00h |
| ID2 | NV value | NV value | NV value |
| ID3 | NV value | NV value | NV value |

*Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only*

### 9.15 Module Input/Output Pins

### 9.15.1  Output or Bi-directional (I/O) Pins

| Output or Bi-directional pins | After Power On | After Hardware Reset | After Software Reset |
|---|---|---|---|
| TE | Low | Low | Low |
| D7 to D0 (Output driver) | High-Z (Inactive) | High-Z (Inactive) | High-Z (Inactive) |

| Input pins | During Power On Process | After Power On | After Hardware Reset | After Software Reset | During Power Off Process |
|---|---|---|---|---|---|
| RESX | See 9.14 | Input valid | Input valid | Input valid | See 9.14 |
| CSX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| D/CX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| WRX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| RDX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| D7 to D0 | Input invalid | Input valid | Input valid | Input valid | Input invalid |

*Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.*

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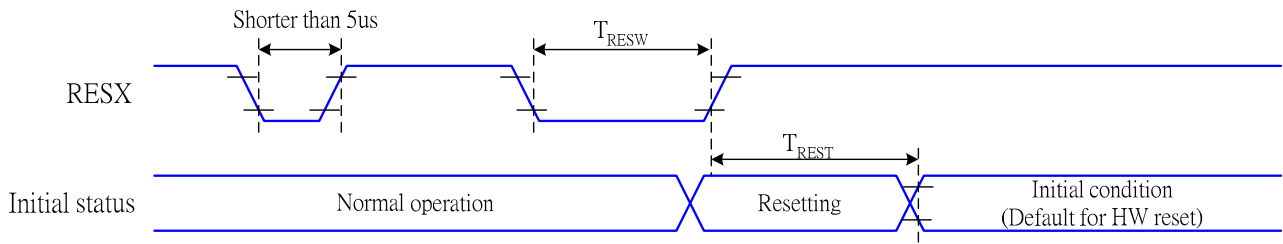
**9.16 Reset Timing**



Table 9.16.1 Reset timing

| Related Pins | Symbol | Parameter | MIN | MAX | Unit |
|---|---|---|---|---|---|
| RESX | tRESW | Reset pulse duration | 10 | - | us |
| | tREST | Reset cancel | - | 5 | ms |
| | | | | 120 | ms |

Notes:
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:
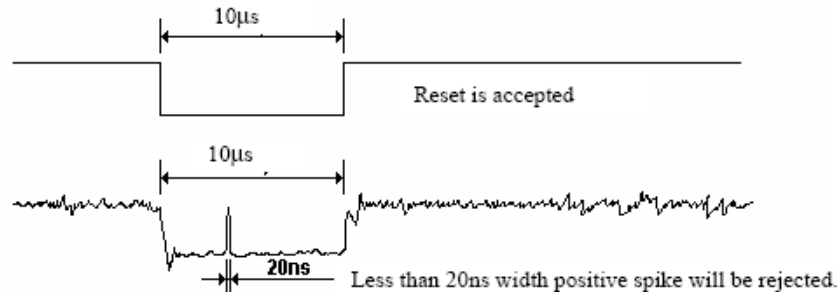


5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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### 9.17 Color Depth Conversion Look Up Tables

### 9.17.1 65536 Color to 262,144 Color

| Color | Look Up Table Output Frame Memory Data (6-bits) | Default value after H/W Reset | RGBSET Parameter | Look Up Table Input Data 65k Color (5-bits) |
|---|---|---|---|---|
| RED | R005 R004 R003 R002 R001 R000 | 000000 | 1 | 00000 |
| | R015 R014 R013 R012 R011 R010 | 000010 | 2 | 00001 |
| | R025 R024 R023 R022 R021 R020 | 000100 | 3 | 00010 |
| | R035 R034 R033 R032 R031 R030 | 000110 | 4 | 00011 |
| | R045 R044 R043 R042 R041 R040 | 001000 | 5 | 00100 |
| | R055 R054 R053 R052 R051 R050 | 001010 | 6 | 00101 |
| | R065 R064 R063 R062 R061 R060 | 001100 | 7 | 00110 |
| | R075 R074 R073 R072 R071 R070 | 001110 | 8 | 00111 |
| | R085 R084 R083 R082 R081 R080 | 010000 | 9 | 01000 |
| | R095 R094 R093 R092 R091 R090 | 010010 | 10 | 01001 |
| | R105 R104 R103 R102 R101 R100 | 010100 | 11 | 01010 |
| | R115 R114 R113 R112 R111 R110 | 010110 | 12 | 01011 |
| | R125 R124 R123 R122 R121 R120 | 011000 | 13 | 01100 |
| | R135 R134 R133 R132 R131 R130 | 011010 | 14 | 01101 |
| | R145 R144 R143 R142 R141 R140 | 011100 | 15 | 01110 |
| | R155 R154 R153 R152 R151 R150 | 011110 | 16 | 01111 |
| | R165 R164 R163 R162 R161 R160 | 100001 | 17 | 10000 |
| | R175 R174 R173 R172 R171 R170 | 100011 | 18 | 10001 |
| | R185 R184 R183 R182 R181 R180 | 100101 | 19 | 10010 |
| | R195 R194 R193 R192 R191 R190 | 100111 | 20 | 10011 |
| | R205 R204 R203 R202 R201 R200 | 101001 | 21 | 10100 |
| | R215 R214 R213 R212 R211 R210 | 101011 | 22 | 10101 |
| | R225 R224 R223 R222 R221 R220 | 101101 | 23 | 10110 |
| | R235 R234 R233 R232 R231 R230 | 101111 | 24 | 10111 |
| | R245 R244 R243 R242 R241 R240 | 110001 | 25 | 11000 |
| | R255 R254 R253 R252 R251 R250 | 110011 | 26 | 11001 |
| | R265 R264 R263 R262 R261 R260 | 110101 | 27 | 11010 |
| | R275 R274 R273 R272 R271 R270 | 110111 | 28 | 11011 |
| | R285 R284 R283 R282 R281 R280 | 111001 | 29 | 11100 |
| | R295 R294 R293 R292 R291 R290 | 111011 | 30 | 11101 |
| | R305 R304 R303 R302 R301 R300 | 111101 | 31 | 11110 |
| | R315 R314 R313 R312 R311 R310 | 111111 | 32 | 11111 |

| Color | Look Up Table Output Frame Memory Data (6-bits) | Default value after H/W Reset | RGBSET Parameter | Look Up Table Input Data 65k Color (5-bits) |
|---|---|---|---|---|
| GREEN | G005 G004 G003 G002 G001 G000 | 000000 | 33 | 000000 |
| | G015 G014 G013 G012 G011 G010 | 000001 | 34 | 000001 |
| | G025 G024 G023 G022 G021 G020 | 000010 | 35 | 000010 |
| | G035 G034 G033 G032 G031 G030 | 000011 | 36 | 000011 |
| | G045 G044 G043 G042 G041 G040 | 000100 | 37 | 000100 |
| | G055 G054 G053 G052 G051 G050 | 000101 | 38 | 000101 |
| | G065 G064 G063 G062 G061 G060 | 000110 | 39 | 000110 |
| | G075 G074 G073 G072 G071 G070 | 000111 | 40 | 000111 |
| | G085 G084 G083 G082 G081 G080 | 001000 | 41 | 001000 |
| | G095 G094 G093 G092 G091 G090 | 001001 | 42 | 001001 |
| | G105 G104 G103 G102 G101 G100 | 001010 | 43 | 001010 |
| | G115 G114 G113 G112 G111 G110 | 001011 | 44 | 001011 |
| | G125 G124 G123 G122 G121 G120 | 001100 | 45 | 001100 |
| | G135 G134 G133 G132 G131 G130 | 001101 | 46 | 001101 |
| | G145 G144 G143 G142 G141 G140 | 001110 | 47 | 001110 |
| | G155 G154 G153 G152 G151 G150 | 001111 | 48 | 001111 |
| | G165 G164 G163 G162 G161 G160 | 010000 | 49 | 010000 |
| | G175 G174 G173 G172 G171 G170 | 010001 | 50 | 010001 |
| | G185 G184 G183 G182 G181 G180 | 010010 | 51 | 010010 |
| | G195 G194 G193 G192 G191 G190 | 010011 | 52 | 010011 |
| | G205 G204 G203 G202 G201 G200 | 010100 | 53 | 010100 |

| | | | | |
|---|---|---|---|---|
| G215 G214 G213 G212 G211 G210 | 010101 | 54 | 010101 | |
| G225 G224 G223 G222 G221 G220 | 010110 | 55 | 010110 | |
| G235 G234 G233 G232 G231 G230 | 010111 | 56 | 010111 | |
| G245 G244 G243 G242 G241 G240 | 011000 | 57 | 011000 | |
| G255 G254 G253 G252 G251 G250 | 011001 | 58 | 011001 | |
| G265 G264 G263 G262 G261 G260 | 011010 | 59 | 011010 | |
| G275 G 274 G273 G272 G271 G270 | 011011 | 60 | 011011 | |
| G285 G 284 G283 G282 G281 G280 | 011100 | 61 | 011100 | |
| G295 G 294 G293 G292 G291 G290 | 011101 | 62 | 011101 | |
| G305 G 304 G303 G302 G301 G300 | 011110 | 63 | 011110 | |
| G315 G 314 G313 G312 G311 G310 | 011111 | 64 | 011111 | |
| G325 G324 G323 G322 G321 G320 | 100000 | 65 | 100000 | |
| G335 G334 G333 G332 G331 G330 | 100001 | 66 | 100001 | |
| G345 G344 G343 G342 G341 G340 | 100010 | 67 | 100010 | |
| G355 G354 G353 G352 G351 G350 | 100011 | 68 | 100011 | |
| G365 G364 G363 G362 G361 G360 | 100100 | 69 | 100100 | |
| G375 G374 G373 G372 G371 G370 | 100101 | 70 | 100101 | |
| G385 G384 G383 G382 G381 G380 | 100110 | 71 | 100110 | |
| G395 G394 G393 G392 G391 G390 | 100111 | 72 | 100111 | |
| G405 G404 G403 G402 G401 G400 | 101000 | 73 | 101000 | |
| G415 G414 G413 G412 G411 G410 | 101001 | 74 | 101001 | |
| G425 G424 G423 G422 G421 G420 | 101010 | 75 | 101010 | |
| G435 G434 G433 G432 G431 G430 | 101011 | 76 | 101011 | |
| G445 G444 G443 G442 G441 G440 | 101100 | 77 | 101100 | |
| G455 G454 G453 G452 G451 G450 | 101101 | 78 | 101101 | |
| G465 G464 G463 G462 G461 G460 | 101110 | 79 | 101110 | |
| G475 G474 G473 G472 G471 G470 | 101111 | 80 | 101111 | |
| G485 G484 G483 G482 G481 G480 | 110000 | 81 | 110000 | |
| G495 G494 G493 G492 G491 G490 | 110001 | 82 | 110001 | |
| G505 G504 G503 G502 G501 G500 | 110010 | 83 | 110010 | |
| G515 G514 G513 G512 G511 G510 | 110011 | 84 | 110011 | |
| G525 G524 G523 G522 G521 G520 | 110100 | 85 | 110100 | |
| G535 G534 G533 G532 G531 G530 | 110101 | 86 | 110101 | |
| G545 G544 G543 G542 G541 G540 | 110110 | 87 | 110110 | |
| G555 G554 G553 G552 G551 G550 | 110111 | 88 | 110111 | |
| G565 G564 G563 G562 G561 G560 | 111000 | 89 | 111000 | |
| G575 G574 G573 G572 G571 G570 | 111001 | 90 | 111001 | |
| G585 G584 G583 G582 G581 G580 | 111010 | 91 | 111010 | |
| G595 G594 G593 G592 G591 G590 | 111011 | 92 | 111011 | |
| G605 G604 G603 G602 G601 G600 | 111100 | 93 | 111100 | |
| G615 G614 G613 G612 G611 G610 | 111101 | 94 | 111101 | |
| G625 G624 G623 G622 G621 G620 | 111110 | 95 | 111110 | |
| G635 G634 G633 G632 G631 G630 | 111111 | 96 | 111111 | |

| Color | Look Up Table Output Frame Memory Data (6-bits) | Default value after H/W Reset | RGBSET Parameter | Look Up Table Input Data 65k Color (5-bits) |
|---|---|---|---|---|
| BLUE | B005 B004 B003 B002 B001 B000 | 000000 | 97 | 00000 |
| | B015 B014 B013 B012 B011 B010 | 000010 | 98 | 00001 |
| | B025 B024 B023 B022 B021 B020 | 000100 | 99 | 00010 |
| | B035 B034 B033 B032 B031 B030 | 000110 | 100 | 00011 |
| | B045 B044 B043 B042 B041 B040 | 001000 | 101 | 00100 |
| | B055 B054 B053 B052 B051 B050 | 001010 | 102 | 00101 |
| | B065 B064 B063 B062 B061 B060 | 001100 | 103 | 00110 |
| | B075 B074 B073 B072 B071 B070 | 001110 | 104 | 00111 |
| | B085 B084 B083 B082 B081 B080 | 010000 | 105 | 01000 |
| | B095 B094 B093 B092 B091 B090 | 010010 | 106 | 01001 |
| | B105 B104 B103 B102 B101 B100 | 010100 | 107 | 01010 |
| | B115 B114 B113 B112 B111 B110 | 010110 | 108 | 01011 |
| | B125 B124 B123 B122 B121 B120 | 011000 | 109 | 01100 |
| | B135 B134 B133 B132 B131 B130 | 011010 | 110 | 01101 |
| | B145 B144 B143 B142 B141 B140 | 011100 | 111 | 01110 |
| | B155 B154 B153 B152 B151 B150 | 011110 | 112 | 01111 |
| | B165 B164 B163 B162 B161 B160 | 100001 | 113 | 10000 |

| | B175 B174 B173 B172 B171 B170 | 100011 | 114 | 10001 |
| --- | --- | --- | --- | --- |
| | B185 B184 B183 B182 B181 B180 | 100101 | 115 | 10010 |
| | B195 B194 B193 B192 B191 B190 | 100111 | 116 | 10011 |
| | B205 B204 B203 B202 B201 B200 | 101001 | 117 | 10100 |
| | B215 B214 B213 B212 B211 B210 | 101011 | 118 | 10101 |
| | B225 B224 B223 B222 B221 B220 | 101101 | 119 | 10110 |
| | B235 B234 B233 B232 B231 B230 | 101111 | 120 | 10111 |
| | B245 B244 B243 B242 B241 B240 | 110001 | 121 | 11000 |
| | B255 B254 B253 B252 B251 B250 | 110011 | 122 | 11001 |
| | B265 B264 B263 B262 B261 B260 | 110101 | 123 | 11010 |
| | B275 B274 B273 B272 B271 B270 | 110111 | 124 | 11011 |
| | B285 B284 B283 B282 B281 B280 | 111001 | 125 | 11100 |
| | B295 B294 B293 B292 B291 B290 | 111011 | 126 | 11101 |
| | B305 B304 B303 B302 B301 B300 | 111101 | 127 | 11110 |
| | B315 B314 B313 B312 B311 B310 | 111111 | 128 | 11111 |

### 9.17.2 4096 Color to 262,144 Color

| Color | Look Up Table Output Frame Memory Data (6-bits) | Default value after H/W Reset | RGBSET Parameter | Look Up Table Input Data 4k Color (4-bits) |
|---|---|---|---|---|
| RED | R005 R004 R003 R002 R001 R000 | 000000 | 1 | 0000 |
| | R015 R014 R013 R012 R011 R010 | 000100 | 2 | 0001 |
| | R025 R024 R023 R022 R021 R020 | 001000 | 3 | 0010 |
| | R035 R034 R033 R032 R031 R030 | 001100 | 4 | 0011 |
| | R045 R044 R043 R042 R041 R040 | 010001 | 5 | 0100 |
| | R055 R054 R053 R052 R051 R050 | 010101 | 6 | 0101 |
| | R065 R064 R063 R062 R061 R060 | 011001 | 7 | 0110 |
| | R075 R074 R073 R072 R071 R070 | 011101 | 8 | 0111 |
| | R085 R084 R083 R082 R081 R080 | 100010 | 9 | 1000 |
| | R095 R094 R093 R092 R091 R090 | 100110 | 10 | 1001 |
| | R105 R104 R103 R102 R101 R100 | 101010 | 11 | 1010 |
| | R115 R114 R113 R112 R111 R110 | 101110 | 12 | 1011 |
| | R125 R124 R123 R122 R121 R120 | 110011 | 13 | 1100 |
| | R135 R134 R133 R132 R131 R130 | 110111 | 14 | 1101 |
| | R145 R144 R143 R142 R141 R140 | 111011 | 15 | 1110 |
| | R155 R154 R153 R152 R151 R150 | 111111 | 16 | 1111 |
| | R165 R164 R163 R162 R161 R160 | ------ | 17 | Not used |
| | \| | \| | \| | |
| | R315 R314 R313 R312 R311 R310 | ------ | 32 | |
| GREEN | G005 G004 G003 G002 G001 G000 | 000000 | 33 | 0000 |
| | G015 G014 G013 G012 G011 G010 | 000100 | 34 | 0001 |
| | G025 G024 G023 G022 G021 G020 | 001000 | 35 | 0010 |
| | G035 G034 G033 G032 G031 G030 | 001100 | 36 | 0011 |
| | G045 G044 G043 G042 G041 G040 | 010001 | 37 | 0100 |
| | G055 G054 G053 G052 G051 G050 | 010101 | 38 | 0101 |
| | G065 G064 G063 G062 G061 G060 | 011001 | 39 | 0110 |
| | G075 G074 G073 G072 G071 G070 | 011101 | 40 | 0111 |
| | G085 G084 G083 G082 G081 G080 | 100010 | 41 | 1000 |
| | G095 G094 G093 G092 G091 G090 | 100110 | 42 | 1001 |
| | G105 G104 G103 G102 G101 G100 | 101010 | 43 | 1010 |
| | G115 G114 G113 G112 G111 G110 | 101110 | 44 | 1011 |
| | G125 G124 G123 G122 G121 G120 | 110011 | 45 | 1100 |
| | G135 G134 G133 G132 G131 G130 | 110111 | 46 | 1101 |
| | G145 G144 G143 G142 G141 G140 | 111011 | 47 | 1110 |
| | G155 G154 G153 G152 G151 G150 | 111111 | 48 | 1111 |
| | G165 G164 G163 G162 G161 G160 | ------ | 49 | Not used |
| | \| | \| | \| | |
| | G635 G634 G633 G632 G631 G630 | ------ | 96 | |
| BLUE | B005 B004 B003 B002 B001 B000 | 000000 | 97 | 0000 |
| | B015 B014 B013 B012 B011 B010 | 000100 | 98 | 0001 |
| | B025 B024 B023 B022 B021 B020 | 001000 | 99 | 0010 |
| | B035 B034 B033 B032 B031 B030 | 001100 | 100 | 0011 |
| | B045 B044 B043 B042 B041 B040 | 010001 | 101 | 0100 |
| | B055 B054 B053 B052 B051 B050 | 010101 | 102 | 0101 |
| | B065 B064 B063 B062 B061 B060 | 011001 | 103 | 0110 |
| | B075 B074 B073 B072 B071 B070 | 011101 | 104 | 0111 |
| | B085 B084 B083 B082 B081 B080 | 100010 | 105 | 1000 |
| | B095 B094 B093 B092 B091 B090 | 100110 | 106 | 1001 |
| | B105 B104 B103 B102 B101 B100 | 101010 | 107 | 1010 |
| | B115 B114 B113 B112 B111 B110 | 101110 | 108 | 1011 |
| | B125 B124 B123 B122 B121 B120 | 110011 | 109 | 1100 |
| | B135 B134 B133 B132 B131 B130 | 110111 | 110 | 1101 |
| | B145 B144 B143 B142 B141 B140 | 111011 | 111 | 1110 |
| | B155 B154 B153 B152 B151 B150 | 111111 | 112 | 1111 |
| | B165 B164 B163 B162 B161 B160 | ------ | 113 | Not used |
| | \| | \| | \| | |
| | B315 B314 B313 B312 B311 B310 | ------ | 128 | |

## 10 Command

### 10.1 System function Command List and Description

Table 10.1.1 System Function command List (1)

| Instruction | Refer | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NOP | 10.1.1 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (00h) | No Operation |
| SWRESET | 10.1.2 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (01h) | Software reset |
| RDDID | 10.1.3 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (04h) | Read Display ID |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 |  | ID1 read |
|  |  | 1 | 1 | ↑ | - | 1 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 |  | ID2 read |
|  |  | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 |  | ID3 read |
| RDDST | 10.1.4 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | (09h) | Read Display Status |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | BSTON | MY | MX | MV | ML | RGB | MH | ST24 |  | - |
|  |  | 1 | 1 | ↑ | - | ST23 | IFPF2 | IFPF1 | IFPF0 | IDMON | PTLON | SLOUT | NORON |  | - |
|  |  | 1 | 1 | ↑ | - | VSSON | ST14 | INVON | ST12 | ST11 | DISON | TEON | GCS2 |  | - |
|  |  | 1 | 1 | ↑ | - | GCS1 | GCS0 | TELOM | ST4 | ST3 | ST2 | ST1 | ST0 |  | - |
| RDDPM | 10.1.5 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | (0Ah) | Read Display Power |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | BSTON | IDMON | PTLON | SLPOUT | NORON | DISON | - | - |  | - |
| RDD MADCTL | 10.1.6 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | (0Bh) | Read Display |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | MY | MX | MV | ML | RGB | MH | - | - |  | - |
| RDD COLMOD | 10.1.7 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | (0Ch) | Read Display Pixel |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | 0 | 0 | 0 | 0 | - | IFPF2 | IFPF1 | IFPF0 |  | - |
| RDDIM | 10.1.8 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | (0Dh) | Read Display Image |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | VSSON | D6 | INVON | - | - | GCS2 | GCS1 | GCS0 |  | - |
| RDDSM | 10.1.9 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | (0Eh) | Read Display Signal |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | TEON | TELOM | - | - | - | - | - | - |  | - |

"-": Don't care

# ST7735

Table 10.1.2 System Function command List (2)

| Instruction | Refer | D/C | WR | RDX | D17- | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SLPIN | 10.1.10 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | (10h) | Sleep in & booster off |
| SLPOUT | 10.1.11 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | (11h) | Sleep out & booster on |
| PTLON | 10.1.12 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | (12h) | Partial mode on |
| NORON | 10.1.13 | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | (13h) | Partial off (Normal) |
| INVOFF | 10.1.14 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | (20h) | Display inversion off |
| INVON | 10.1.15 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | (21h) | Display inversion on |
| GAMSET | 10.1.16 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | (26h) | Gamma curve select |
|  |  | 1 | ↑ | 1 | - | - | - | - | - | GC3 | GC2 | GC1 | GC0 |  | - |
| DISPOFF | 10.1.17 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | (28h) | Display off |
| DISPON | 10.1.18 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | (29h) | Display on |
| CASET | 10.1.19 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | (2Ah) | Column address set |
|  |  | 1 | ↑ | 1 | - | XS15 | XS14 | XS13 | XS12 | XS11 | XS10 | XS9 | XS8 |  | X address start: 0≦XS≦X |
|  |  | 1 | ↑ | 1 | - | XS7 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 |  |  |
|  |  | 1 | ↑ | 1 | - | XE15 | XE14 | XE13 | XE12 | XE11 | XE10 | XE9 | XE8 |  | X address end: S≦XE≦X |
|  |  | 1 | ↑ | 1 | - | XE7 | XE6 | XE5 | XE4 | XE3 | XE2 | XE1 | XE0 |  |  |
| RASET | 10.1.20 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | (2Bh) | Row address set |
|  |  | 1 | ↑ | 1 | - | YS15 | YS14 | YS13 | YS12 | YS11 | YS10 | YS9 | YS8 |  | Y address start: 0≦YS≦Y |
|  |  | 1 | ↑ | 1 | - | YS7 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 |  |  |
|  |  | 1 | ↑ | 1 | - | YE15 | YE14 | YE13 | YE12 | YE11 | YE10 | YE9 | YE8 |  | Y address end:S≦YE≦Y |
|  |  | 1 | ↑ | 1 | - | YE7 | YE6 | YE5 | YE4 | YE3 | YE2 | YE1 | YE0 |  |  |
| RAMWR | 10.1.21 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | (2Ch) | Memory write |
|  |  | 1 | ↑ | 1 | - | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |  | Write data |
| RAMRD | 10.1.22 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | (2Eh) | Memory read |
|  |  | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |  | Dummy read |
|  |  | 1 | 1 | ↑ | - | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |  | Read data |

"-": Don't care

Table 10.1.3 System Function command List (3)

| Instruction | Refer | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLAR | 10.1.23 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | (30h) | Partial start/end address set |
| | | 1 | ↑ | 1 | - | PSL15 | PSL14 | PSL13 | PSL12 | PSL11 | PSL10 | PSL9 | PSL8 | | Partial start address (0,1,2, ..P) |
| | | 1 | ↑ | 1 | - | PSL7 | PSL6 | PSL5 | PSL4 | PSL3 | PSL2 | PSL1 | PSL0 | | |
| | | 1 | ↑ | 1 | - | PEL15 | PEL14 | PEL13 | PEL12 | PEL11 | PEL10 | PEL9 | PEL8 | | Partial end address (0,1,2, .., P) |
| | | 1 | ↑ | 1 | - | PEL7 | PEL6 | PEL5 | PEL4 | PEL3 | PEL2 | PEL1 | PEL0 | | |
| TEOFF | 10.1.24 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (34h) | Tearing effect line off |
| TEON | 10.1.25 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | (35h) | Tearing effect mode set & on |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | TELOM | | Mode1: TELOM="0" Mode2: TELOM="1" |
| MADCTL | 10.1.26 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (36h) | Memory data access control |
| | | 1 | ↑ | 1 | - | MY | MX | MV | ML | RGB | MH | - | - | | - |
| IDMOFF | 10.1.27 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | (38h) | Idle mode off |
| IDMON | 10.1.28 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | (39h) | Idle mode on |
| COLMOD | 10.1.29 | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | (3Ah) | Interface pixel format |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | IFPF2 | IFPF1 | IFPF0 | | Interface format |
| RDID1 | 10.1.30 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | (DAh) | Read ID1 |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | | Read parameter |
| RDID2 | 10.1.31 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | (DBh) | Read ID2 |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | | 1 | 1 | ↑ | - | 1 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | | Read parameter |
| RDID3 | 10.1.32 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | (DCh) | Read ID3 |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | | Read parameter |

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DA to F are for factory use of driver supplier.

Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).

# ST7735

## 10.1.1 NOP (00h)

| 00H | NOP (No Operation) | | | | | | | | | | | | |
|-----|------|-----|-----|-------|----|----|----|----|----|----|----|----|-----|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| NOP | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (00h) |
| Parameter | No Parameter | | | | | | | | | | | | - |
| Description | This command is empty command. | | | | | | | | | | | | |

"-" Don't care

# *ST7735*

## 10.1.2 SWRESET (01h): Software Reset

| 01H | SWRESET (Software Reset) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| SWRESET | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (01h) |
| Parameter | No Parameter | | | | | | | | | | | - |
| Description | "-" Don't care<br><br>-If Software Reset is applied during Sleep In mode, it will be necessary to wait 120msec before sending next command.<br><br>-The display module loads all default values to the registers during 120msec.<br><br>-If Software Reset is applied during Sleep Out or Display On Mode, it will be necessary to wait 120msec before sending next command. | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | |



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### 10.1.3 RDDID (04h): Read Display ID

| 04H | | | | | | RDDID (Read Display ID) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDDID | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (04h) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | |
| 3rd parameter | 1 | 1 | ↑ | - | 1 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | |
| 4th parameter | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | |

| | |
|---|---|
| Description | -This read byte returns 24-bit display identification information.<br><br>-The 1st parameter is dummy data<br><br>-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.<br><br>-The 3rd parameter (ID26 to ID20): LCD module/driver version ID<br><br>-The 4th parameter (ID37 to UD30): LCD module/driver ID.<br><br>-Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.<br><br>"-" Don't care |

| | |
|---|---|
| Default | |

| Status | Default Value | | |
|---|---|---|---|
| | ID1 | ID2 | ID3 |
| Power On Sequence | - | NV Value | NV Value |
| S/W Reset | - | NV Value | NV Value |
| H/W Reset | - | NV Value | NV Value |

Flow Chart

# ST7735

### 10.1.4 RDDST (09h): Read Display Status

| 09H | | | | | RDDST (Read Display Status) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDDST | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | (09h) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | BSTON | MY | MX | MV | ML | RGB | MH | ST24 | |
| 3rd parameter | 1 | 1 | ↑ | - | ST23 | IFPF2 | IFPF1 | IFPF0 | IDMON | PTLON | SLOUT | NORON | |
| 4th parameter | 1 | 1 | ↑ | - | ST15 | ST14 | INVON | ST12 | ST11 | DISON | TEON | GCS2 | |
| 5th parameter | 1 | 1 | ↑ | - | GCS1 | GCS0 | TELOM | ST4 | ST3 | ST2 | ST1 | ST0 | |

| Description | This command indicates the current status of the display as described in the table below: |

| Bit | Description | Value |
|---|---|---|
| BSTON | Booster Voltage Status | '1' =Booster on, '0' =Booster off |
| MY | Row Address Order (MY) | '1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0') |
| MX | Column Address Order (MX) | '1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1') |
| MV | Row/Column Exchange (MV) | '1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0' |
| ML | Scan Address Order (ML) | '0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1') |
| RGB | RGB/ BGR Order (RGB) | '1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0') |
| MH | Horizontal Order | '0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1') |
| ST24 | For Future Use | '0' |
| ST23 | For Future Use | '0' |
| IFPF2 | Interface Color Pixel Format Definition | "011" = 12-bit / pixel, |
| IFPF1 | | "101" = 16-bit / pixel, |
| IFPF0 | | "110" = 18-bit / pixel, others are no define |
| IDMON | Idle Mode On/Off | '1' = On, "0" = Off |
| PTLON | Partial Mode On/Off | '1' = On, "0" = Off |
| SLPOUT | Sleep In/Out | '1' = Out, "0" = In |
| NORON | Display Normal Mode On/Off | '1' = Normal Display, '0' = Partial Display |
| ST15 | Vertical Scrolling Status (Not Used) | '1' = Scroll on,"0" = Scroll off |
| ST14 | Horizontal Scroll Status (Not Used) | '0' |
| INVON | Inversion Status | '1' = On, "0" = Off |
| ST12 | All Pixels On (Not Used) | '0' |

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| | | | |
|---|---|---|---|
| DISON | Display On/Off | '1' = On, "0" = Off | |
| TEON | Tearing effect line on/off | '1' = On, "0" = Off | |
| GCSEL2 | | "000" = GC0 | |
| GCSEL1 | | "001" = GC1 | |
| | Gamma Curve Selection | "010" = GC2 | |
| GCSEL0 | | "011" = GC3 | |
| | | "100" to "111" = Not defined | |
| TELOM | Tearing effect line mode | '0' = mode1, '1' = mode2 | |
| ST4 | For Future Use | '0' | |
| ST3 | For Future Use | '0' | |
| ST2 | For Future Use | '0' | |
| ST1 | For Future Use | '0' | |
| ST0 | For Future Use | '0' | |

"-" Don't care

**Default**

| Status | Default Value (ST31 to ST0) | | | |
|---|---|---|---|---|
| | ST[31-24] | ST[23-16] | ST[15-8] | ST[7-0] |
| Power On Sequence | 0000-0000 | 0110-0001 | 0000-0000 | 0000-0000 |
| S/W Reset | 0xxx0xx00 | 0xxx-0001 | 0000-0000 | 0000-0000 |
| H/W Reset | 0000-0000 | 0110-0001 | 0000-0000 | 0000-0000 |

**Flow Chart**

# *ST7735*

## 10.1.5  RDDPM (0Ah): Read Display Power Mode

| 0AH | RDDPM (Read Display Power Mode) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDDPM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | (0Ah) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | | BSTON | IDMON | PTLON | SLPOUT | NORON | DISON | D1 | D0 | |

This command indicates the current status of the display as described in the table below:

"-" Don't care

<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>BSTON</td><td>Booster Voltage Status</td><td>'1' =Booster on,<br>'0' =Booster off</td></tr>
<tr><td>IDMON</td><td>Idle Mode On/Off</td><td>'1' = Idle Mode On,<br>'0' = Idle Mode Off</td></tr>
<tr><td>PTLON</td><td>Partial Mode On/Off</td><td>'1' = Partial Mode On,<br>'0' = Partial Mode Off</td></tr>
<tr><td>SLPON</td><td>Sleep In/Out</td><td>'1' = Sleep Out,<br>'0' = Sleep In</td></tr>
<tr><td>NORON</td><td>Display Normal ModemOn/Off</td><td>'1' = Normal Display,<br>'0' = Partial Display</td></tr>
<tr><td>DISON</td><td>Display On/Off</td><td>'1' = Display On,<br>'0' = Display Off</td></tr>
<tr><td>D1</td><td>Not Used</td><td>'0'</td></tr>
<tr><td>D0</td><td>Not Used</td><td>'0'</td></tr>
</table>

**Description**

**Default**

| Status | Default Value (D7 to D0) |
|---|---|
| Power On Sequence | 0000_1000(08h) |
| S/W Reset | 0000_1000(08h) |
| H/W Reset | 0000_1000(08h) |

**Flow Chart**

# ST7735
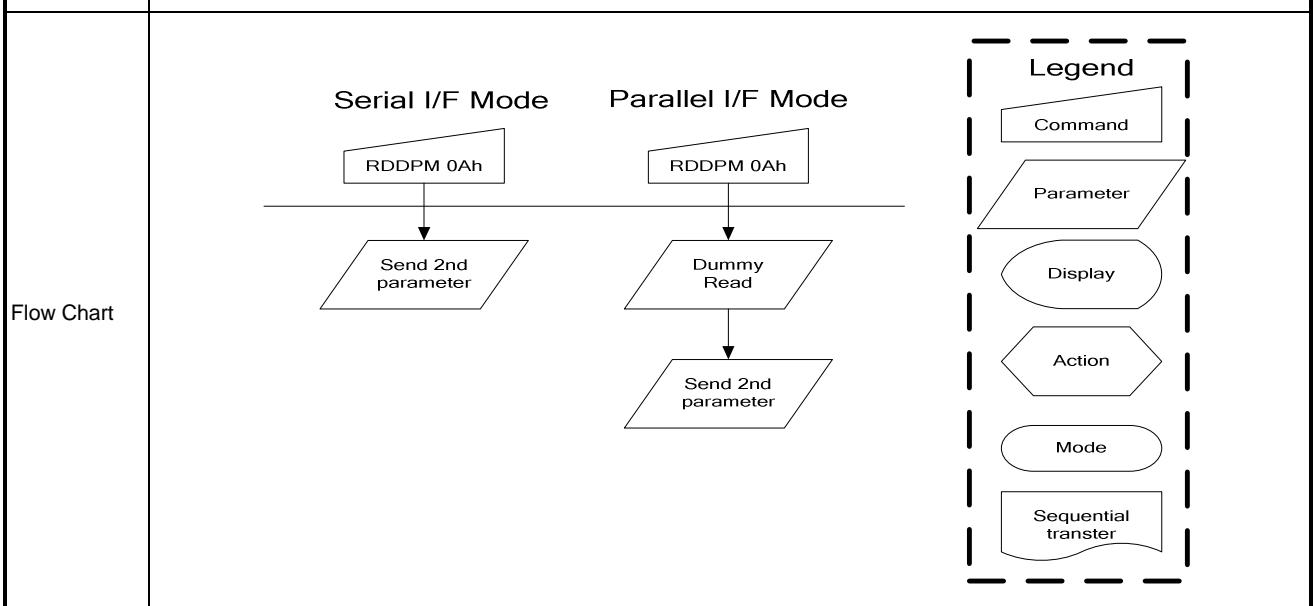
## 10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

| 0BH | | | | RDDMADCTL (Read Display MADCTL) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDDMADCTL | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | (0Bh) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | | MY | MX | MV | ML | RGB | MH | D1 | D0 | |

**Description**

This command indicates the current status of the display as described in the table below:

"-" Don't care

| Bit | Description | Value |
|---|---|---|
| MX | Column Address Order | '1' = Right to Left (When MADCTL B6='1')<br>'0' = Left to Right (When MADCTL B6='0') |
| MY | Row Address Order | '1' = Bottom to Top (When MADCTL B7='1')<br>'0' = Top to Bottom (When MADCTL B7='0') |
| MV | Row/Column Order (MV) | '1' = Row/column exchange (MV=1)<br>'0' = Normal (MV=0) |
| ML | Vertical Refresh Order | '1' =LCD Refresh Bottom to Top<br>'0' =LCD Refresh Top to Bottom |
| RGB | RGB/BGR Order | '1' =BGR, "0"=RGB |
| MH | Horizontal Refresh Order | LCD horizontal refresh direction control<br>'0' = LCD horizontal refresh Left to right<br>'1' = LCD horizontal refresh right to left |
| D1 | Not Used | '0' |
| D0 | Not Used | '0' |

**Default**

| Status | Default Value (D7 to D0) |
|---|---|
| Power On Sequence | 0000_0000 (00h) |
| S/W Reset | No change |
| H/W Reset | 0000_0000 (00h) |

**Flow Chart**

# *ST7735*
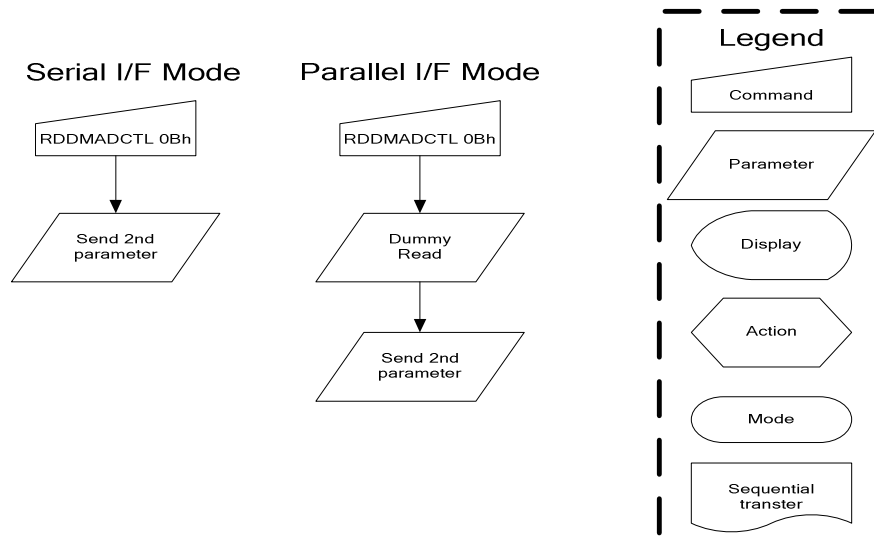
## 10.1.7  RDDCOLMOD (0Ch): Read Display Pixel Format

| 0CH | RDDCOLMOD (Read Display Pixel Format) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDDCOLMOD | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | (0Ch) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | 0 | 0 | 0 | 0 | - | IFPF2 | IFPF1 | IFPF0 | |

| Description | This command indicates the current status of the display as described in the table below: |
|---|---|
| | <table><tr><td>IFPF[2:0]</td><td>MCU Interface Color Format</td></tr><tr><td>011</td><td>12-bit/pixel</td></tr><tr><td>101</td><td>16-bit/pixel</td></tr><tr><td>110</td><td>18-bit/pixel</td></tr><tr><td>111</td><td>No used</td></tr></table><br>Others are no define and invalid<br><br>"-" Don't care |

| Default | <table><tr><td>Status</td><td>Default Value</td></tr><tr><td></td><td>IFPF[2:0]</td></tr><tr><td>Power On Sequence</td><td>0110 (18 bits/pixel)</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>0110 (18 bits/pixel)</td></tr></table> |
|---|---|

| Flow Chart |  |
|---|---|

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## 10.1.8 RDDIM (0Dh): Read Display Image Mode

| 0DH | RDDIM (0Dh): Read Display Image Mode | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDDIM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | (0Dh) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | | VSSON | D6 | INVON | D4 | D3 | GCS2 | GCS1 | GCS0 | |

| | This command indicates the current status of the display as described in the table below:<br><br>"-" Don't care |
|---|---|
| Description | | Bit | Description | Value |
| | |---|---|---|
| | | VSSON | Reversed | "0" |
| | | D6 | Reversed | "0" |
| | | INVON | Inversion On/Off | "1" = Inversion is On,<br>"0" = Inversion is Off |
| | | D4 | All Pixels On | "0" (Not used) |
| | | D3 | All Pixels Off | "0" (Not used) |
| | | GCS2<br>GCS1<br>GCS0 | Gamma Curve Selection | "000" = GC0,<br>"001" = GC1,<br>"010" = GC2,<br>"011" = GC3, "100" to "111" = Not defined |

| | | Status | Default Value(D7 to D0) |
|---|---|---|---|
| Default | | Power On Sequence | 0000_0000 (00h) |
| | | S/W Reset | 0000_0000 (00h) |
| | | H/W Reset | 0000_0000 (00h) |

| | |
|---|---|
| Flow Chart | **Serial I/F Mode**    **Parallel I/F Mode**    **Legend**<br><br>RDDIM 0Dh    RDDIM 0Dh    Command<br>Host Display<br>Send 2nd parameter    Dummy Read    Parameter<br>Send 2nd parameter    Display<br>Action<br>Mode<br>Sequential transter |

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### 10.1.9  RDDSM (0Eh): Read Display Signal Mode

| 0EH | | | | | RDDSM (0Eh): Read Display Signal Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDDSM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | (0Eh) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | TEON | TELOM | D5 | D4 | D3 | D2 | D1 | D0 | |

| Description | This command indicates the current status of the display as described in the table below: |
|---|---|
| | "-" Don't care |
| | | Bit | Description | Value |
| | | TEON | Tearing Effect Line On/Off | "1" = On, "0" = Off |
| | | TELOM | Tearing effect line mode | "1" = mode2, "0" = mode1 |
| | | D5 | Not Used | "1" = On, "0" = Off |
| | | D4 | Not Used | "1" = On, "0" = Off |
| | | D3 | Not Used | "1" = On, "0" = Off |
| | | D2 | Not Used | "1" = On, "0" = Off |
| | | D1 | Not Used | "1" = On, "0" = Off |
| | | D0 | Not Used | "1" = On, "0" = Off |

| Default | Status | Default Value(D7~D0) |
|---|---|---|
| | Power On Sequence | 0000_0000 (00h) |
| | S/W Reset | 0000_0000 (00h) |
| | H/W Reset | 0000_0000 (00h) |

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| Flow Chart | Serial I/F Mode — Read RDDSM → Send 2nd parameter; Parallel I/F Mode — Read RDDSM → Dummy Read → Send 2nd parameter; Host/Display; Legend — Command, Parameter, Display, Action, Mode, Sequential transter |
| --- | --- |

# *ST7735*

**10.1.10 SLPIN (10h): Sleep In**

| 10H | SLPIN (Sleep In) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| SLPIN | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | (10h) |
| Parameter | No Parameter | | | | | | | | | | | - |
| Description | -This command causes the LCD module to enter the minimum power consumption mode.<br><br>-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. | | | | | | | | | | | |
| Restriction | -This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).<br><br>-When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits. | | | | | | | | | | | |

| Default | | |
|---|---|---|
| | **Status** | **Default Value** |
| | Power On Sequence | Sleep in mode |
| | S/W Reset | Sleep in mode |
| | H/W Reset | Sleep in mode |

| Flow Chart | |
|---|---|
| |  |

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## 10.1.11 SLPOUT (11h): Sleep Out

| 11H | SLPOUT (Sleep Out) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| SLPOUT | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | (11h) |
| Parameter | No Parameter | | | | | | | | | | | - |
| Description | -This command turns off sleep mode.<br><br>-In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started. |
| Restriction | -This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).<br><br>-When IC is in Sleep In mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.<br><br>-When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command due to the download of default value of registers and the execution of self-diagnostic function. |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Sleep in mode |
| | S/W Reset | Sleep in mode |
| | H/W Reset | Sleep in mode |

| Flow Chart | |
|---|---|

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## 10.1.12 PTLON (12h): Partial Display Mode On

| 12H | PTLON (12h): Partial Display Mode On | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PTLON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | (12h) |
| Parameter | No Parameter | | | | | | | | | | | - |
| Description | -This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)<br><br>-To leave Partial mode, the Normal Display Mode On command (13h) should be written.<br><br>"-" Don't care | | | | | | | | | | | |
| Default | <table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table> | | | | | | | | | | | |
| Flow Chart | See Partial Area (30h) | | | | | | | | | | | |

### 10.1.13 NORON (13h): Normal Display Mode On

| 13H | NORON (Normal Display Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| NORON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | (13h) |
| Parameter | No Parameter | | | | | | | | | | | | - |

| Description | -This command returns the display to normal mode.<br><br>-Normal display mode on means Partial mode off.<br><br>-Exit from NORON by the Partial mode On command (12h)<br><br>"-" Don't care |
|---|---|
| Default | <table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table> |
| Flow Chart | See Partial Area Definition Descriptions for details of when to use this command |

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### 10.1.14 INVOFF (20h): Display Inversion Off

| 20H | IVNOFF (Normal Display Mode Off) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| INVOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | (20h) |
| Parameter | No Parameter | | | | | | | | | | | | - |

| | |
|---|---|
| Description | -This command is used to recover from display inversion mode.<br><br>"-" Don't care |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Display Inversion off |
| | S/W Reset | Display Inversion off |
| | H/W Reset | Display Inversion off |

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**10.1.15 INVON (21h): Display Inversion On**

| 21H | IVNOFF (Display Inversion On) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| INVON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | (21h) |
| Parameter | No Parameter | | | | | | | | | | | | - |

| Description | -This command is used to enter into display inversion mode<br><br>-To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.<br><br>"-" Don't care<br><br>(Example)<br>Memory       Display<br>Top-Left (0,0) |
|---|---|

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Display Inversion off |
| | S/W Reset | Display Inversion off |
| | H/W Reset | Display Inversion off |

| Flow Chart | |
|---|---|

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

Display Inversion OFF Mode

INVON (21h)

Display Inversion ON Mode

# ST7735

## 10.1.16 GAMSET (26h): Gamma Set

| 26H | GAMSET (Gamma Set) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| GAMSET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | (26h) |
| Parameter | 1 | ↑ | 1 | - | - | - | - | - | GC3 | GC2 | GC1 | GC0 | |

**Description**

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

| GC [7:0] | Parameter | Curve Selected | |
|---|---|---|---|
| | | GS=1 | GS=0 |
| 01h | GC0 | Gamma Curve 1 (G2.2) | Gamma Curve 1 (G1.0) |
| 02h | GC1 | Gamma Curve 2 (G1.8) | Gamma Curve 2 (G2.5) |
| 04h | GC2 | Gamma Curve 3 (G2.5) | Gamma Curve 3 (G2.2) |
| 08h | GC3 | Gamma Curve 4 (G1.0) | Gamma Curve 4 (G1.8) |

Note: All other values are undefined.

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 01h |
| S/W Reset | 01h |
| H/W Reset | 01h |

**Flow Chart**

# ST7735

## 10.1.17 DISPOFF (28h): Display Off

| 28H | DISPOFF (Display Off) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| DISPOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | (28h) |
| Parameter | No Parameter | | | | | | | | | | | - |

| Description | - This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. <br><br> - This command makes no change of contents of frame memory. <br><br> - This command does not change any other status. <br><br> - There will be no abnormal visible effect on the display. <br><br> - Exit from this command by Display On (29h) <br><br> - The delay time between DISPON and DISPOFF needs 120ms at least. <br><br> **(Example)** <br> Memory → Display <br><br> Note1: Complete 1 frame display (ex: continue 2-falling edges of VS) <br><br> Note2: Please use command 28h (display off) combined with command 10h (sleep in) to make module into display off status. Please check the application note of ST7735 when using display off function. |
|---|---|

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Display off |
| | S/W Reset | Display off |
| | H/W Reset | Display off |

**Flow Chart**

Display On Mode → DISPOFF → Display Off Mode

Legend:
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transter

# ST7735

## 10.1.18 DISPON (29h): Display On
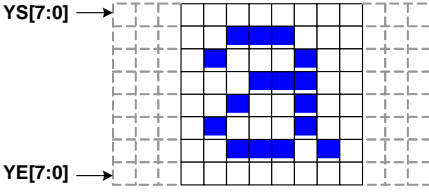
| 29H | DISPON (Display On) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DISPON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | (29h) |
| Parameter | No Parameter | | | | | | | | | | | - |

| Description | - This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.<br><br>- This command makes no change of contents of frame memory.<br><br>- This command does not change any other status.<br><br>- The delay time between DISPON and DISPOFF needs 120ms at least<br><br>**(Example)**<br>**Memory** → **Display** |
|---|---|

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Display off |
| | S/W Reset | Display off |
| | H/W Reset | Display off |

| Flow Chart | |
|---|---|

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

Display Off Mode

DISPON

Display On Mode

# ST7735

## 10.1.19 CASET (2Ah): Column Address Set

| 2AH | | | | | CASET(Colume Address Set)_ | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| CASET(2Ah) | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | (2Ah) |
| 1st parameter | 1 | ↑ | 1 | - | XS15 | XS14 | XS13 | XS12 | XS11 | XS10 | XS9 | XS8 | |
| 2nd parameter | 1 | ↑ | 1 | - | XS7 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 | |
| 3rd parameter | 1 | ↑ | 1 | - | XE15 | XE14 | XE13 | XE12 | XE11 | XE10 | XE9 | XE8 | |
| 4th parameter | 1 | ↑ | 1 | - | XE7 | XE6 | XE5 | XE4 | XE3 | XE2 | XE1 | XE0 | |

| Description | -The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes. <br><br> -Each value represents one column line in the Frame Memory. <br><br> XS[7:0]    XE[7:0] |
|---|---|

| Restriction | XS [15:0] always must be equal to or less than XE [15:0] <br><br> When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored. <br><br> 1. 128X160 memory base (GM = '011') <br><br> (Parameter range: 0 < XS [15:0] < XE [15:0] < 127 (007Fh)): MV="0") <br><br> (Parameter range: 0 < XS [15:0] < XE [15:0] < 159 (009Fh)): MV="1") <br><br> 2. 132X162 memory base (GM = '000') <br><br> (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV="0") <br><br> (Parameter range: 0 < XS [15:0] < XE [15:0] < 161 (00A1h)): MV="1") |
|---|---|

Default:

| GM Status | Status | Default Value | | |
|---|---|---|---|---|
| | | XS [7:0] | XE [7:0] (MV='0 ') | XE [7:0] (MV='1') |
| GM='011' (128x160 memory base) | Power On Sequence | 0000h | 007Fh (127) | |
| | S/W Reset | 0000h | 007Fh (127) | 009Fh (159) |
| | H/W Reset | 0000h | 007Fh (127) | |
| GM='000' (132x162 memory base) | Power On Sequence | 0000h | 0083h (131) | |
| | S/W Reset | 0000h | 0083h (131) | 00A1h (161) |
| | H/W Reset | 0000h | 0083h (131) | |

# ST7735

CASET

↓

1st parameter XS[15:0]
2nd parameter XE[15:0]

↓

PASET

↓

1st parameter YS[15:0]
2nd parameter YE[15:0]

↓

RAMWR

↓

Image Data
D1[7:0],D2[7:0]
... ... .Dn[7:0]

↓

Any Command

If needed

## Legend

Command

Parameter

Display

Action

Mode

Sequential
transter

# ST7735

## 10.1.20 RASET (2Bh): Row Address Set

| 2BH | RASET (Row Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RASET (2Bh) | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | (2Bh) |
| 1st parameter | 1 | ↑ | 1 | - | YS15 | YS14 | YS13 | YS12 | YS11 | YS10 | YS9 | YS8 | |
| 2nd parameter | 1 | ↑ | 1 | - | YS7 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 | |
| 3rd parameter | 1 | ↑ | 1 | - | YE15 | YE14 | YE13 | YE12 | YE11 | YE10 | YE9 | YE8 | |
| 4th parameter | 1 | ↑ | 1 | - | YE7 | YE6 | YE5 | YE4 | YE3 | YE2 | YE1 | YE0 | |

| | |
|---|---|
| Description | The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes.<br><br>Each value represents one column line in the Frame Memory.<br><br>**YS[7:0]** →<br><br>**YE[7:0]** → |
| Restriction | YS [15:0] always must be equal to or less than YE [15:0]<br><br>When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.<br><br>1. 128X160 memory base (GM = '011')<br><br>(Parameter range: 0 < YS [15:0] < YE [15:0] < 159 (009Fh)): MV="0"<br><br>(Parameter range: 0 < YS [15:0] < YE [15:0] < 127 (007Fh)): MV="1"<br><br>2. 132X162 memory base (GM = '000')<br><br>(Parameter range: 0 < YS [15:0] < YE [15:0] < 161 (00A1h)): MV="0"<br><br>(Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (0083h)): MV="1" |

| | | | | | |
|---|---|---|---|---|---|
| **Default** | GM status | Status | Default Value | | |
| | | | YS [15:0] | YE [15:0] (MV='0') | YE [15:0] (MV='1') |
| | GM='011' (128x160 memory base) | Power On Sequence | 0000h | 009Fh (159) | |
| | | S/W Reset | 0000h | 009Fh (159) | 007Fh (127) |
| | | H/W Reset | 0000h | 009Fh (159) | |
| | GM='000' (132x162 memory base) | Power On Sequence | 0000h | 00A1h (161) | |
| | | S/W Reset | 0000h | 00A1h (161) | 0083h (131) |
| | | H/W Reset | 0000h | 00A1h (161) | |

# ST7735

Flow Chart

CASET

↓

1st parameter XS[15:0]
2nd parameter XE[15:0]

↓

PASET

↓

1st parameter YS[15:0]
2nd parameter YE[15:0]

↓

RAMWR

↓

Image Data
D1[7:0],D2[7:0]
… … .Dn[7:0]

↓

Any Command

If needed

If needed

Legend

Command

Parameter

Display

Action

Mode

Sequential
transter

### 10.1.21 RAMWR (2Ch): Memory Write

| 2CH | RAMWR (Memory Write) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RAMWR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | (2Ch) |
| 1st parameter | 1 | ↑ | 1 | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| \| | 1 | ↑ | 1 | \| | \| | \| | \| | \| | \| | \| | \| | \| | |
| Nth parameter | 1 | ↑ | 1 | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

| Description | In all color modes, there is no restriction on length of parameters. |
|---|---|
| | 1. 128X160 memory base (GM = '011') |
| | 128x160x18-bit memory can be written by this command |
| | Memory range: (0000h, 0000h) -> (007Fh, 09Fh) |
| | 2. 132x162 memory base (GM = '000') |
| | 132x162x18-bit memory can be written on this command. |
| | Memory range: (0000h, 0000h) -> (0083h, 00A1h) |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Contents of memory is set randomly |
| | S/W Reset | Contents of memory is not cleared |
| | H/W Reset | Contents of memory is not cleared |

| Flow Chart | |
|---|---|

RAMWR

Image Data
D1[7:0],D2[7:0]
… … .Dn[7:0]

Any Command

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

# *ST7735*

## 10.1.22 RAMRD (2Eh): Memory Read

| 2EH | | RAMHD (Memory Read) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RAMHD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | (2Eh) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | |
| 2nd parameter | 1 | 1 | ↑ | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | | 1 | 1 | ↑ | | | | | | | | | | |
| (N+1)th parameter | 1 | 1 | ↑ | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

| Description | -This command is used to transfer data from frame memory to MCU.<br><br>-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.<br><br>-The Start Column/Start Row positions are different in accordance with MADCTL setting.<br><br>-Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 9.10<br><br>-Frame Read can be cancelled by sending any other command.<br><br>-The data color coding is fixed to 18-bit in reading function. Please see section 9.8 "Data color coding" for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.<br><br><br>Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory.Please check the LUT in chapter 9.17 when using memory read function. |
|---|---|

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Contents of memory is set randomly |
| | S/W Reset | Contents of memory is not cleared |
| | H/W Reset | Contents of memory is not cleared |

| Flow Chart |  |
|---|---|

### 10.1.23 PTLAR (30h): Partial Area

| 30H | | | | | PTLAR (Partial Area) | | | | | | | |
|-----|-----|-----|------|-------|-------|-------|-------|-------|-------|-------|-------|-----|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PTLAR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | (30h) |
| 1st parameter | 1 | ↑ | 1 | - | PSL15 | PSL14 | PSL13 | PSL12 | PSL11 | PSL10 | PSL9 | PSL8 | |
| 2nd parameter | 1 | ↑ | 1 | - | PSL7 | PSL6 | PSL5 | PSL4 | PSL3 | PSL2 | PSL1 | PSL0 | |
| 3rd parameter | 1 | ↑ | 1 | - | PEL15 | PEL14 | PEL13 | PEL12 | PEL11 | PEL10 | PEL9 | PEL8 | |
| 4th parameter | 1 | ↑ | 1 | - | PEL7 | PEL6 | PEL5 | PEL4 | PEL3 | PEL2 | PEL1 | PEL0 | |

**Description**

-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row

(PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

-If End Row > Start Row, when MADCTL ML='0'

**End row**
**PEL [7:0]** → Non-display area

Partial display area

**PSL [7:0]** → Non-display area
**Start row**

-If End Row > Start Row, when MADCTL ML='1'

**Start row**
**PSL [7:0]** → Non-display area

Partial display area

**PEL [7:0]** → Non-display area
**End row**

-If End Row < Start Row, when MADCTL ML='0'

**End row**
**PEL [7:0]** → Partial display area

Non-display area

**PSL [7:0]** →
**Start row**

Partial display area

-If End Row = Start Row then the Partial Area will be one row deep.

**Default**

| Status | Default Value | | |
|--------|---------------|---|---|
| | PSL [15:0] | PEL [15:0] | |
| GM[2:0] | "xxx" | GM[2:0]="011" | GM[2:0]="000" |
| Power On Sequence | 0000h | 009Fh | 00A1h |
| S/W Reset | 0000h | 009Fh | 00A1h |
| H/W Reset | 0000h | 009Fh | 00A1h |

# ST7735

## 2. Leave Partial Mode

### 1. TO Enter Partial Mode:

```
PLTAR
  ↓
SR[15:0]
  ↓
ER[15:0]
  ↓
PTLON
  ↓
Partial Mode
```

```
Partial Mode
  ↓
DISPOFF  ←──── ()ptional)
  ↓             To prevent
NORON          Tearing Effect
  ↓             Image displayed
Partial Mode
OFF
  ↓
RAMRW
  ↓
Image Data
D1[7:0],D2[7:0]
... ... ..Dn[7:0]
  ↓
DISPON
```

### Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transter

# ST7735
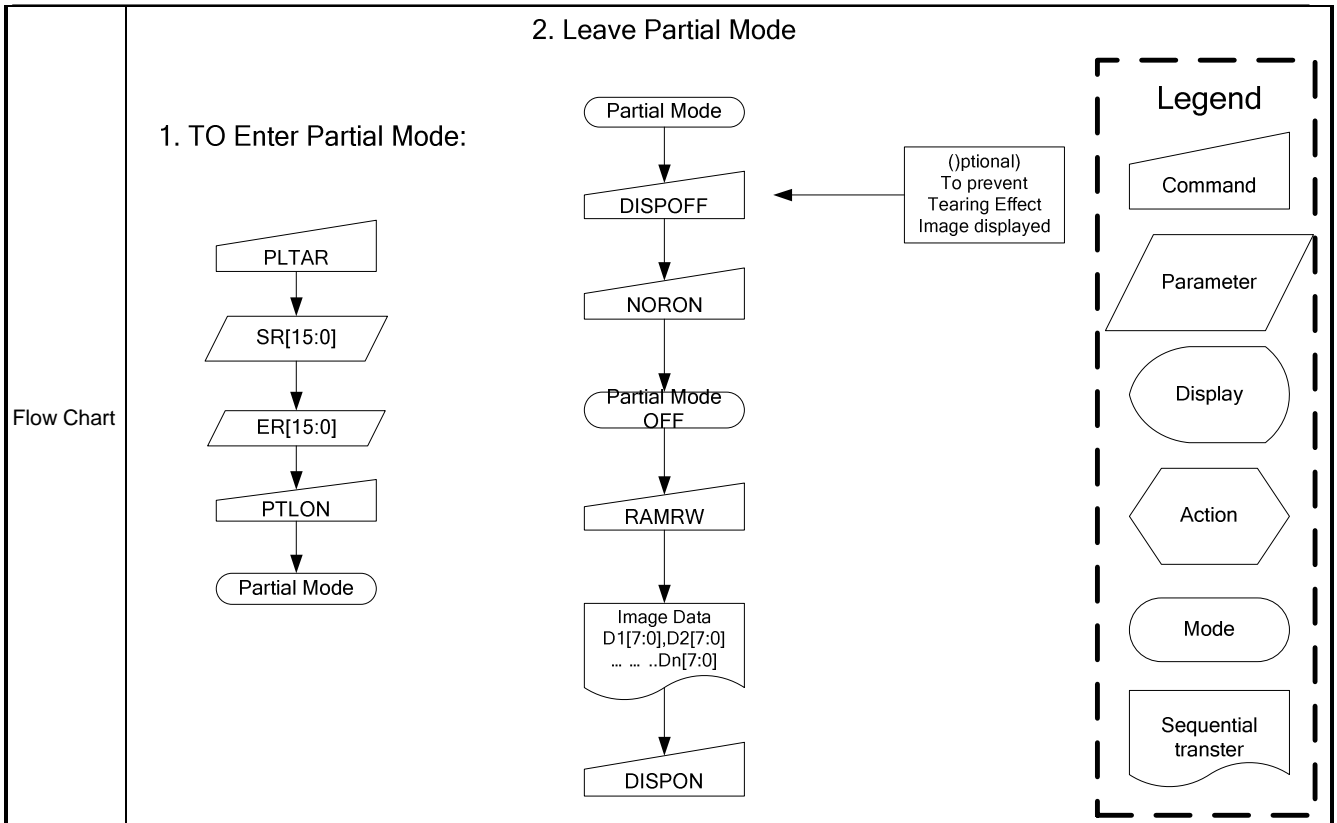
## 10.1.24 TEOFF (34h): Tearing Effect Line OFF

| 34H | TEOFF (Tearing Effect Line OFF) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| TEOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (34h) |
| Parameter | No Parameter | | | | | | | | | | | | - |
| Description | -This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. | | | | | | | | | | | | |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | OFF |
| | S/W Reset | OFF |
| | H/W Reset | OFF |

**Flow Chart**

TE Line Output ON

TEOFF

TE Line Output OFF

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

# ST7735

### 10.1.25 TEON (35h): Tearing Effect Line ON

| 35H | TEON (Tearing Effect Line ON) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| TEON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | (35h) |
| Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TELOM | |

| | |
|---|---|
| Description | -This command is used to turn ON the Tearing Effect output signal from the TE signal line.<br><br>-This output is not affected by changing MADCTL bit ML.<br><br>-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:<br><br>-When TELOM ='0': The Tearing Effect output line consists of V-Blanking information only<br><br>**Vertical time scale** $T_{vdl}$ $T_{vdh}$<br><br>-When TELOM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information<br><br>**Vertical time scale** $T_{vdl}$ $T_{vdh}$<br><br>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low. |
| Default | Status / Default Value table:<br><br>Power On Sequence — Tearing effect off & TELOM=0<br>S/W Reset — Tearing effect off & TELOM=0<br>H/W Reset — Tearing effect off & TELOM=0 |
| Flow Chart | TE Line Output OFF → TEON → TELOM → TE Line Output ON<br><br>Legend: Command, Parameter, Display, Action, Mode, Sequential transter |
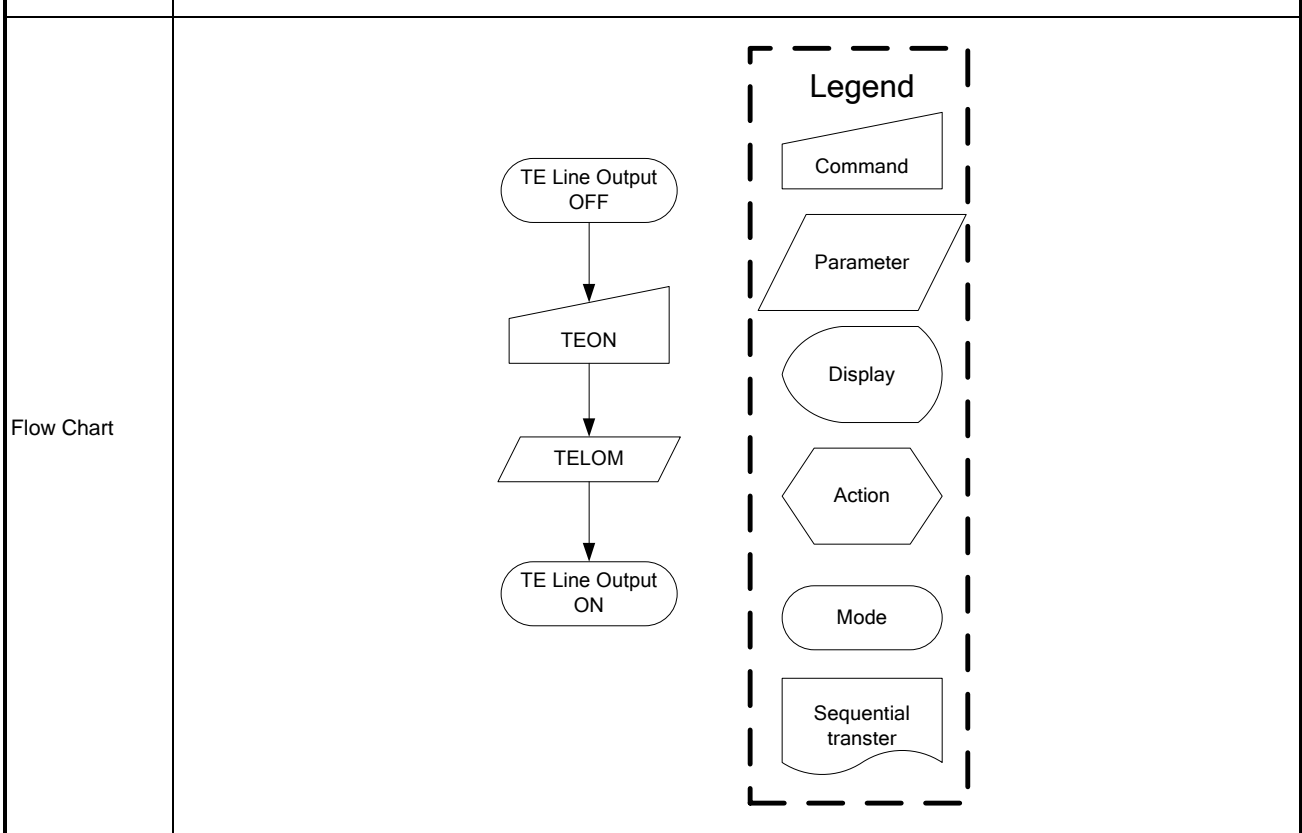
## 10.1.26 MADCTL (36h): Memory Data Access Control

| 36H | MADCTL (Memory Data Access Control) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| MADCTL | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (36h) |
| Parameter | 1 | ↑ | 1 | - | MY | MX | MV | ML | RGB | MH | - | - | |

| Description | -This command defines read/ write scanning direction of frame memory. |
|---|---|

-This command defines read/ write scanning direction of frame memory.

| Bit | NAME | DESCRIPTION |
|---|---|---|
| MY | Row Address Order | These 3bits controls MCU to memory write/read direction. |
| MX | Column Address Order | |
| MV | Row/Column Exchange | |
| ML | Vertical Refresh Order | LCD vertical refresh direction control<br>'0' = LCD vertical refresh Top to Bottom<br>'1' = LCD vertical refresh Bottom to Top |
| RGB | RGB-BGR ORDER | Color selector switch control<br>'0' =RGB color filter panel,<br>'1' =BGR color filter panel) |
| MH | Horizontal Refresh Order | LCD horizontal refresh direction control<br>'0' = LCD horizontal refresh Left to right<br>'1' = LCD horizontal refresh right to left |

-Bit Assignment

# *ST7735*

| | |
|---|---|
| | **Top-left (0, 0)** **Memory**     **Top-left (0, 0)** **Memory** <br><br> ML="0"      ML="1" <br><br> Send first / Send 2nd / Send 3rd → Send last    Send last ← Send 3rd / Send 2nd / Send first <br><br> **Top-left (0, 0)** **Display**     **Top-left (0, 0)** **Display** |

| Default | | |
|---|---|---|
| | Status | Default Value |
| | Power On Sequence | MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0 |
| | S/W Reset | No Change |
| | H/W Reset | MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0 |

| Flow Chart | |
|---|---|
| | MADCTL <br><br> ↓ <br><br> 1st parameter B[7:0]      **Legend** <br> Command <br> Parameter <br> Display <br> Action <br> Mode <br> Sequential transfer |

## ST7735

### 10.1.27 IDMOFF (38h): Idle Mode Off

| 38H | IDMOFF (Idle Mode Off) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| IDMOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | (38h) |
| Parameter | No Parameter | | | | | | | | | | | | - |

| Description | -This command is used to recover from Idle mode on.<br><br>-In the idle off mode,<br><br>1. LCD can display 4096, 65k or 262k colors.<br><br>2. Normal frame frequency is applied. |
|---|---|

| Default | | |
|---|---|---|
| | Status | Default Value |
| | Power On Sequence | Idle Mode Off |
| | S/W Reset | Idle Mode Off |
| | H/W Reset | Idle Mode Off |

| Flow Chart | |
|---|---|

Idle on mode

IDMOFF

Idle off mode

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

# *ST7735*

## 10.1.28 IDMON (39h): Idle Mode On

| 39H | IDMON (Idle Mode On) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| IDMOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | (39h) |
| Parameter | No Parameter | | | | | | | | | | | - |

| Description | -This command is used to enter into Idle mode on. <br><br> -There will be no abnormal visible effect on the display mode change transition. <br><br> -In the idle on mode, <br><br> 1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. <br><br> 2. 8-Color mode frame frequency is applied. <br><br> 3. Exit from IDMON by Idle Mode Off (38h) command |
|---|---|

(Example) Memory → Display, Top-Left (0,0)

| Color | R5 R4 R3 R2 R1 R0 | G5 G4 G3 G2 G1 G0 | B5 B4 B3 B4 B1 B0 |
|---|---|---|---|
| Black | 0xxxxx | 0xxxxx | 0xxxxx |
| Blue | 0xxxxx | 0xxxxx | 1xxxxx |
| Red | 1xxxxx | 0xxxxx | 0xxxxx |
| Magenta | 1xxxxx | 0xxxxx | 1xxxxx |
| Green | 0xxxxx | 1xxxxx | 0xxxxx |
| Cyan | 0xxxxx | 1xxxxx | 1xxxxx |
| Yellow | 1xxxxx | 1xxxxx | 0xxxxx |
| White | 1xxxxx | 1xxxxx | 1xxxxx |

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | No |
| | Partial Mode On, Idle Mode On, Sleep Out | No |
| | Sleep In | Yes |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Idle Mode Off |
| | S/W Reset | Idle Mode Off |
| | H/W Reset | Idle Mode Off |

| Flow Chart | |
|---|---|

Idle off mode

↓

IDMON

↓

Idle on mode

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

# *ST7735*

## 10.1.29 COLMOD (3Ah): Interface Pixel Format

| 3AH | COLMOD (3Ah): Interface Pixel Format | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| COLMOD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | (3Ah) |
| Parameter | 1 | ↑ | 1 | - | - | - | - | - | - | IFPF2 | IFPF1 | IFPF0 | |

| Description | This command is used to define the format of RGB picture data, which is to be transferred via the |
|---|---|
| | MCU interface. The formats are shown in the table: |

| IFPF[2:0] | | MCU Interface Color Format |
|---|---|---|
| 011 | 3 | 12-bit/pixel |
| 101 | 5 | 16-bit/pixel |
| 110 | 6 | 18-bit/pixel |
| 111 | 7 | No used |

Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

Note2: The Command 3Ah should be set at 55h when writing 16-bit/pixel data into frame memory, but 3Ah should be re-set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | No |
| | Partial Mode On, Idle Mode On, Sleep Out | No |
| | Sleep In | Yes |

| Default | Status | Default Value | |
|---|---|---|---|
| | | IFPF[2:0] | VIPF[3:0] |
| | Power On Sequence | 0110(18-bit/Pixel) | 0110(18-bit/Pixel) |
| | S/W Reset | No Change | No Change |
| | H/W Reset | 0110(18-bit/Pixel) | 0110(18-bit/Pixel) |

| Flow Chart |  |
|---|---|

# *ST7735*

## 10.1.30 RDID1 (DAh): Read ID1 Value

| DAH | RDID1 (Read ID1 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDID1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | (DAh) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | |

| | |
|---|---|
| Description | -This read byte returns 8-bit LCD module's manufacturer ID<br><br>-The 1st parameter is dummy data<br><br>-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.<br><br>NOTE: See command RDDID (04h), 2nd parameter. |

| | Status | Availability |
|---|---|---|
| Register Availability | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | No |
| | Partial Mode On, Idle Mode On, Sleep Out | No |
| | Sleep In | Yes |

| | Status | Default Value |
|---|---|---|
| Default | Power On Sequence | - |
| | S/W Reset | - |
| | H/W Reset | - |

| | |
|---|---|
| Flow Chart |  |

**10.1.31 RDID2 (DBh): Read ID2 Value**

| DBH | | | | | | RDID2 (Read ID2 Value) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDID2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | (DBh) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | 1 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | |

| | |
|---|---|
| Description | -This read byte returns 8-bit LCD module/driver version ID<br><br>-The 1st parameter is dummy data<br><br>-The 2nd parameter (ID26 to ID20): LCD module/driver version ID<br><br>-Parameter Range: ID=80h to FFh<br><br><table><tr><td>ID26 to ID20</td><td>Version</td><td>Changes</td></tr><tr><td>80h</td><td></td><td></td></tr><tr><td>81h</td><td></td><td></td></tr><tr><td>82h</td><td></td><td></td></tr><tr><td>83h</td><td></td><td></td></tr></table><br>NOTE: See command RDDID (04h), 3rd parameter. |
| Register Availability | <table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table> |
| Default | <table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>NV Value</td></tr><tr><td>S/W Reset</td><td>NV Value</td></tr><tr><td>H/W Reset</td><td>NV Value</td></tr></table> |
| Flow Chart |  |

## 10.1.32 RDID3 (DCh): Read ID3 Value

| DCH | | | | | RDID3 (Read ID2 Value) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| RDID3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | (DCh) |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | |

| | |
|---|---|
| Description | -This read byte returns 8-bit LCD module/driver ID. <br><br> -The 1st parameter is dummy data <br><br> -The 2nd parameter (ID37 to ID30): LCD module/driver ID. <br><br> NOTE: See command RDDID (04h), 4th parameter. |

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | No |
| | Partial Mode On, Idle Mode On, Sleep Out | No |
| | Sleep In | Yes |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | NV Value |
| | S/W Reset | NV Value |
| | H/W Reset | NV Value |

| | |
|---|---|
| Flow Chart |  |

## 10.2 Panel Function Command List and Description

Table 10.2.1 Panel Function Command List (1)

| Instruction | Refer | D/CX | WRX | RDX | D23-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FRMCTR1 | 10.2.1 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | (B1h) | In normal mode (Full colors) |
| | | 1 | ↑ | 1 | - | | | | | RTNA3 | RTNA2 | RTNA1 | RTNA0 | | RTNA set 1-line period FPA: front porch BPA: back porch |
| | | 1 | ↑ | 1 | - | | | FPA5 | FPA4 | FPA3 | FPA2 | FPA1 | FPA0 | | |
| | | 1 | ↑ | 1 | - | | | BPA5 | BPA4 | BPA3 | BPA2 | BPA1 | BPA0 | | |
| FRMCTR2 | 10.2.2 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | (B2h) | In Idle mode (8-colors) |
| | | 1 | ↑ | 1 | - | | | | | RTNB3 | RTNB2 | RTNB1 | RTNB0 | | RTNB: set 1-line period FPB: front porch BPB: back porch |
| | | 1 | ↑ | 1 | - | | | FPB5 | FPB4 | FPB3 | FPB2 | FPB1 | FPB0 | | |
| | | 1 | ↑ | 1 | - | | | BPB5 | BPB4 | BPB3 | BPB2 | BPB1 | BPB0 | | |
| FRMCTR3 | 10.2.3 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (B3h) | In partial mode + Full colors |
| | | 1 | ↑ | 1 | - | | | | | RTNC3 | RTNC2 | RTNC1 | RTNC0 | | RTNC,RTND: set 1-line period FPC,FPD: front porch BPC,BPD: back porch |
| | | 1 | ↑ | 1 | - | | | FPC5 | FPC4 | FPC3 | FPC2 | FPC1 | FPC0 | | |
| | | 1 | ↑ | 1 | - | | | BPC5 | BPC4 | BPC3 | BPC2 | BPC1 | BPC0 | | |
| | | 1 | ↑ | 1 | - | | | | | RTND3 | RTND2 | RTND1 | RTND0 | | |
| | | 1 | ↑ | 1 | - | | | FPD5 | FPD4 | FPD3 | FPD2 | FPD1 | FPD0 | | |
| | | 1 | ↑ | 1 | - | | | BPD5 | BPD4 | BPD3 | BPD2 | BPD1 | BPD0 | | |
| INVCTR | 10.2.4 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (B4h) | Display inversion control |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | NLA | NLB | NLC | | NLA,NLB,NLC set inversion |
| DISSET5 | 10.2.5 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (B6h) | Display function setting |
| | | 1 | ↑ | 1 | - | 0 | 0 | NO1 | NO0 | SDT1 | SDT0 | EQ1 | EQ0 | | SDT: set amount of source delay |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | PTG1 | PTG0 | PT1 | PT0 | | EQ: set EQ period PT: No display area source/VCOM/Gate output control |

Table 10.2.2 Panel Function Command List (2)

| Instruction | Refer | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWCTR1 | 10.2.6 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | (C0h) | Power control setting |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | VRH4 | VRH3 | VRH2 | VRH1 | VRH0 | | VRH: Set the GVDD voltage |
| | | 1 | ↑ | 1 | - | 0 | 1 | IB-SEL1 | IB-SEL0 | 0 | 0 | 0 | 0 | | |
| PWCTR2 | 10.2.7 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | (C1h) | Power control setting |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | BT2 | BT1 | BT0 | | BT: set VGH/ VGL voltage |
| PWCTR3 | 10.2.8 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (C2h) | In normal mode (Full colors) |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | APA2 | APA1 | APA0 | | APA: adjust the operational amplifier |
| | | | | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | DCA2 | DCA1 | DCA0 | | DCA: adjust the booster Voltage |
| | | | | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| PWCTR4 | 10.2.9 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | (C3h) | In Idle mode (8-colors) |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | APB2 | APB1 | APB0 | | APB: adjust the operational amplifier |
| | | | | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | DCB2 | DCB1 | DCB0 | | DCB: adjust the booster Voltage |
| | | | | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| PWCTR5 | 10.2.10 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | (C4h) | In partial mode + Full colors |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | APC2 | APC1 | APC0 | | APC: adjust the operational amplifier |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | DCC2 | DCC1 | DCC0 | | DCC: adjust the booster circuit for Idle mode |
| VMCTR1 | 10.2.11 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | (C5h) | VCOM control 1 |
| | | 1 | ↑ | 1 | - | - | VMH6 | VMH5 | VMH4 | VMH3 | VMH2 | VMH1 | VMH0 | | VMH: VCOMH voltage control |
| | | 1 | ↑ | 1 | - | - | VML6 | VML5 | VML4 | VML3 | VML2 | VML1 | VML0 | | VML: VCOML voltage control |
| VMOFCTR | 10.2.12 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | (C7h) | Set VCOM offset control |
| | | 1 | ↑ | 1 | - | - | - | - | VMF4 | VMF3 | VMF2 | VMF1 | VMF0 | | |
| WRID2 | 10.2.13 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | (D1h) | Set LCM version code |
| | | 1 | ↑ | 1 | - | - | ID2[6] | ID2[5] | ID2[4] | ID2[3] | ID2[2] | ID2[1] | ID2[0] | | |

"-": Don't care

*Note 1: C0h to C7h are fixed for about power controller*

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Table 10.2.3 Panel Function Command List (3)

| Instruction | Refer | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRID3 | 10.2.14 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | (D2h) | Customer Project code |
| | | 1 | ↑ | 1 | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | | Set the project code at ID3 |
| PWCTR6 | 10.2.15 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | (FC) | In partial mode + Idle |
| | | 1 | ↑ | 1 | - | | Sapa [2] | Sapa [1] | Sapa [0] | --- | Sapb [2] | Sapb [1] | Sapb [0] | | |
| | | 1 | ↑ | 1 | - | | Sapc [2] | Sapc [1] | Sapc [0] | --- | DCD [2] | DCD [1] | DCD [0] | | |
| NVCTR1 | 10.2.16 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | (D9) | EEPROM control status |
| | | 1 | ↑ | 1 | - | 0 | 0 | VMF _EN | ID2 _EN | 0 | 0 | 0 | 0 | | |
| NVCTR2 | 10.2.17 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | (DEh) | EEPROM Read Command |
| | | 1 | ↑ | 1 | - | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5 | Action code |
| NVCTR3 | 10.2.18 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | (DFh) | EEPROM Write Command |
| | | 1 | ↑ | 1 | - | EE_ IB7 | EE_ IB6 | EE_ IB5 | EE_ IB4 | EE_ IB3 | EE_ IB2 | EE_ IB1 | EE_ IB0 | | |
| | | 1 | ↑ | 1 | - | EE_ CMD7 | EE_ CMD6 | EE_ CMD5 | EE_ CMD4 | EE_ CMD3 | EE_ CMD2 | EE_ CMD1 | EE_ CMD0 | | |
| | | 1 | ↑ | 1 | - | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5 | |

 "-": Don't care

*Note 1: The D1h to D3h registers are fixed for about ID code setting.*

*Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)*

Table 10.2.4 Panel Function Command List (4)

| Instruction | Refer | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GAMCTRP1 | 10.2.19 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | (E0h) | Set Gamma adjustment (+ polarity) |
| | | 1 | ↑ | 1 | - | --- | --- | VRFP[5] | VRFP[4] | VRFP[3] | VRFP[2] | VRFP[1] | VRF0P[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | VOS0P[5] | VOS0P[4] | VOS0P[3] | VOS0P[2] | VOS0P[1] | VOS0P[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP0[5] | PKP0[4] | PKP0[3] | PKP0[2] | PKP0[1] | PKP0[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP1[5] | PKP1[4] | PKP1[3] | PKP1[2] | PKP1[1] | PKP1[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP2[5] | PKP2[4] | PKP2[3] | PKP2[2] | PKP2[1] | PKP2[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP3[5] | PKP3[4] | PKP3[3] | PKP3[2] | PKP3[1] | PKP3[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP4[5] | PKP4[4] | PKP4[3] | PKP4[2] | PKP4[1] | PKP4[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP5[5] | PKP5[4] | PKP5[3] | PKP5[2] | PKP5[1] | PKP5[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP6[5] | PKP6[4] | PKP6[3] | PKP6[2] | PKP6[1] | PKP6[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP7[5] | PKP7[4] | PKP7[3] | PKP7[2] | PKP7[1] | PKP7[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP8[5] | PKP8[4] | PKP8[3] | PKP8[2] | PKP8[1] | PKP8[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKP9[5] | PKP9[4] | PKP9[3] | PKP9[2] | PKP9[1] | PKP9[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV0P[5] | SELV0P[4] | SELV0P[3] | SELV0P[2] | SELV0P[1] | SELV0P[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV1P[5] | SELV1P[4] | SELV1P[3] | SELV1P[2] | SELV1P[1] | SELV1P[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV62P[5] | SELV62P[4] | SELV62P[3] | SELV62P[2] | SELV62P[1] | SELV62P[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV63P[5] | SELV63P[4] | SELV63P[3] | SELV63P[2] | SELV63P[1] | SELV63P[0] | | |
| GAMCTRN1 | 10.2.20 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | (E1h) | Set Gamma adjustment (- polarity) |
| | | 1 | ↑ | 1 | - | --- | --- | VRF0N[5] | VRF0N[4] | VRF0N[3] | VRF0N[2] | VRF0N[1] | VRF0N[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | VOS0N[5] | VOS0N[4] | VOS0N[3] | VOS0N[2] | VOS0N[1] | VOS0N[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN0[5] | PKN0[4] | PKN0[3] | PKN0[2] | PKN0[1] | PKN0[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN1[5] | PKN1[4] | PKN1[3] | PKN1[2] | PKN1[1] | PKN1[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN2[5] | PKN2[4] | PKN2[3] | PKN2[2] | PKN2[1] | PKN2[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN3[5] | PKN3[4] | PKN3[3] | PKN3[2] | PKN3[1] | PKN3[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN4[5] | PKN4[4] | PKN4[3] | PKN4[2] | PKN4[1] | PKN4[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN5[5] | PKN5[4] | PKN5[3] | PKN5[2] | PKN5[1] | PKN5[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN6[5] | PKN6[4] | PKN6[3] | PKN6[2] | PKN6[1] | PKN6[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN7[5] | PKN7[4] | PKN7[3] | PKN7[2] | PKN7[1] | PKN7[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN8[5] | PKN8[4] | PKN8[3] | PKN8[2] | PKN8[1] | PKN8[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | PKN9[5] | PKN9[4] | PKN9[3] | PKN9[2] | PKN9[1] | PKN9[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV0N[5] | SELV0N[4] | SELV0N[3] | SELV0N[2] | SELV0N[1] | SELV0N[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV1N[5] | SELV1N[4] | SELV1N[3] | SELV1N[2] | SELV1N[1] | SELV1N[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV62N[5] | SELV62N[4] | SELV62N[3] | SELV62N[2] | SELV62N[1] | SELV62N[0] | | |
| | | 1 | ↑ | 1 | - | --- | --- | SELV63N[5] | SELV63N[4] | SELV63N[3] | SELV63N[2] | SELV63N[1] | SELV63N[0] | | |
| EXTCTRL | 10.2.21 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | (F0h) | Extension Command Control |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | |
| VCOM4L | 10.2.22 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (FFh) | Vcom 4 Level control |
| | | 1 | ↑ | 1 | - | TC2[3] | TC2[2] | TC2[1] | TC2[0] | TC1[3] | TC1[2] | TC1[1] | TC1[0] | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | TC3[3] | TC3[2] | TC3[1] | TC3[0] | | |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | | |

 "-": Don't care

*Note 1: E0-E1 registers are fixed for adjusting Gamma*

## 10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

| B1H | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | FRMCTR1 (Frame Rate Control) | | | | | | | | | | | |
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| FRMCTR1 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | (B1h) |
| 1$^{st}$ parameter | 1 | ↑ | 1 | - | - | - | - | - | RTNA3 | RTNA2 | RTNA1 | RTNA0 | |
| 2$^{nd}$ parameter | 1 | ↑ | 1 | - | - | - | FPA5 | FPA4 | FPA3 | FPA2 | FPA1 | FPA0 | |
| 3$^{rd}$ parameter | 1 | ↑ | 1 | - | - | - | BPA5 | BPA4 | BPA3 | BPA2 | BPA1 | BPA0 | |

| Description | -Set the frame frequency of the full colors normal mode. <br><br> - Frame rate=fosc/((RTNA + 20) x (LINE + FPA + BPA)) <br><br> - 1 < FPA(front porch) + BPA(back porch) ; Back porch $\neq 0$ <br><br> Note: fosc = 333kHz |
|---|---|

| Default | | | |
|---|---|---|---|
| | Status | Default Value | |
| | | GM[2:0] = "000" | GM[2:0] = "011" |
| | Power On Sequence | 02h/2Ch/2Dh | 02h/2Dh/2Eh |
| | S/W Reset | 02h/2Ch/2Dh | 02h/2Dh/2Eh |
| | H/W Reset | 02h/2Ch/2Dh | 02h/2Dh/2Eh |

| Flow Chart |  |
|---|---|

### 10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

| B2H | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | FRMCTR2 (Frame Rate Control) | | | | | | | | | |
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| FRMCTR2 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | (B2h) |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | RTNB3 | RTNB2 | RTNB1 | RTNB0 | |
| 2nd parameter | 1 | ↑ | 1 | - | - | - | FPB5 | FPB4 | FPB3 | FPB2 | FPB1 | FPB0 | |
| 3rd parameter | 1 | ↑ | 1 | - | - | - | BPB5 | BPB4 | BPB3 | BPB2 | BPB1 | BPB0 | |

| Description | -Set the frame frequency of the Idle mode.<br><br>- Frame rate=fosc/((RTNB + 20) x (LINE + FPB + BPB))<br><br>- 1 < FPB(front porch) + BPB(back porch) ; Back porch $\neq 0$<br><br>Note: fosc = 333kHz |
|---|---|

| Default | Status | Default Value | |
|---|---|---|---|
| | | GM[2:0] = "000" | GM[2:0] = "011" |
| | Power On Sequence | 02h/2Ch/2Dh | 02h/2Dh/2Eh |
| | S/W Reset | 02h/2Ch/2Dh | 02h/2Dh/2Eh |
| | H/W Reset | 02h/2Ch/2Dh | 02h/2Dh/2Eh |

| Flow Chart | |
|---|---|

FRMCTR2

1st Parameter
2nd parameter

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

### 10.2.3  FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

| B3H | FRMCTR3 (Frame Rate Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| FRMCTR3 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (B3h) |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | RTNC3 | RTNC2 | RTNC1 | RTNC0 | |
| 2nd parameter | 1 | ↑ | 1 | - | - | - | FPC5 | FPC4 | FPC3 | FPC2 | FPC1 | FPC0 | |
| 3rd parameter | 1 | ↑ | 1 | - | - | - | BPC5 | BPC4 | BPC3 | BPC2 | BPC1 | BPC0 | |
| 4th parameter | 1 | ↑ | 1 | - | - | - | - | - | RTND3 | RTND2 | RTND1 | RTND0 | |
| 5th parameter | 1 | ↑ | 1 | - | - | - | FPD5 | FPD4 | FPD3 | FPD2 | FPD1 | FPD0 | |
| 6th parameter | 1 | ↑ | 1 | - | - | - | BPD5 | BPD4 | BPD3 | BPD2 | BPD1 | BPD0 | |

| Description | -Set the frame frequency of the Partial mode/ full colors.<br><br>- 1st parameter to 3rd parameter are used in line inversion mode.<br><br>- 4th parameter to 6th parameter are used in frame inversion mode.<br><br>- Frame rate=fosc/((RTNC + 20) x (LINE + FPC + BPC))<br><br>- 1 < FPC(front porch) + BPC(back porch) ; Back porch $\neq 0$<br><br>Note: fosc = 333kHz |
|---|---|

| Default | | | |
|---|---|---|---|
| | Status | Default Value | |
| | | GM[2:0] = "000" | GM[2:0] = "011" |
| | Power On Sequence | 02h/2Ch/2Dh/02h/2Ch/2Dh | 02h/2Dh/2Eh/02h/2Dh/2Eh |
| | S/W Reset | 02h/2Ch/2Dh/02h/2Ch/2Dh | 02h/2Dh/2Eh/02h/2Dh/2Eh |
| | H/W Reset | 02h/2Ch/2Dh/02h/2Ch/2Dh | 02h/2Dh/2Eh/02h/2Dh/2Eh |

| Flow Chart | |
|---|---|

FRMCTR3

1st Parameter
2nd parameter

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

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## 10.2.4  INVCTR (B4h): Display Inversion Control

| B4H | INVCTR (Display Inversion Control) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| INVCTR | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (B4h) |
| Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | NLA | NLB | NLC | |

| Description | -Display Inversion mode control<br><br>-NLA: Inversion setting in full colors normal mode (Normal mode on) |
|---|---|

| NLA | Inversion setting in full Colors normal mode |
|---|---|
| 0 | Line Inversion |
| 1 | Frame Inversion |

-NLB: Inversion setting in Idle mode (Idle mode on)

| NLB | Inversion setting in Idle mode |
|---|---|
| 0 | Line Inversion |
| 1 | Frame Inversion |

-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

| NLC | Inversion setting in full Colors partial mode |
|---|---|
| 0 | Line Inversion |
| 1 | Frame Inversion |

**Default**

| Status | Default Value | | | |
|---|---|---|---|---|
| | NLA | NLB | NLC | B4h |
| Power On Sequence | 1d | 1d | 1d | 03h |
| S/W Reset | 1d | 1d | 1d | 03h |
| H/W Reset | 1d | 1d | 1d | 03h |

**Flow Chart**

INVCTR

↓

1st Parameter

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

### 10.2.5  DISSET5 (B6h): Display Function set 5

| B6H | DISSET (Display Function set 5) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| DISSET5 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (B6h) |
| 1st parameter | 1 | ↑ | 1 | - | 0 | 0 | NO1 | NO0 | SDT1 | SDT0 | EQ1 | EQ0 | |
| 2nd parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | PTG1 | PTG0 | PT1 | PT0 | |

| Description | 1st parameter: Set output waveform relation.<br>-NO[1:0]: Set the amount of non-overlap of the gate output |
|---|---|

| NO[1:0] | | Amount of non-overlap of the gate output |
|---|---|---|
| | | Refer the Internal oscillator |
| 00 | 00h | 1 clock cycle |
| 01 | 01h | 2 clock cycle |
| 10 | 02h | 4 clock cycle |
| 11 | 03h | 6 clock cycle |

-SDT[1:0]: Set delay amount from gate signal rising edge of the source output.

| SDT[1:0] | | Delay amount form gate signal rising edge of the source output |
|---|---|---|
| | | Refer the Internal oscillator |
| 00 | 00h | 0 clock cycle |
| 01 | 01h | 1 clock cycle |
| 10 | 02h | 2 clock cycle |
| 11 | 03h | 3 clock cycle |

-EQ[1:0]: Set the Equalizing period

| EQ[1:0] | | Equalizing period |
|---|---|---|
| | | Refer the Internal oscillator |
| 00 | 00h | No EQ |
| 01 | 01h | 3 clock cycle |
| 10 | 02h | 5 clock cycle |
| 11 | 03h | 7 clock cycle |

-2nd parameter: Set the output waveform in non-display area.
-PTG[1:0]: Determine gate output in a non-display area in the partial mode

| PTG[1:0] | | Gate output in a non-display area |
|---|---|---|
| 00 | 00h | Normal scan |
| 01 | 01h | Fix on VGL |
| 10 | 02h | Fix on VGL |
| 11 | 03h | Fix on VGL |

-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode

| PT[1:0] | | Source output on non-display area | | VCOM output on non-display area | |
|---|---|---|---|---|---|
| | | Positive | Negative | Positive | Negative |
| 00 | 00h | V63 | V0 | VCOML | VCOMH |
| 01 | 01h | V0 | V63 | VCOML | VCOMH |
| 10 | 02h | AGND | AGND | AGND | AGND |
| 11 | 03h | Hi-z | Hi-z | AGND | AGND |

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| | Status | Default Value |
|---|---|---|
| Default | | B6h |
| | Power On Sequence | 15h/00h |
| | S/W Reset | 15h/00h |
| | H/W Reset | 15h/00h |

| | |
|---|---|
| Flow Chart | DISSET5 → 1st Parameter / 2nd parameter<br><br>**Legend**<br>Command<br>Parameter<br>Display<br>Action<br>Mode<br>Sequential transter |

### 10.2.6 PWCTR1 (C0h): Power Control 1

| C0H | | | | | | | | | | | | | PWCTR1 (Power Control 1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PWCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | (C0h) |
| 1st paramete | 1 | ↑ | 1 | - | 0 | 0 | 0 | VRH4 | VRH3 | VRH2 | VRH1 | VRH0 | |
| 2nd parameter | 1 | ↑ | 1 | - | 0 | 1 | IB_SEL1 | IB_SEL0 | - | 0 | 0 | 0 | |

Description

-Set the GVDD voltage
Note: AVDD=5.3V

| VRH[4:0] | | GVDD |
|---|---|---|
| 00000 | 00h | 5.00 |
| 00001 | 01h | 4.75 |
| 00010 | 02h | 4.70 |
| 00011 | 03h | 4.65 |
| 00100 | 04h | 4.60 |
| 00101 | 05h | 4.55 |
| 00110 | 06h | 4.50 |
| 00111 | 07h | 4.45 |
| 01000 | 08h | 4.40 |
| 01001 | 09h | 4.35 |
| 01010 | 0Ah | 4.30 |
| 01011 | 0Bh | 4.25 |
| 01100 | 0Ch | 4.20 |
| 01101 | 0Dh | 4.15 |
| 01110 | 0Eh | 4.10 |
| 01111 | 0Fh | 4.05 |
| 10000 | 10h | 4.00 |
| 10001 | 11h | 3.95 |
| 10010 | 12h | 3.90 |
| 10011 | 13h | 3.85 |
| 10100 | 14h | 3.80 |
| 10101 | 15h | 3.75 |
| 10110 | 16h | 3.70 |
| 10111 | 17h | 3.65 |
| 11000 | 18h | 3.60 |
| 11001 | 19h | 3.55 |
| 11010 | 1Ah | 3.50 |
| 11011 | 1Bh | 3.45 |
| 11100 | 1Ch | 3.40 |
| 11101 | 1Dh | 3.35 |
| 11110 | 1Eh | 3.25 |
| 11111 | 1Fh | 3.00 |

| IB_SEL[1:0] | | AVDD |
|---|---|---|
| 00 | 00h | 2.5uA |
| 01 | 01h | 2.0uA |
| 10 | 02h | 1.5uA |
| 11 | 03h | 1.0uA |

Restriction

-If this register not using the register need be reserved.
-The deviation value of GVDD between with Measurement and Specification : Max <= 50mV

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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| Default | Status | Default Value |
| --- | --- | --- |
| | | C0h |
| | Power On Sequence | 02h/70h |
| | S/W Reset | 02h/70h |
| | H/W Reset | 02h/70h |

Flow Chart

PWCTR1

1st Parameter
2nd parameter

Legend

Command

Parameter

Display

Action

Mode

Sequential
transter

### 10.2.7  PWCTR2 (C1h): Power Control 2

| C1H | PWCTR2 (Power Control 2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PWCTR2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | (C1h) |
| 1st parameter | 1 | ↑ | 1 | | 0 | 0 | 0 | 0 | 0 | BT2 | BT1 | BT0 | |

| Description | -Set the VGH and VGL supply power level |
|---|---|

| BT[2:0] | VGH | | VGL | |
|---|---|---|---|---|
| 000 | 4X | 9.8 | -3X | -7.35 |
| 001 | 4X | 9.8 | -4X | -9.8 |
| 010 | 5X | 12.25 | -3X | -7.35 |
| 011 | 5X | 12.25 | -4X | -9.8 |
| 100 | 5X | 12.25 | -5X | -12.25 |
| 101 | 6X | 14.7 | -3X | -7.35 |
| 110 | 6X | 14.7 | -4X | -9.8 |
| 111 | 6X | 14.7 | -5X | -12.25 |

| Restriction | -If this register not using the register need be reserved.<br>-The deviation value of VGH/ VGL between with Measurement and Specification: Max <= 1V<br>-VGH-VGL <= 32V |
|---|---|

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In | Yes |

| Default | Status | Default Value |
|---|---|---|
| | | C1h |
| | Power On Sequence | 05h |
| | S/W Reset | 05h |
| | H/W Reset | 05h |

| Flow Chart |  |
|---|---|

### 10.2.8  PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

| C2H | | | | | | PWCTR3 (Power Control 3) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PWCTR3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (C2h) |
| 1st parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | APA2 | APA1 | APA0 | |
| 2nd parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | DCA2 | DCA1 | DCA0 | |

| | |
|---|---|
| Description | -Set the amount of current in Operational amplifier in normal mode/full colors.<br>-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.<br><br>**AP[2:0] table**<br><br>-Set the Booster circuit Step-up cycle in Normal mode/ full colors.<br><br>**DC[2:0] table**<br><br>Note: BCLK is Clock frequency for Booster circuit |

| AP[2:0] | | Amount of Current in Operational Amplifier |
|---|---|---|
| 000 | 00h | Operation of the operational amplifier stops |
| 001 | 01h | Small |
| 010 | 02h | Medium Low |
| 011 | 03h | Medium |
| 100 | 04h | Medium High |
| 101 | 05h | Large |
| 110 | 06h | Reserved |
| 111 | 07h | Reserved |

| DC[2:0] | | Step-up cycle in Booster circuit 1 | Step-up cycle in Booster circuit 2,4 |
|---|---|---|---|
| 000 | 00h | BCLK / 1 | BCLK / 1 |
| 001 | 01h | BCLK / 1 | BCLK / 2 |
| 010 | 02h | BCLK / 1 | BCLK / 4 |
| 011 | 03h | BCLK / 2 | BCLK / 2 |
| 100 | 04h | BCLK / 2 | BCLK / 4 |
| 101 | 05h | BCLK / 4 | BCLK / 4 |
| 110 | 06h | BCLK / 4 | BCLK / 8 |
| 111 | 07h | BCLK / 4 | BCLK / 16 |

| | |
|---|---|
| Restriction | -If this register not using the register need be reserved. |

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In | Yes |

| Default | Status | Default Value |
|---|---|---|
| | | C2h |
| | Power On Sequence | 01h/01h |
| | S/W Reset | 01h/01h |
| | H/W Reset | 01h/01h |

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| | |
|---|---|
| Flow Chart |  |

### 10.2.9   PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

| C3H | | | | | | | | | | | | | PWCTR4 (Power Control 4) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PWCTR4 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | (C3h) |
| 1st parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | APB2 | APB1 | APB0 | |
| 2nd parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | DCB2 | DCB1 | DCB0 | |

| | |
|---|---|
| Description | -Set the amount of current in Operational amplifier in Idle mode/8 colors.<br>-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.<br><br><table><tr><td colspan="2">AP[2:0]</td><td>Amount of Current in Operational Amplifier</td></tr><tr><td>000</td><td>00h</td><td>Operation of the operational amplifier stops</td></tr><tr><td>001</td><td>01h</td><td>Small</td></tr><tr><td>010</td><td>02h</td><td>Medium Low</td></tr><tr><td>011</td><td>03h</td><td>Medium</td></tr><tr><td>100</td><td>04h</td><td>Medium High</td></tr><tr><td>101</td><td>05h</td><td>Large</td></tr><tr><td>110</td><td>06h</td><td>Reserved</td></tr><tr><td>111</td><td>07h</td><td>Reserved</td></tr></table><br>-Set the Booster circuit Step-up cycle in Idle mode/8 colors.<br><table><tr><td colspan="2">DC[2:0]</td><td>Step-up cycle in Booster circuit 1</td><td>Step-up cycle in Booster circuit 2,4</td></tr><tr><td>000</td><td>00h</td><td>BCLK / 1</td><td>BCLK / 1</td></tr><tr><td>001</td><td>01h</td><td>BCLK / 1</td><td>BCLK / 2</td></tr><tr><td>010</td><td>02h</td><td>BCLK / 1</td><td>BCLK / 4</td></tr><tr><td>011</td><td>03h</td><td>BCLK / 2</td><td>BCLK / 2</td></tr><tr><td>100</td><td>04h</td><td>BCLK / 2</td><td>BCLK / 4</td></tr><tr><td>101</td><td>05h</td><td>BCLK / 4</td><td>BCLK / 4</td></tr><tr><td>110</td><td>06h</td><td>BCLK / 4</td><td>BCLK / 8</td></tr><tr><td>111</td><td>07h</td><td>BCLK / 4</td><td>BCLK / 16</td></tr></table><br>Note: BCLK is Clock frequency for Booster circuit |
| Restriction | -If this register not using the register need be reserved. |
| Register Availability | <table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table> |
| Default | <table><tr><td>Status</td><td>Default Value</td></tr><tr><td></td><td>C3h</td></tr><tr><td>Power On Sequence</td><td>02h/07h</td></tr><tr><td>S/W Reset</td><td>02h/07h</td></tr><tr><td>H/W Reset</td><td>02h/07h</td></tr></table> |

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PWCTR4

1st Parameter
2nd parameter

**Legend**

Command

Parameter

Display

Action

Mode

Sequential
transter

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### 10.2.10 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

| C4H | | | | | | PWCTR5 (Power Control 5) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PWCTR5 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | (C4h) |
| 1st parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | APC2 | APC1 | APC0 | |
| 2nd parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | DCC2 | DCC1 | DCC0 | |

| Description | -Set the amount of current in Operational amplifier in Partial mode/ full-colors. |
|---|---|
| | -Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver. |

| AP[2:0] | | Amount of Current in Operational Amplifier |
|---|---|---|
| 000 | 00h | Operation of the operational amplifier stops |
| 001 | 01h | Small |
| 010 | 02h | Medium Low |
| 011 | 03h | Medium |
| 100 | 04h | Medium High |
| 101 | 05h | Large |
| 110 | 06h | Reserved |
| 111 | 07h | Reserved |

-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

| DC[2:0] | | Step-up cycle in Booster circuit 1 | Step-up cycle in Booster circuit 2,4 |
|---|---|---|---|
| 000 | 00h | BCLK / 1 | BCLK / 1 |
| 001 | 01h | BCLK / 1 | BCLK / 2 |
| 010 | 02h | BCLK / 1 | BCLK / 4 |
| 011 | 03h | BCLK / 2 | BCLK / 2 |
| 100 | 04h | BCLK / 2 | BCLK / 4 |
| 101 | 05h | BCLK / 4 | BCLK / 4 |
| 110 | 06h | BCLK / 4 | BCLK / 8 |
| 111 | 07h | BCLK / 4 | BCLK / 16 |

Note: BCLK is Clock frequency for Booster circuit

| Restriction | -If this register not using the register need be reserved. |
|---|---|

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In | Yes |

| Default | Status | Default Value |
|---|---|---|
| | | C4h |
| | Power On Sequence | 02h/04h |
| | S/W Reset | 02h/04h |
| | H/W Reset | 02h/04h |

| | |
|---|---|
| Flow Chart | PWCTR5 → 1st Parameter / 2nd parameter<br><br>**Legend**<br>Command<br>Parameter<br>Display<br>Action<br>Mode<br>Sequential transter |

## 10.2.11 VMCTR1 (C5h): VCOM Control 1

| C5H | VMCTR1 (VCOM Control 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| VMCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | (C5h) |
| 1st parameter | 1 | ↑ | 1 | - | - | VMH6 | VMH5 | VMH 4 | VMH 3 | VMH 2 | VMH 1 | VMH 0 | |
| 2nd parameter | 1 | ↑ | 1 | - | - | VML6 | VML5 | VML4 | VML3 | VML2 | VML1 | VML0 | |

Description

-Set VCOMH Voltage

| VMH[6:0] | | VCOMH | VMH[6:0] | | VCOMH | VMH[6:0] | | VCOMH | VMH[6:0] | | VCOMH |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000000 | 00h | 2.500 | 0011011 | 1Bh | 3.175 | 0110110 | 36h | 3.850 | 1010001 | 51h | 4.525 |
| 0000001 | 01h | 2.525 | 0011100 | 1Ch | 3.200 | 0110111 | 37h | 3.875 | 1010010 | 52h | 4.550 |
| 0000010 | 02h | 2.550 | 0011101 | 1Dh | 3.225 | 0111000 | 38h | 3.900 | 1010011 | 53h | 4.575 |
| 0000011 | 03h | 2.575 | 0011110 | 1Eh | 3.250 | 0111001 | 39h | 3.925 | 1010100 | 54h | 4.600 |
| 0000100 | 04h | 2.600 | 0011111 | 1Fh | 3.275 | 0111010 | 3Ah | 3.950 | 1010101 | 55h | 4.625 |
| 0000101 | 05h | 2.625 | 0100000 | 20h | 3.300 | 0111011 | 2Bh | 3.975 | 1010110 | 56h | 4.650 |
| 0000110 | 06h | 2.650 | 0100001 | 21h | 3.325 | 0111100 | 3Ch | 4.000 | 1010111 | 57h | 4.675 |
| 0000111 | 07h | 2.675 | 0100010 | 22h | 3.350 | 0111101 | 3Dh | 4.025 | 1011000 | 58h | 4.700 |
| 0001000 | 08h | 2.700 | 0100011 | 23h | 3.375 | 0111110 | 3Eh | 4.050 | 1011001 | 59h | 4.725 |
| 0001001 | 09h | 2.725 | 0100100 | 24h | 3.400 | 0111111 | 3Fh | 4.075 | 1011010 | 5Ah | 4.750 |
| 0001010 | 0Ah | 2.750 | 0100101 | 25h | 3.425 | 1000000 | 40h | 4.100 | 1011011 | 5Bh | 4.775 |
| 0001011 | 0Bh | 2.775 | 0100110 | 26h | 3.450 | 1000001 | 41h | 4.125 | 1011100 | 5Ch | 4.800 |
| 0001100 | 0Ch | 2.800 | 0100111 | 27h | 3.475 | 1000010 | 42h | 4.150 | 1011101 | 5Dh | 4.825 |
| 0001101 | 0Dh | 2.825 | 0101000 | 28h | 3.500 | 1000011 | 43h | 4.175 | 1011110 | 5Eh | 4.850 |
| 0001110 | 0Eh | 2.850 | 0101001 | 29h | 3.525 | 1000100 | 44h | 4.200 | 1011111 | 5Fh | 4.875 |
| 0001111 | 0Fh | 2.875 | 0101010 | 2Ah | 3.550 | 1000101 | 45h | 4.225 | 1100000 | 60h | 4.900 |
| 0010000 | 10h | 2.900 | 0101011 | 2Bh | 3.575 | 1000110 | 46h | 4.250 | 1100001 | 61h | 4.925 |
| 0010001 | 11h | 2.925 | 0101100 | 2Ch | 3.600 | 1000111 | 47h | 4.275 | 1100010 | 62h | 4.950 |
| 0010010 | 12h | 2.950 | 0101101 | 2Dh | 3.625 | 1001000 | 48h | 4.300 | 1100011 | 63h | 4.975 |
| 0010011 | 13h | 2.975 | 0101110 | 2Eh | 3.650 | 1001001 | 49h | 4.325 | 1100100 | 64h | 5.000 |
| 0010100 | 14h | 3.000 | 0101111 | 2Fh | 3.675 | 1001010 | 4Ah | 4.350 | 1100101 | 65h | Not Permitted |
| 0010101 | 15h | 3.025 | 0110000 | 30h | 3.700 | 1001011 | 4Bh | 4.375 | | | |
| 0010110 | 16h | 3.050 | 0110001 | 31h | 3.725 | 1001100 | 4Ch | 4.400 | 1111111 | 7Fh | |
| 0010111 | 17h | 3.075 | 0110010 | 32h | 3.750 | 1001101 | 4Dh | 4.425 | | | |
| 0011000 | 18h | 3.100 | 0110011 | 33h | 3.775 | 1001110 | 4Eh | 4.450 | | | |
| 0011001 | 19h | 3.125 | 0110100 | 34h | 3.800 | 1001111 | 4Fh | 4.475 | | | |
| 0011010 | 1Ah | 3.150 | 0110101 | 35h | 3.825 | 1010000 | 50h | 4.500 | | | |

# *ST7735*

-Set VCOML Voltage

| VML[6:0] | | VCOML | VML[6:0] | | VCOML | VML[6:0] | | VCOML | VML[6:0] | | VCOML |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000000 | 00h | | 0011011 | 1Bh | -1.825 | 0110110 | 36h | -1.150 | 1010001 | 51h | -0.475 |
| 0000001 | 01h | Not Permitted | 0011100 | 1Ch | -1.800 | 0110111 | 37h | -1.125 | 1010010 | 52h | -0.450 |
| 0000010 | 02h | | 0011101 | 1Dh | -1.775 | 0111000 | 38h | -1.100 | 1010011 | 53h | -0.425 |
| 0000011 | 03h | | 0011110 | 1Eh | -1.750 | 0111001 | 39h | -1.075 | 1010100 | 54h | -0.400 |
| 0000100 | 04h | -2.400 | 0011111 | 1Fh | -1.725 | 0111010 | 3Ah | -1.050 | 1010101 | 55h | -0.375 |
| 0000101 | 05h | -2.375 | 0100000 | 20h | -1.700 | 0111011 | 3Bh | -1.025 | 1010110 | 56h | -0.350 |
| 0000110 | 06h | -2.350 | 0100001 | 21h | -1.675 | 0111100 | 3Ch | -1.000 | 1010111 | 57h | -0.325 |
| 0000111 | 07h | -2.325 | 0100010 | 22h | -1.650 | 0111101 | 3Dh | -0.975 | 1011000 | 58h | -0.300 |
| 0001000 | 08h | -2.300 | 0100011 | 23h | -1.625 | 0111110 | 3Eh | -0.950 | 1011001 | 59h | -0.275 |
| 0001001 | 09h | -2.275 | 0100100 | 24h | -1.600 | 0111111 | 3Fh | -0.925 | 1011010 | 5Ah | -0.250 |
| 0001010 | 0Ah | -2.250 | 0100101 | 25h | -1.575 | 1000000 | 40h | -0.900 | 1011011 | 5Bh | -0.225 |
| 0001011 | 0Bh | -2.225 | 0100110 | 26h | -1.550 | 1000001 | 41h | -0.875 | 1011100 | 5Ch | -0.200 |
| 0001100 | 0Ch | -2.200 | 0100111 | 27h | -1.525 | 1000010 | 42h | -0.850 | 1011101 | 5Dh | -0.175 |
| 0001101 | 0Dh | -2.175 | 0101000 | 28h | -1.500 | 1000011 | 43h | -0.825 | 1011110 | 5Eh | -0.150 |
| 0001110 | 0Eh | -2.150 | 0101001 | 29h | -1.475 | 1000100 | 44h | -0.800 | 1011111 | 5Fh | -0.125 |
| 0001111 | 0Eh | -2.125 | 0101010 | 2Ah | -1.450 | 1000101 | 45h | -0.775 | 1100000 | 60h | -0.100 |
| 0010000 | 10h | -2.100 | 0101011 | 2Bh | -1.425 | 1000110 | 46h | -0.750 | 1100001 | 61h | -0.075 |
| 0010001 | 11h | -2.075 | 0101100 | 2Ch | -1.400 | 1000111 | 47h | -0.725 | 1100010 | 62h | -0.050 |
| 0010010 | 12h | -2.050 | 0101101 | 2Dh | -1.375 | 1001000 | 48h | -0.700 | 1100011 | 63h | -0.025 |
| 0010011 | 13h | -2.025 | 0101110 | 2Eh | -1.350 | 1001001 | 49h | -0.675 | 1100100 | 64h | 0.000 |
| 0010100 | 14h | -2.000 | 0101111 | 2Fh | -1.325 | 1001010 | 4Ah | -0.650 | 1100101 | 65h | Not Permitted |
| 0010101 | 15h | -1.975 | 0110000 | 30h | -1.300 | 1001011 | 4Bh | -0.625 | | \| | |
| 0010110 | 16h | -1.950 | 0110001 | 31h | -1.275 | 1001100 | 4Ch | -0.600 | 1111111 | 7Fh | |
| 0010111 | 17h | -1.925 | 0110010 | 32h | -1.250 | 1001101 | 4Dh | -0.575 | | | |
| 0011000 | 18h | -1.900 | 0110011 | 33h | -1.225 | 1001110 | 4Eh | -0.550 | | | |
| 0011001 | 19h | -1.875 | 0110100 | 34h | -1.200 | 1001111 | 4Fh | -0.525 | | | |
| 0011010 | 1Ah | -1.850 | 0110101 | 35h | -1.175 | 1010000 | 50h | -0.500 | | | |

**Restriction**

-If this register not using the register need be reserved.
-The VCOMAC = VCOMH – VCOML

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | C5h |
| Power On Sequence | 51h/4Dh |
| S/W Reset | 51h/4Dh |
| H/W Reset | 51h/4Dh |

# *ST7735*

| Flow Chart | |
|---|---|
| | VMCTR1 → 1st Parameter / 2nd parameter |
| | Legend: Command, Parameter, Display, Action, Mode, Sequential transter |

### 10.2.12 VMOFCTR (C7h): VCOM Offset Control

| C7H | VMOFCTR (VCOM Offset Control) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| VMOFCTR | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | (C7h) |
| Parameter | 1 | ↑ | 1 | - | - | - | - | VMF4 | VMF3 | VMF2 | VMF1 | VMF0 | |

| | |
|---|---|
| Description | -Set VCOM Voltage level for reduce the flicker issue<br><br>| VMF (hex) | VMF[4:0] | VCOMH,VCOML Output Level |<br>|---|---|---|<br>| 00h | 00000 | "VMH" -16d,"VML"-16d |<br>| 01h | 00001 | "VMH"-15d, "VML"-15d |<br>| 02h | 00010 | "VMH"-14d, "VML"-14d |<br>| \| | \| | \| |<br>| 0Eh | 01110 | "VMH"-2d, "VML"-2d |<br>| 0Fh | 01111 | "VMH"-1d, "VML"-1d |<br>| 10h | 10000 | "VMH", "VML" |<br>| 11h | 10001 | "VMH"+1d, "VML"+1d |<br>| 12h | 10010 | "VMH"+2d, "VML"+2d |<br>| \| | \| | \| |<br>| 1Eh | 11110 | "VMH"+14d, "VML"+14d |<br>| 1Fh | 11111 | "VMH"+15d, "VML"+15d |<br><br>- 1d=25mV, 2d=50mV 3d=75mv....<br><br>- 2.5V <= VMH ± nd <= 5.0V; -2. 5V <= VML ± nd<= 0V (n=0~15,16) |
| Restriction | -If this register not using the register need be reserved. |
| Register Availability | | Status | Availability |<br>|---|---|<br>| Normal Mode On, Idle Mode Off, Sleep Out | Yes |<br>| Normal Mode On, Idle Mode On, Sleep Out | Yes |<br>| Partial Mode On, Idle Mode Off, Sleep Out | Yes |<br>| Partial Mode On, Idle Mode On, Sleep Out | Yes |<br>| Sleep In | Yes | |
| Default | | Status | Default Value |<br>|---|---|<br>| | C7h |<br>| Power On Sequence | F0h |<br>| S/W Reset | F0h |<br>| H/W Reset | F0h | |
| Flow Chart |  |

## 10.2.13 WRID2 (D1h): Write ID2 Value

| D1H | | | | | | | | | | | | | WRID2 (Write ID2 Value) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| WRID2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | (D1h) |
| Parameter | 1 | ↑ | 1 | - | - | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | - |
| Description | -Write 7-bit data of LCD module version to save it to EEPROM. -The parameter ID2[6:0] is LCD Module version ID. | | | | | | | | | | | | |
| Flow Chart |  | | | | | | | | | | | | |

## 10.2.14 WRID3 (D2h): Write ID3 Value

| D2H | WRID3 (Write ID3 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| WRID3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | (D2h) |
| Parameter | 1 | ↑ | 1 | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | - |
| Description | -Write 8-bit data of project code module to save it to EEPROM.<br>-The parameter ID3[7:0] is product project ID. | | | | | | | | | | | | |
| Flow Chart |  | | | | | | | | | | | | |

### 10.2.15 PWCTR6 (FCh): Power Control 5 (in Partial mode + Idle mode)

| FCH | PWCTR6 (Gamma control adjust) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| PWCTR6 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | (FCh) |
| 1st parameter | 1 | ↑ | 1 | - | - | Sapa2 | Sapa1 | Sapa0 | - | Sapb2 | Sapb1 | Sapb0 | |
| 2nd parameter | 1 | ↑ | 1 | - | - | Sapc2 | Sapc1 | Sapc0 | - | DCD2 | DCD1 | DCD0 | |
| Description | -Set the amount of current in Operational amplifier in Partial mode + Idle mode. | | | | | | | | | | | | |

| | Status | Default Value |
|---|---|---|
| Default | | FCh |
| | Power On Sequence | 11h/15h |
| | S/W Reset | 11h/15h |
| | H/W Reset | 11h/15h |

**Flow Chart**

PWCTR6

1st Parameter
2nd parameter

Legend

Command

Parameter

Display

Action

Mode

Sequential transter

### 10.2.16 NVFCTR1 (D9h): EEPROM Control Status

| D9H | NVFCTR1 (NV Memory Function Controller 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| NVFCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | (D9h) |
| parameter | 1 | 1 | ↑ | - | 0 | 0 | VMF_EN | ID2_EN | 0 | 0 | 0 | 0 | |

| Description | -EEPROM control status | |
|---|---|---|
| | **Bit** | **Value** |
| | VMF_EN | "1" = Command C7h enable ; "0" = Command C7h disable |
| | ID2_EN | "1" = Command D1h enable ; "0" = Command D1h disable |

| Default | Status | Default Value |
|---|---|---|
| | | D9h |
| | Power On Sequence | 00h |
| | S/W Reset | 00h |
| | H/W Reset | 00h |

| Flow Chart | |
|---|---|

### 10.2.17 NVFCTR2 (DEh): EEPROM Read Command

| DEH | NVFCTR1 (NV Memory Function Controller 2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| NVFCTR2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | (DEh) |
| parameter | 1 | ↑ | 1 | | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5 |
| Description | EEPROM Read Command<br><br>NOTE: "-" Don't care | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | |

NVCTR2

1st Parameter :
A5h

Legend

Command

Parameter

Display

Action

Mode

Sequential
transfer

### 10.2.18 NVFCTR3 (DFh): EEPROM Write Command

| DFH | NVFCTR1 (NV Memory Function Controller 3 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| NVFCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | (DFh) |
| 1st parameter | 1 | ↑ | 1 | | EE_IB7 | EE_IB6 | EE_IB5 | EE_IB4 | EE_IB3 | EE_IB2 | EE_IB1 | EE_IB0 | |
| 2nd parameter | 1 | ↑ | 1 | | EE_CMD7 | EE_CMD6 | EE_CMD5 | EE_CMD4 | EE_CMD3 | EE_CMD2 | EE_CMD1 | EE_CMD0 | |
| 3rd parameter | 1 | ↑ | 1 | | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5 |
| Description | -EEPROM Write Command<br><br>-EE_IB[7:0] : Select Command. ; ADDR: C7h, D1h, D2h ; Select all: AAh<br><br>-EE_CMD[7:0] : Select to Program/Erase ; Program command : 3Ah ; Erase command : C5h<br><br>NOTE: "-" Don't care | | | | | | | | | | | | |
| Flow Chart |  | | | | | | | | | | | | |

### 10.2.19 GMCTRP1 (E0h): Gamma ('+'polarity) Correction Characteristics Setting

| E0H | | | | | | | GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| GMCTRP1 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | (E0h) |
| 1st parameter | 1 | ↑ | 1 | - | - | - | VRF0P[5] | VRF0P[4] | VF0P[3] | VRF0P[2] | VRF0P[1] | VRF0P[0] | |
| 2nd parameter | 1 | ↑ | 1 | - | - | - | VOS0P[5] | VOS0P[4] | VOS0P[3] | VOS0P[2] | VOS0P[1] | VOS0P[0] | |
| 3rd parameter | 1 | ↑ | 1 | - | - | - | PK0P[5] | PK0P[4] | PK0P[3] | PK0P[2] | PK0P[1] | PK0P[0] | |
| 4th parameter | 1 | ↑ | 1 | - | - | - | PK1P[5] | PK1P[4] | PK1P[3] | PK1P[2] | PK1P[1] | PK1P[0] | |
| 5th parameter | 1 | ↑ | 1 | - | - | - | PK2P[5] | PK2P[4] | PK2P[3] | PK2P[2] | PK2P[1] | PK2P[0] | |
| 6th parameter | 1 | ↑ | 1 | - | - | - | PK3P[5] | PK3P[4] | PK3P[3] | PK3P[2] | PK3P[1] | PK3P[0] | |
| 7th parameter | 1 | ↑ | 1 | - | - | - | PK4P[5] | PK4P[4] | PK4P[3] | PK4P[2] | PK4P[1] | PK4P[0] | |
| 8th parameter | 1 | ↑ | 1 | - | - | - | PK5P[5] | PK5P[4] | PK5P[3] | PK5P[2] | PK5P[1] | PK5P[0] | |
| 9th parameter | 1 | ↑ | 1 | - | - | - | PK6P[5] | PK6P[4] | PK6P[3] | PK6P[2] | PK6P[1] | PK6P[0] | |
| 10th parameter | 1 | ↑ | 1 | - | - | - | PK7P[5] | PK7P[4] | PK7P[3] | PK7P[2] | PK7P[1] | PK7P[0] | |
| 11th parameter | 1 | ↑ | 1 | - | - | - | PK8P[5] | PK8P[4] | PK8P[3] | PK8P[2] | PK8P[1] | PK8P[0] | |
| 12th parameter | 1 | ↑ | 1 | - | - | - | PK9P[5] | PK9P[4] | PK9P[3] | PK9P[2] | PK9P[1] | PK9P[0] | |
| 13th parameter | 1 | ↑ | 1 | - | - | - | SELV0P[5] | SELV0P[4] | SELV0P[3] | SELV0P[2] | SELV0P[1] | SELV0P[0] | |
| 14th parameter | 1 | ↑ | 1 | - | - | - | SELV1P[5] | SELV1P[4] | SELV1P[3] | SELV1P[2] | SELV1P[1] | SELV1P[0] | |
| 15th parameter | 1 | ↑ | 1 | - | - | - | SELV62P[5] | SELV62P[4] | SELV62P[3] | SELV62P[2] | SELV62P[1] | SELV62P[0] | |
| 16th parameter | 1 | ↑ | 1 | - | - | - | SELV63P[5] | SELV63P[4] | SELV63P[3] | SELV63P[2] | SELV63P[1] | SELV63P[0] | |

| Description | Register Group | Positive Polarity | Set-up Contents |
|---|---|---|---|
| | High level adjustment | VRF0P[5:0] | Variable resistor VRHP |
| | Mid level adjustment | SELV0P[5:0] | The voltage of V0 grayscale is selected by the 64 to 1 selector |
| | | SELV1P[5:0] | The voltage of V1 grayscale is selected by the 64 to 1 selector |
| | | PK0P[5:0] | The voltage of V3 grayscale is selected by the 64 to 1 selector |
| | | PK1P[5:0] | The voltage of V6 grayscale is selected by the 64 to 1 selector |
| | | PK2P[5:0] | The voltage of V11 grayscale is selected by the 64 to 1 selector |
| | | PK3P[5:0] | The voltage of V19 grayscale is selected by the 64 to 1 selector |
| | | PK4P[5:0] | The voltage of V27 grayscale is selected by the 64 to 1 selector |
| | | PK5P[5:0] | The voltage of V36 grayscale is selected by the 64 to 1 selector |
| | | PK6P[5:0] | The voltage of V44 grayscale is selected by the 64 to 1 selector |
| | | PK7P[5:0] | The voltage of V52 grayscale is selected by the 64 to 1 selector |
| | | PK8P[5:0] | The voltage of V57 grayscale is selected by the 64 to 1 selector |
| | | PK9P[5:0] | The voltage of V60 grayscale is selected by the 64 to 1 selector |
| | | SELV62P[5:0] | The voltage of V62 grayscale is selected by the 64 to 1 selector |
| | | SELV63P[5:0] | The voltage of V63 grayscale is selected by the 64 to 1 selector |
| | Low level adjustment | VOS0P[5:0] | Variable resistor VRLP |

Flow Chart

GMCTRP1

1st Parameter
2nd Parameter
|

Legend

Command

Parameter

Display

Action

Mode

Sequential
transter
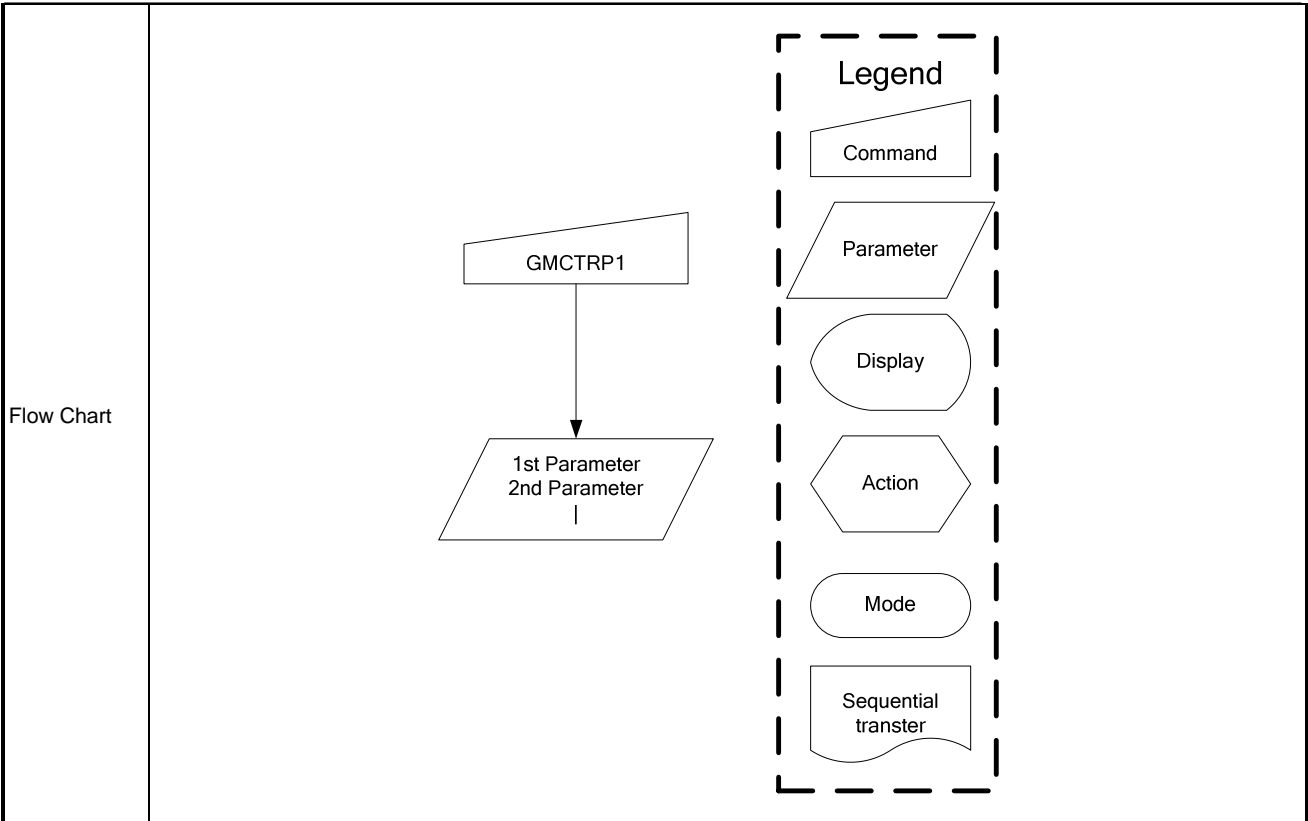
## 10.2.20 GMCTRN1 (E1h): Gamma '-'polarity Correction Characteristics Setting
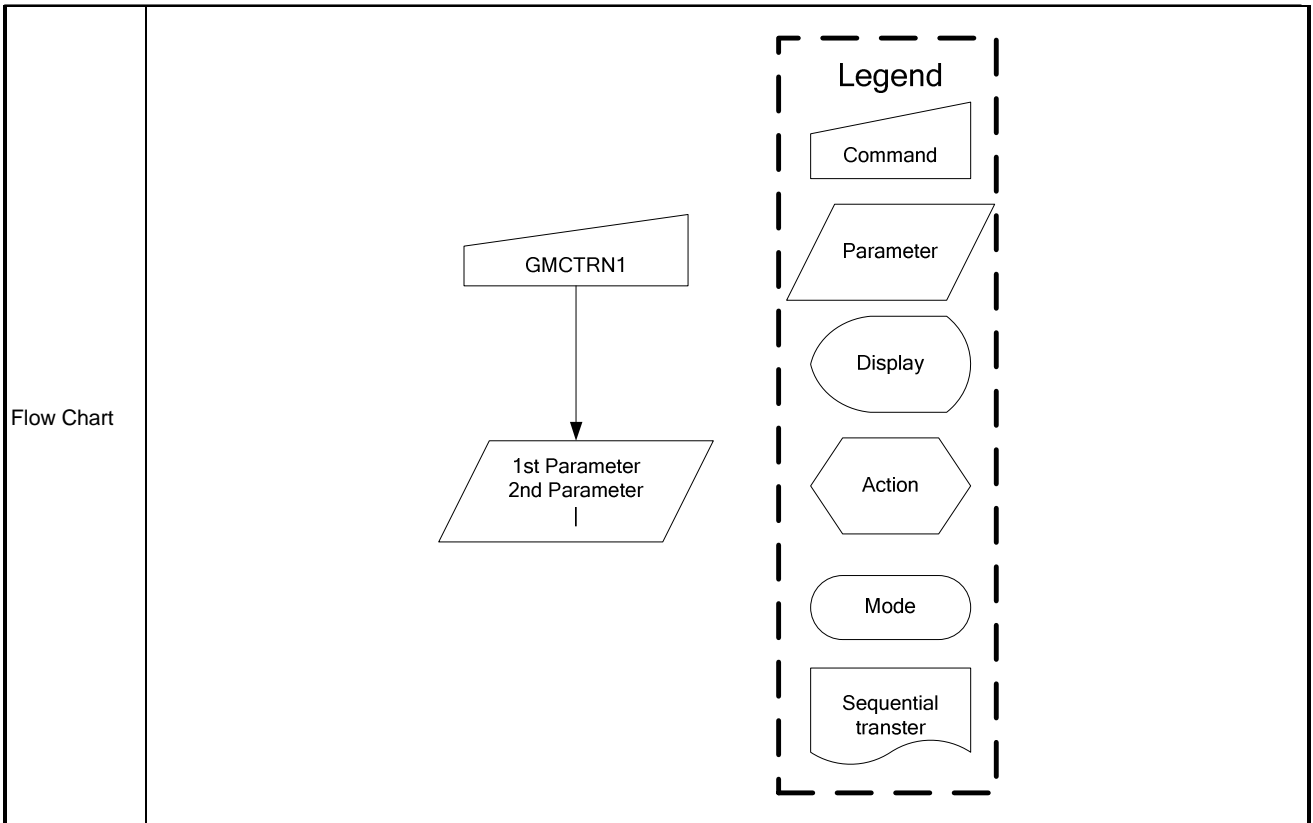
| E1H | | | | | GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting) | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| GMCTRP1 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | (E1h) |
| 1$^{st}$ parameter | 1 | ↑ | 1 | - | - | - | VRF0N[5] | VRF0N[4] | VF0N[3] | VRF0N[2] | VRF0N[1] | VRF0N[0] | |
| 2$^{nd}$ parameter | 1 | ↑ | 1 | - | - | - | VOS0N[5] | VOS0N[4] | VOS0N[3] | VOS0N[2] | VOS0N[1] | VOS0N[0] | |
| 3$^{rd}$ parameter | 1 | ↑ | 1 | - | - | - | PK0N[5] | PK0N[4] | PK0N[3] | PK0N[2] | PK0N[1] | PK0N[0] | |
| 4$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK1N[5] | PK1N[4] | PK1N[3] | PK1N[2] | PK1N[1] | PK1N[0] | |
| 5$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK2N[5] | PK2N[4] | PK2N[3] | PK2N[2] | PK2N[1] | PK2N[0] | |
| 6$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK3N[5] | PK3N[4] | PK3N[3] | PK3N[2] | PK3N[1] | PK3N[0] | |
| 7$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK4N[5] | PK4N[4] | PK4N[3] | PK4N[2] | PK4N[1] | PK4N[0] | |
| 8$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK5N[5] | PK5N[4] | PK5N[3] | PK5N[2] | PK5N[1] | PK5N[0] | |
| 9$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK6N[5] | PK6N[4] | PK6N[3] | PK6N[2] | PK6N[1] | PK6N[0] | |
| 10$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK7N[5] | PK7N[4] | PK7N[3] | PK7N[2] | PK7N[1] | PK7N[0] | |
| 11$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK8N[5] | PK8N[4] | PK8N[3] | PK8N[2] | PK8N[1] | PK8N[0] | |
| 12$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | PK9[5] | PK9N[4] | PK9N[3] | PK9N[2] | PK9N[1] | PK9N[0] | |
| 13$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | SELV0N[5] | SELV0N[4] | SELV0N[3] | SELV0N[2] | SELV0N[1] | SELV0N[0] | |
| 14$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | SELV1N[5] | SELV1N[4] | SELV1N[3] | SELV1N[2] | SELV1N[1] | SELV1N[0] | |
| 15$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | SELV62N[5] | SELV62N[4] | SELV62N[3] | SELV62N[2] | SELV62N[1] | SELV62N[0] | |
| 16$^{th}$ parameter | 1 | ↑ | 1 | - | - | - | SELV63N[5] | SELV63N[4] | SELV63N[3] | SELV63N[2] | SELV63N[1] | SELV63N[0] | |

| Description | Register Group | Negative Polarity | Set-up Contents |
|-------------|----------------|-------------------|-----------------|
| | High level adjustment | VRF0N[5:0] | Variable resistor VRHN |
| | Mid level adjustment | SELV0N[5:0] | The voltage of V0 grayscale is selected by the 64 to 1 selector |
| | | SELV1N[5:0] | The voltage of V1 grayscale is selected by the 64 to 1 selector |
| | | PK0N[5:0] | The voltage of V3 grayscale is selected by the 64 to 1 selector |
| | | PK1N[5:0] | The voltage of V6 grayscale is selected by the 64 to 1 selector |
| | | PK2N[5:0] | The voltage of V11 grayscale is selected by the 64 to 1 selector |
| | | PK3N[5:0] | The voltage of V19 grayscale is selected by the 64 to 1 selector |
| | | PK4N[5:0] | The voltage of V27 grayscale is selected by the 64 to 1 selector |
| | | PK5N[5:0] | The voltage of V36 grayscale is selected by the 64 to 1 selector |
| | | PK6N[5:0] | The voltage of V44 grayscale is selected by the 64 to 1 selector |
| | | PK7N[5:0] | The voltage of V52 grayscale is selected by the 64 to 1 selector |
| | | PK8N[5:0] | The voltage of V57 grayscale is selected by the 64 to 1 selector |
| | | PK9N[5:0] | The voltage of V60 grayscale is selected by the 64 to 1 selector |
| | | SELV62N[5:0] | The voltage of V62 grayscale is selected by the 64 to 1 selector |
| | | SELV63N[5:0] | The voltage of V63 grayscale is selected by the 64 to 1 selector |
| | Low level adjustment | VOS0N[5:0] | Variable resistor VRLN |

| | |
|---|---|
| Flow Chart | Legend<br><br>GMCTRN1 → 1st Parameter / 2nd Parameter<br><br>Command<br>Parameter<br>Display<br>Action<br>Mode<br>Sequential transter |

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### 10.2.21 EXTCTRL (F0h): Extension Command Control

| F0H | EXTCTRL (Extension command control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| EXTCTRL | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | (F0h) |
| parameter | 1 | ↑ | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (01h) |
| Description | When EXTC PIN ="L", this command will enable extension command. <br><br> NOTE: "-" Don't care | | | | | | | | | | | | |
| Flow Chart |  | | | | | | | | | | | | |

### 10.2.22 VCOM4L (FFh): Vcom 4 Level Control

| FFH | VCOM4L (Vcom 4 level control) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| VCOM4L | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (FFh) |
| Parameter1 | 1 | ↑ | 1 | - | TC2[3] | TC2[2] | TC2[1] | TC2[0] | TC1[3] | TC1[2] | TC1[1] | TC1[0] | |
| Parameter2 | 1 | ↑ | 1 | - | - | - | - | - | TC3[3] | TC3[2] | TC3[1] | TC3[0] | |
| Parameter3 | 1 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | (1Ah) |
| Description | | | | | | | | | | | | | |

| TC1[3:0] | Delay time | TC2[3:0] | Delay time | TC3[3:0] | Delay time |
|---|---|---|---|---|---|
| 0000 | 0 clock | 0000 | 0 clock | 0000 | 0 clock |
| 0001 | 1 clock | 0001 | 1 clock | 0001 | 1 clock |
| 0010 | 2 clock | 0010 | 2 clock | 0010 | 2 clock |
| 0011 | 3 clock | 0011 | 3 clock | 0011 | 3 clock |
| 0100 | 4 clock | 0100 | 4 clock | 0100 | 4 clock |
| 0101 | 5 clock | 0101 | 5 clock | 0101 | 5 clock |
| 0110 | 6 clock | 0110 | 6 clock | 0110 | 6 clock |
| 0111 | 7 clock | 0111 | 7 clock | 0111 | 7 clock |
| 1000 | 8 clock | 1000 | 8 clock | 1000 | 8 clock |
| 1001 | 9 clock | 1001 | 9 clock | 1001 | 9 clock |
| 1010 | 10 clock | 1010 | 10 clock | 1010 | 10 clock |
| 1011 | 11 clock | 1011 | 11 clock | 1011 | 11 clock |
| 1100 | 12 clock | 1100 | 12 clock | 1100 | 12 clock |
| 1101 | 13 clock | 1101 | 13 clock | 1101 | 13 clock |
| 1110 | 14 clock | 1110 | 14 clock | 1110 | 14 clock |
| 1111 | 15 clock | 1111 | 15 clock | 1111 | 15 clock |

NOTE: "-" Don't care

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| | |
|---|---|
| Flow Chart | <br><br>**Legend**<br><br>Command<br><br>Parameter<br><br>Display<br><br>Action<br><br>Mode<br><br>Sequential transter<br><br>VCOM4L<br><br>1st Parameter : TC2,TC1<br><br>2nd Parameter : TC3<br><br>3rd Parameter : 1Ah |

# *ST7735*
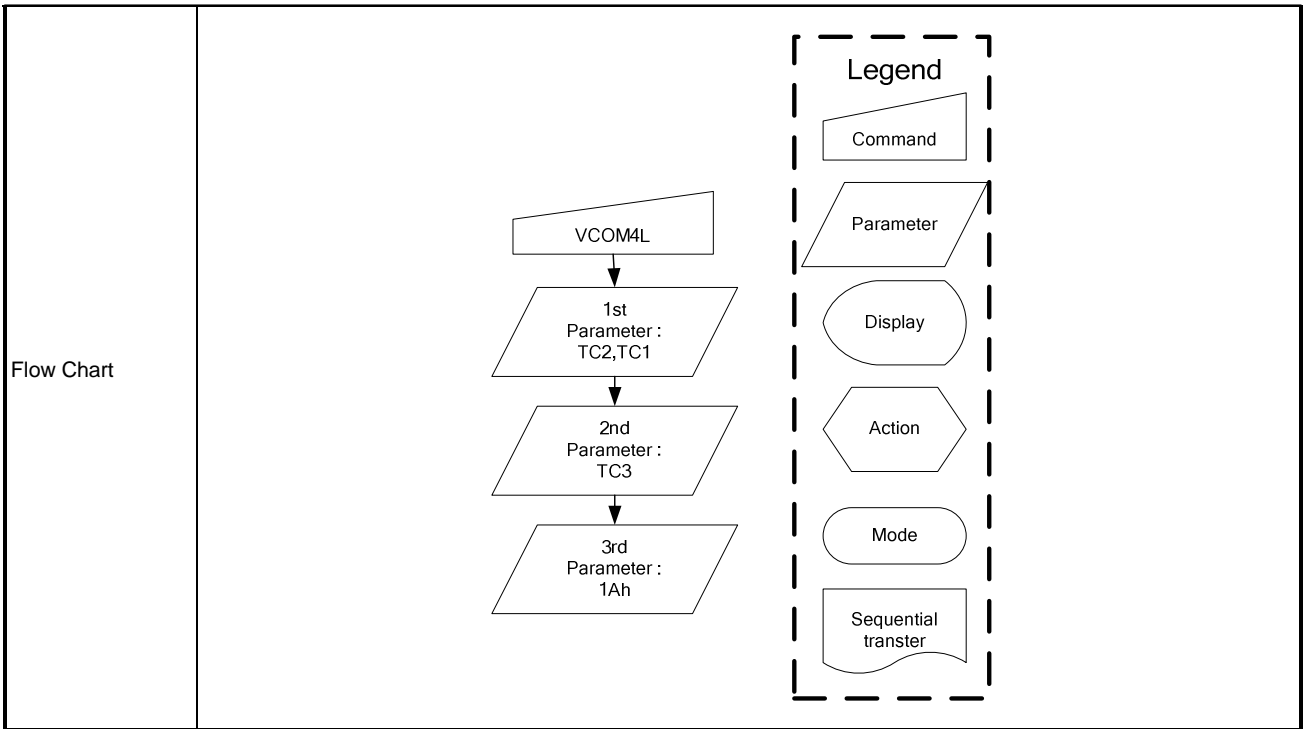
## 11  Power structure

### 11.1 Driver IC Operating Voltage Specification
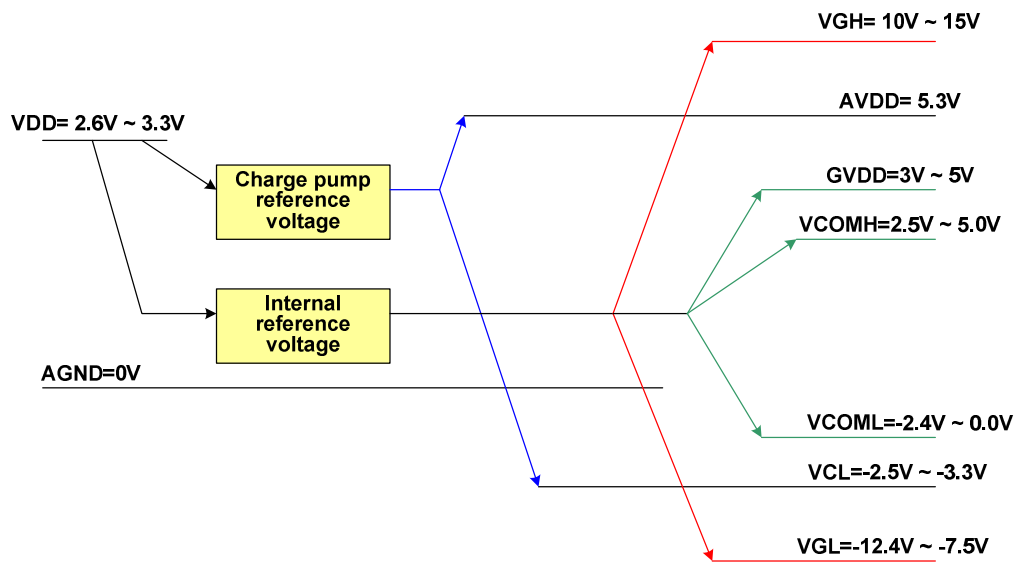


Fig 11.1.1 Power Booster Level

## 11.2 Power Booster Circuit

## 11.2.1 EXTERNAL COMPONENTS CONNECTION

| Pad Name | Connection | Rated (Min) Voltage | Typical capacitance value |
|---|---|---|---|
| VDDI | VDDI (Logic Power) | 6.3V | 1.0 uF |
| VDD | VDD (Analog Power) | 6.3V | 1.0 uF |
| VCC | Connect to Capacitor: VCC -------||------- GND | 6.3V | 1.0 uF |
| C41P, C41N | Connect to Capacitor: C41P -------||--- -----C41N | 6.3V | 1.0 uF |
| C22P, C22N | Connect to Capacitor: C22P -------||--------C22N | 25.0V; 16.0V* | 0.1 uF |
| C23P, C23N | Connect to Capacitor: C23P -------||--- -----C23N | 25.0V; 16.0V* | 0.1 uF |
| C11P, C11N | Connect to Capacitor: C11P -------||--------C11N | 6.3V | 1.0 uF |
| AVDD | Connect to Capacitor: AVDD -------||------- GND | 6.3V | 1.0 uF |
| VGH | Connect to Capacitor: VGH -------||------- GND | 25.0V; 16.0V* | 0.1 uF |
| VGL | Connect to Capacitor: VGL -------||------- GND | 25.0V; 16.0V* | 0.1 uF |
| VCL | Connect to Capacitor: VCL -------||------- GND | 6.3V | 1.0 uF |
| VCOMH | Connect to Capacitor: VCOMH-------||--------- GND | 6.3V | 1.0 uF |
| VCOML | Connect to Capacitor: VCOML -------||------- GND | 6.3V | 1.0 uF |

*Note: For the typical specification of capacitor, the surge voltage is 125% of rated voltage. The capacitor of rated voltage of 16V can be only used for the case of VGH < 12.8V and VGL > -12.8V to prevent from stability issue. For normal usage, please use the capacitor of 25V rating.*

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## 12  Gamma structure

### 12.1 TRUCTURE OF GRAYSCALE AMPLIFIER

The structure of grayscale amplifier is shown as below. 16 voltage levels (VIN0-VIN15) between GVDD and VGS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.
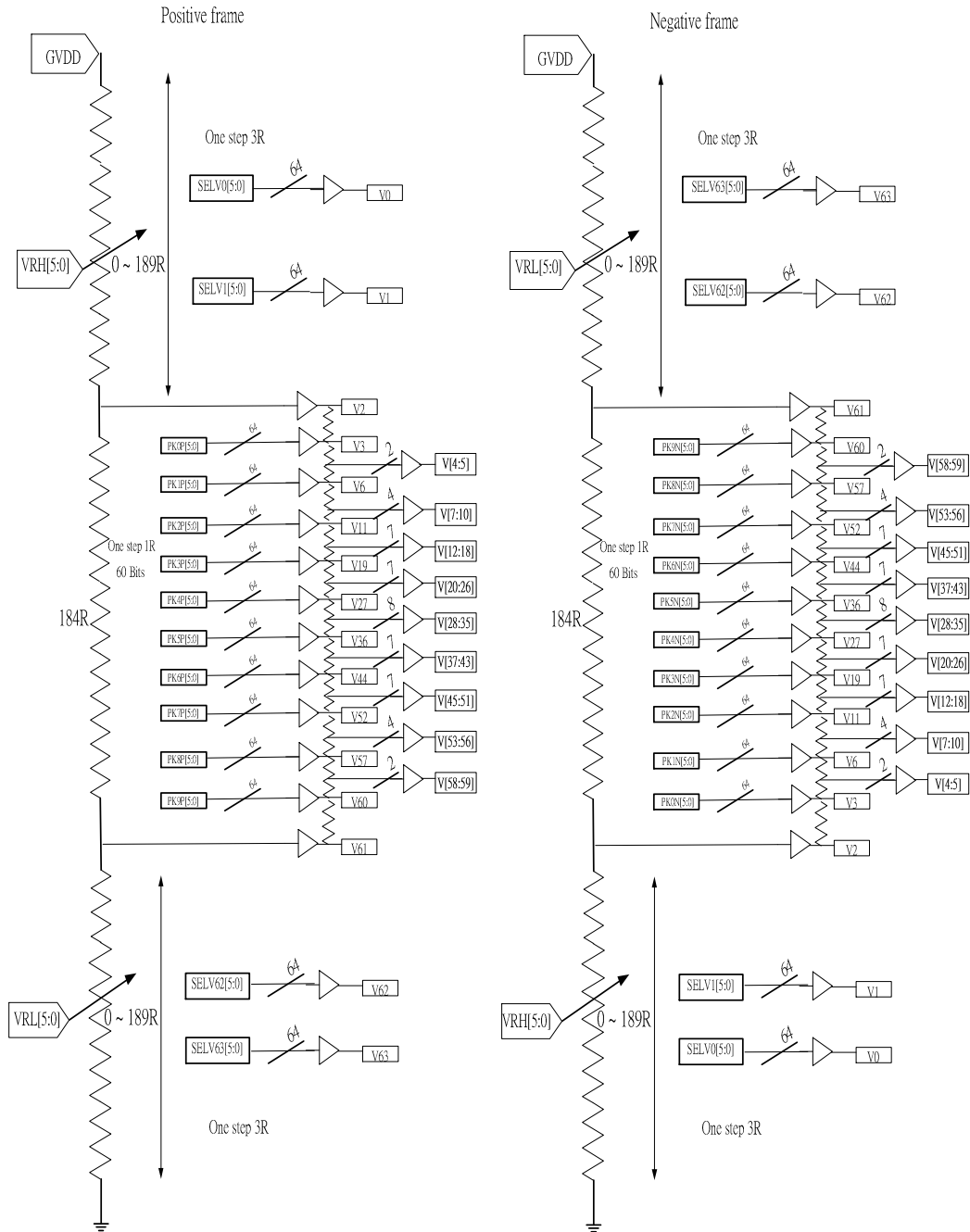
**12.2 Gamma Voltage Formula (Positive/ Negative Polarity)**

| Gray Level | Voltage Formula (Positive) | Voltage Formula (Negative) |
| --- | --- | --- |
| 0 | VINP0 | VINN0 |
| 1 | VINP1 | VINN1 |
| 2 | VINP2 | VINN2 |
| 3 | VINP3 | VINN3 |
| 4 | V3-(V3-V6)*(11/30) | V3-(V3-V6)*(11/30) |
| 5 | V3-(V3-V6)*(21/30) | V3-(V3-V6)*(21/30) |
| 6 | VINP4 | VINN4 |
| 7 | V6-(V6-V11)*(7/30) | V6-(V6-V11)*(7/30) |
| 8 | V6-(V6-V11)*(14/30) | V6-(V6-V11)*(14/30) |
| 9 | V6-(V6-V11)*(20/30) | V6-(V6-V11)*(20/30) |
| 10 | V6-(V6-V11)*(25/30) | V6-(V6-V11)*(25/30) |
| 11 | VINP5 | VINN5 |
| 12 | V11-(V11-V19)*(4/32) | V11-(V11-V19)*(4/32) |
| 13 | V11-(V11-V19)*(8/32) | V11-(V11-V19)*(8/32) |
| 14 | V11-(V11-V19)*(12/32) | V11-(V11-V19)*(12/32) |
| 15 | V11-(V11-V19)*(16/32) | V11-(V11-V19)*(16/32) |
| 16 | V11-(V11-V19)*(20/32) | V11-(V11-V19)*(20/32) |
| 17 | V11-(V11-V19)*(24/32) | V11-(V11-V19)*(24/32) |
| 18 | V11-(V11-V19)*(28/32) | V11-(V11-V19)*(28/32) |
| 19 | VINP6 | VINN6 |
| 20 | V19-(V19-V27)*(4/32) | V19-(V19-V27)*(4/32) |
| 21 | V19-(V19-V27)*(8/32) | V19-(V19-V27)*(8/32) |
| 22 | V19-(V19-V27)* (12/32) | V19-(V19-V27)* (12/32) |
| 23 | V19-(V19-V27)* (1632/) | V19-(V19-V27)* (1632/) |
| 24 | V19-(V19-V27)* (20/32) | V19-(V19-V27)* (20/32) |
| 25 | V19-(V19-V27)* (24/32) | V19-(V19-V27)* (24/32) |
| 26 | V19-(V19-V27)* (28/32) | V19-(V19-V27)* (28/32) |
| 27 | VINP7 | VINN7 |
| 28 | V27-(V27-V36)* (4/36) | V27-(V27-V36)* (4/36) |
| 29 | V27-(V27-V36)* (8/36) | V27-(V27-V36)* (8/36) |
| 30 | V27-(V27-V36)* (12/36) | V27-(V27-V36)* (12/36) |
| 31 | V27-(V27-V36)* (16/36) | V27-(V27-V36)* (16/36) |
| 32 | V27-(V27-V36)* (20/36) | V27-(V27-V36)* (20/36) |
| 33 | V27-(V27-V36)* (24/36) | V27-(V27-V36)* (24/36) |
| 34 | V27-(V27-V36)* (28/36) | V27-(V27-V36)* (28/36) |
| 35 | V27-(V27-V36)* (32/36) | V27-(V27-V36)* (32/36) |
| 36 | VINP8 | VINN8 |
| 37 | V36-(V36-V44)*(4/32) | V36-(V36-V44)*(4/32) |
| 38 | V36-(V36-V44)*(8/32) | V36-(V36-V44)*(8/32) |
| 39 | V36-(V36-V44)*(12/32) | V36-(V36-V44)*(12/32) |

| 40 | V36-(V36-V44)*(16/32) | V36-(V36-V44)*(16/32) |
| --- | --- | --- |
| 41 | V36-(V36-V44)*(20/32) | V36-(V36-V44)*(20/32) |
| 42 | V36-(V36-V44)*(24/32) | V36-(V36-V44)*(24/32) |
| 43 | V36-(V36-V44)*(28/32) | V36-(V36-V44)*(28/32) |
| 44 | VINP9 | VINN9 |
| 45 | V44-(V44-V52)*(4/32) | V44-(V44-V52)*(4/32) |
| 46 | V44-(V44-V52)*(8/32) | V44-(V44-V52)*(8/32) |
| 47 | V44-(V44-V52)*(12/32) | V44-(V44-V52)*(12/32) |
| 48 | V44-(V44-V52)*(16/32) | V44-(V44-V52)*(16/32) |
| 49 | V44-(V44-V52)*(20/32) | V44-(V44-V52)*(20/32) |
| 50 | V44-(V44-V52)*(24/32) | V44-(V44-V52)*(24/32) |
| 51 | V44-(V44-V52)*(28/32) | V44-(V44-V52)*(28/32) |
| 52 | VINP10 | VINN10 |
| 53 | V52-(V52-V57)*(5/30) | V52-(V52-V57)*(5/30) |
| 54 | V52-(V52-V57)*(11/30) | V52-(V52-V57)*(11/30) |
| 55 | V52-(V52-V57)*(17/30) | V52-(V52-V57)*(17/30) |
| 56 | V52-(V52-V57)*(23/30) | V52-(V52-V57)*(23/30) |
| 57 | VINP11 | VINN11 |
| 58 | V57-(V57-V60)*(8/30) | V57-(V57-V60)*(8/30) |
| 59 | V57-(V57-V60)*(18/30) | V57-(V57-V60)*(18/30) |
| 60 | VINP12 | VINN12 |
| 61 | VINP13 | VINN13 |
| 62 | VINP14 | VINN14 |
| 63 | VINP15 | VINN15 |

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## 13 Example Connection with Panel direction and Different Resolution

### 13.1 Application of connection with panel direction

Case 1: (This is default case)
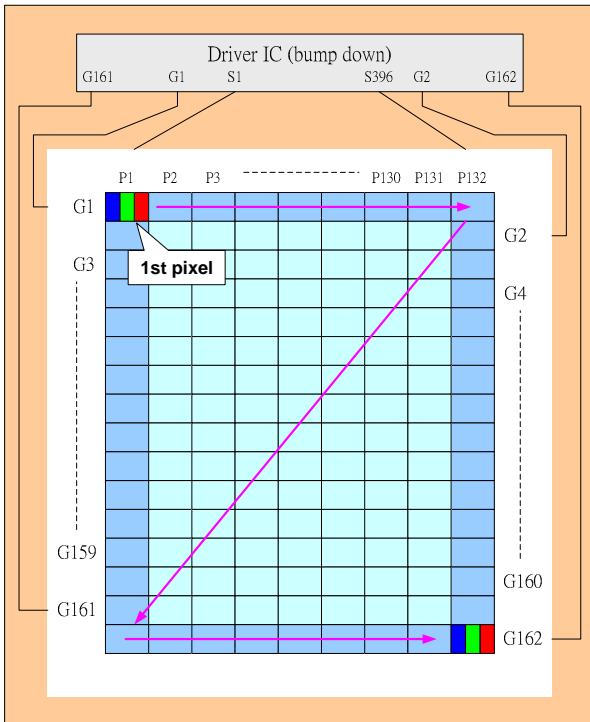- 1<sup>st</sup> Pixel is at Left Top of the panel
- RGB filter order = RGB
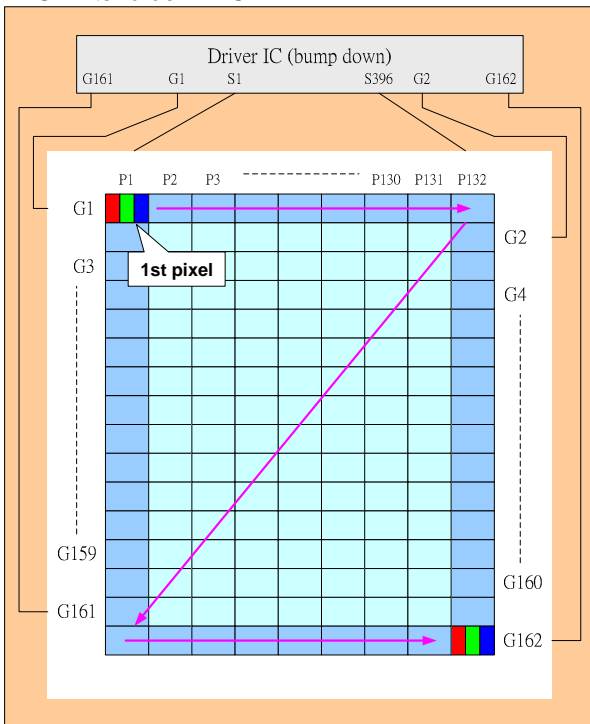


- Direction default setting (H/W)

SMX = ' 0'

SMY = '0'

SRGB = '0'

S1 = Filter R

S2 = Filter G

S3 = Filter B

- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



Case 2:
- 1<sup>st</sup> Pixel is at Left Top of the panel
- RGB filter order = BGR



- Direction default setting (H/W)

SMX = ' 0'

SMY = '0'

SRGB = '1'

S1 = Filter B

S2 = Filter G

S3 = Filter R

- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

Case 3:
- 1<sup>st</sup> Pixel is at Righ Bottom of the panel
- RGB filter order = RGB



- Direction default setting (H/W)
SMX = ' 1'
SMY = '1'
SRGB = '0'
S1 = Filter R
S2 = Filter G
S3 = Filter B
- Display direction control (S/W)
- X-Mirror control by MX
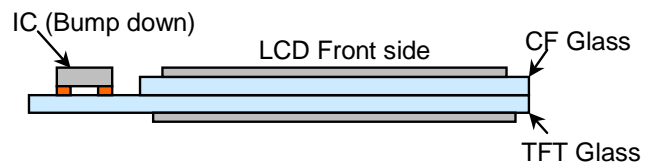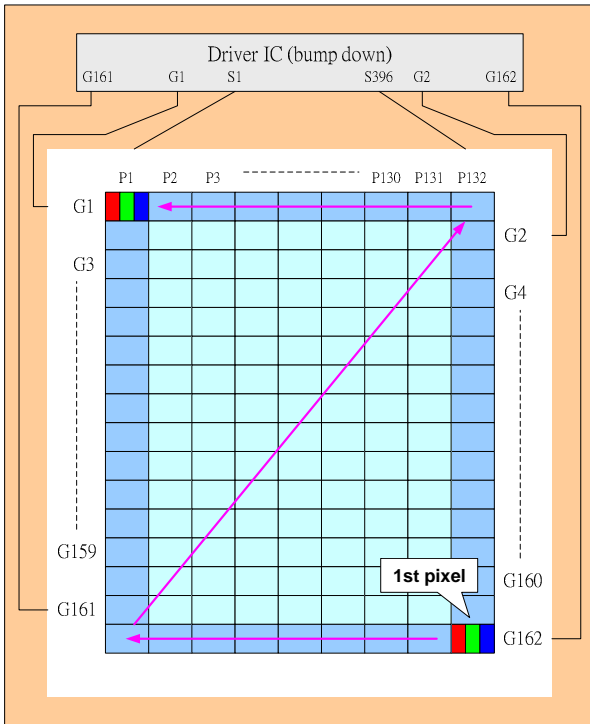- Y-Mirror control by MY
- XY-Exchange control by MV

Case 4:
- 1<sup>st</sup> Pixel is at Righ Bottom of the panel
- RGB filter order = BGR



- Direction default setting (H/W)
SMX = '1'
SMY = '1'
SRGB = '1'
S1 = Filter B
S2 = Filter G
S3 = Filter R
- Display direction control (S/W)
- X-Mirror control by MX
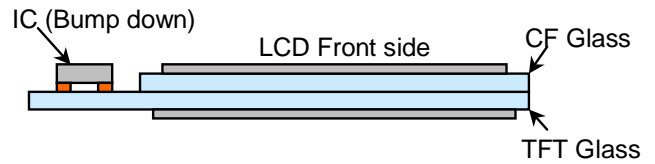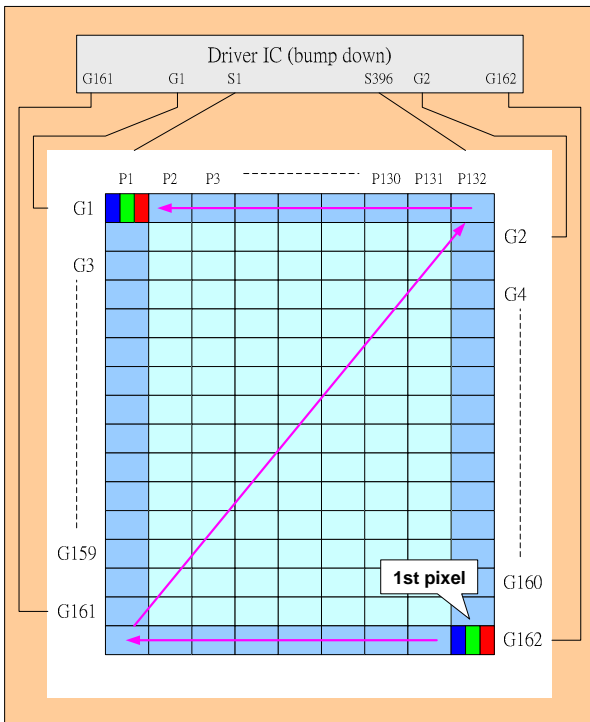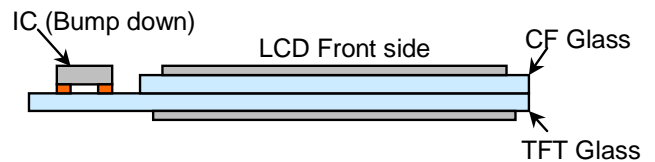- Y-Mirror control by MY
- XY-Exchange control by MV

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## 13.2 Application of connection with Different resolution

Case1 of Resolution (128RGB x 160) (GM[2:0] = "011")
RAM size=128 x 160 x 18-bit (Used)
Display size = 128RGB x 160

### 1). Example for SMX=SMY='0'

GRAM  size = 128 x 160 x 18-bits

- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

- Direction default setting (H/W)
  SMX = '0'
  SMY = '0'
  SRGB = '0'

### 2). Example for SMX=SMY='1'

GRAM  size  = 128  x  160  x  18-bits

- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

- Direction default setting (H/W)
  SMX = ' 1'
  SMY = ' 1'
  SRGB = '0'
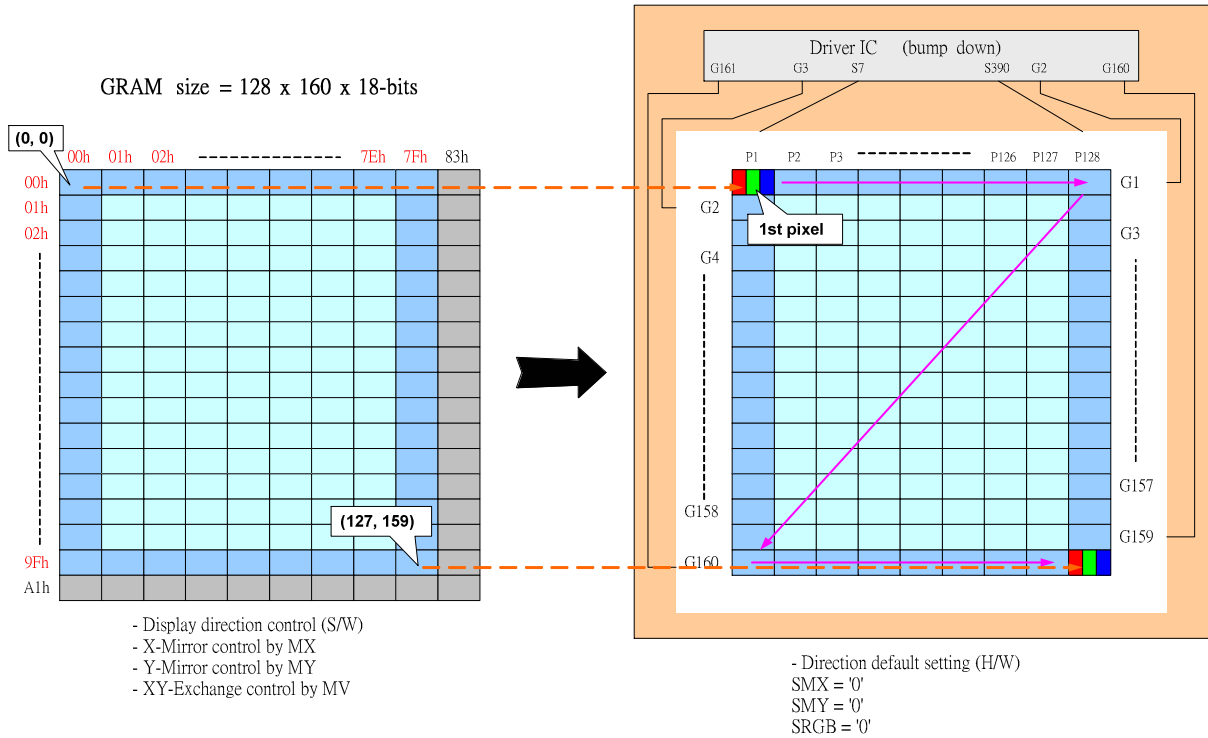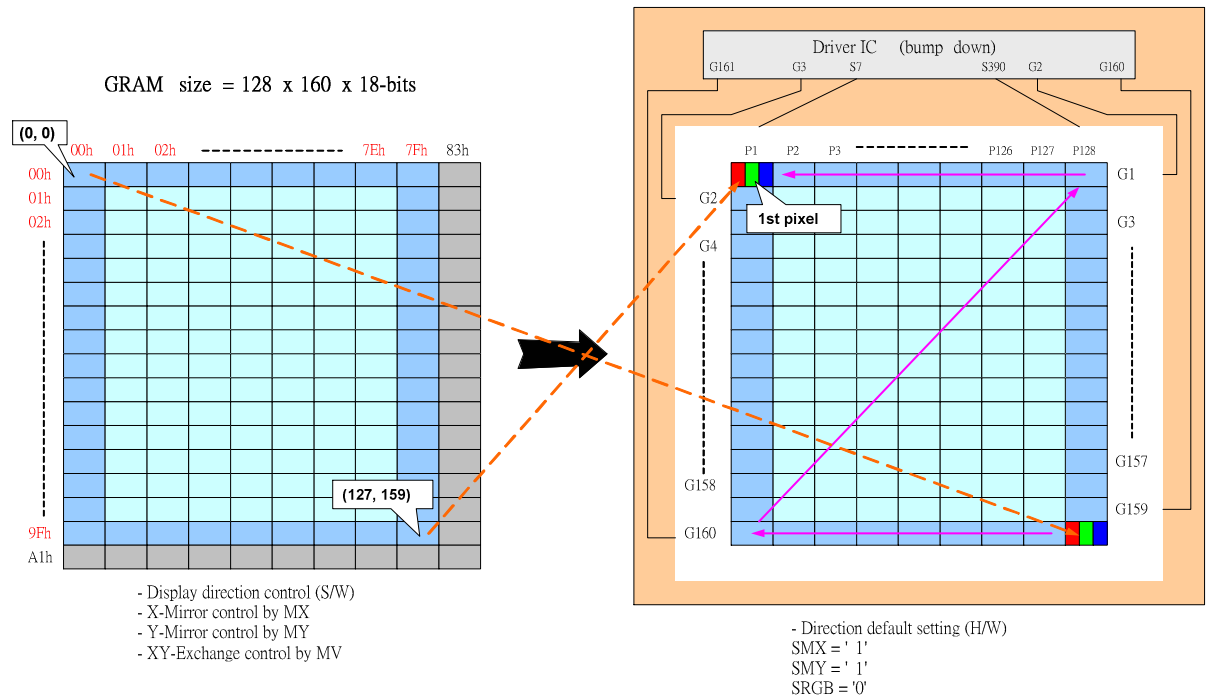
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Case2 of Resolution (132RGB x 162) (GM[2:0] = "000")
RAM size=132 x 162 x 18-bit (Used)
Display size = 132RGB x 162

1). Example for SMX=SMY='0'

**GRAM size = 132 x 162 x 18-bits**



- **Display direction control (S/W)**
- **X-Mirror control by MX**
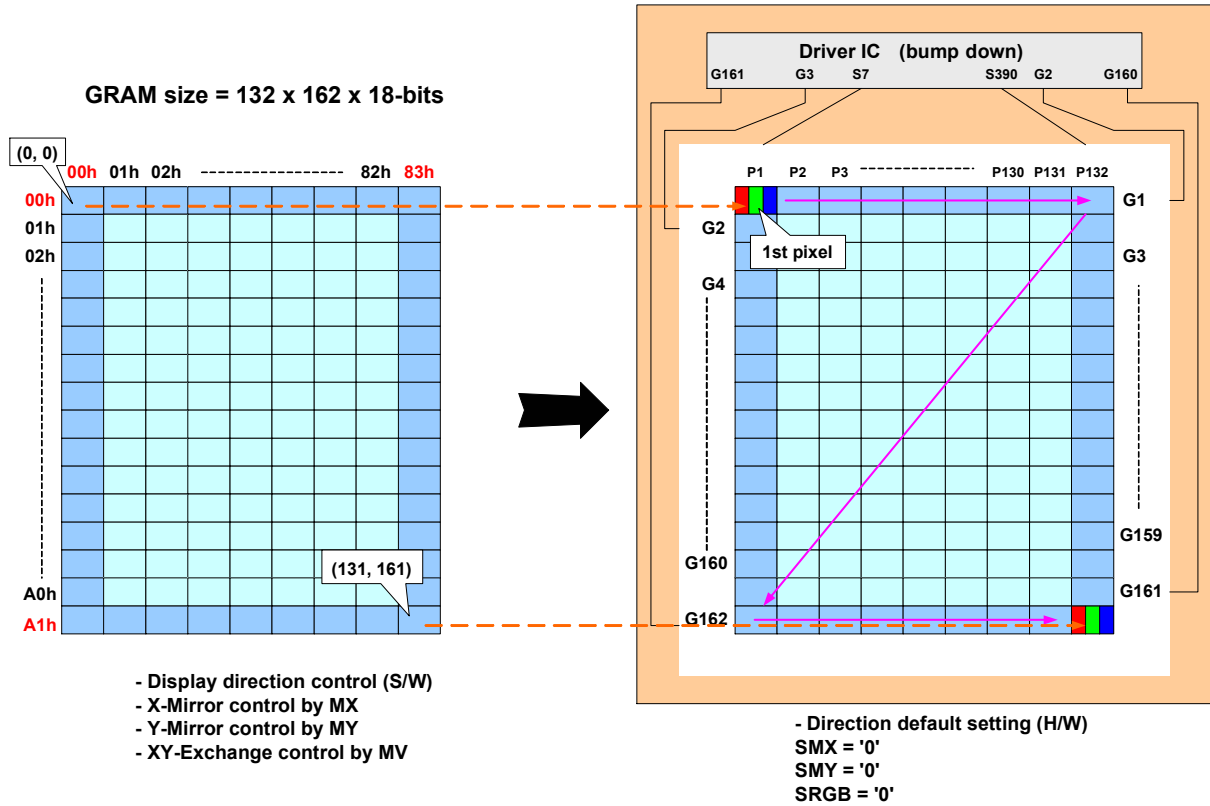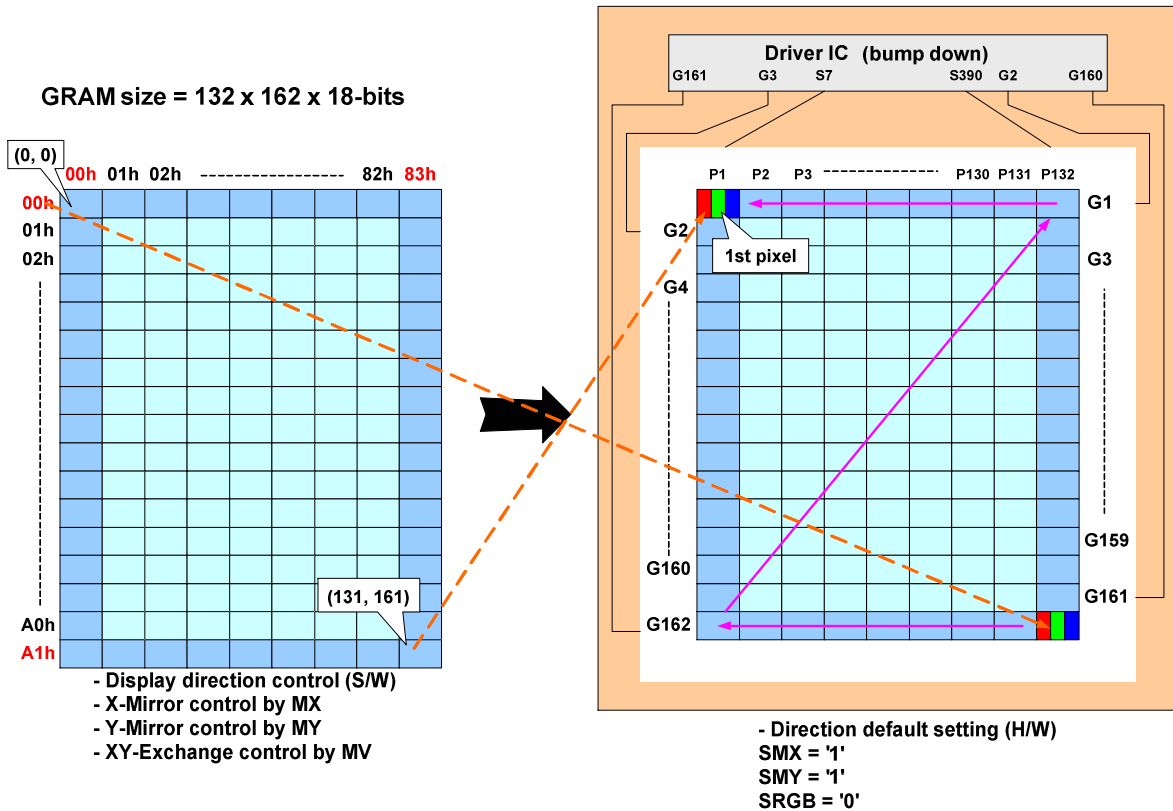- **Y-Mirror control by MY**
- **XY-Exchange control by MV**

- **Direction default setting (H/W)**
**SMX = '0'**
**SMY = '0'**
**SRGB = '0'**

2). Example for SMX=SMY='1'

**GRAM size = 132 x 162 x 18-bits**



- **Display direction control (S/W)**
- **X-Mirror control by MX**
- **Y-Mirror control by MY**
- **XY-Exchange control by MV**

- **Direction default setting (H/W)**
**SMX = '1'**
**SMY = '1'**
**SRGB = '0'**

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## 13.3 MicroProcessor Interface applications

8080-Seriers MCU + SPI Interface ( IM2='1')

### 13.3.1 8080-Series MCU Interface for 8-bit data bus (IM1, IM0="00")
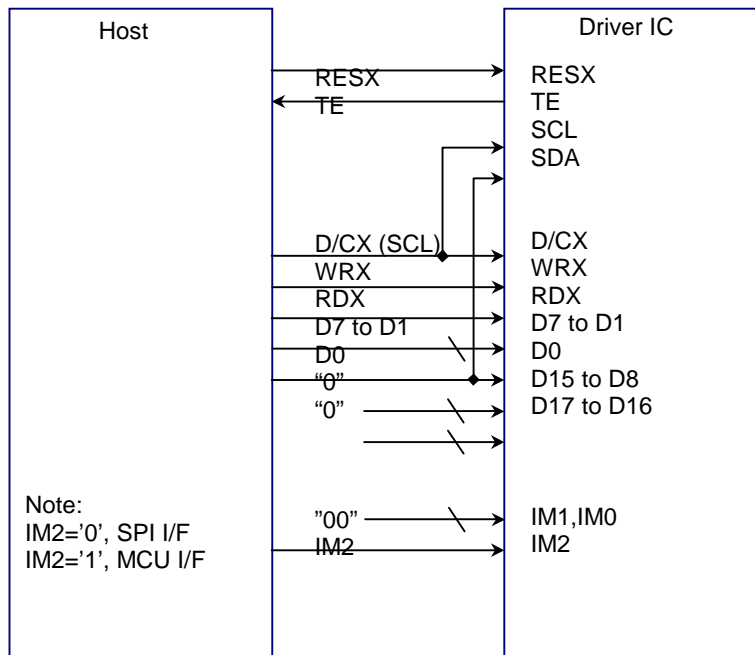


Fig. 13.3.1 8080 Series MCU Interface for 8-bit data bus

### 13.3.2 8080-Series MCU Interface for 16-bit data bus (IM1, IM0="01")



Fig. 13.3.2 8080 Series MCU Interface for 16-bit data bus

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### 13.3.3 8080-Series MCU Interface for 9-bit data bus (IM1, IM0="10")



Fig. 13.3.3 8080 Series MCU Interface for 9-bit data bus

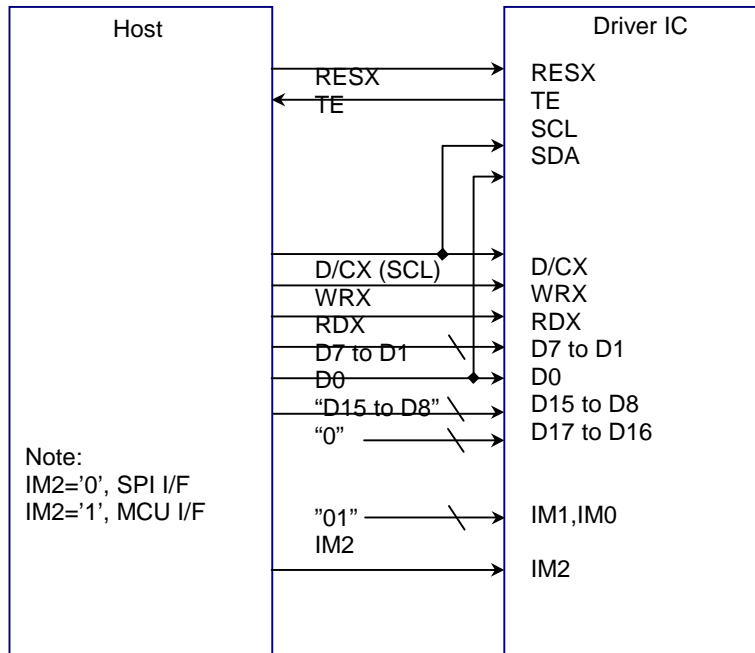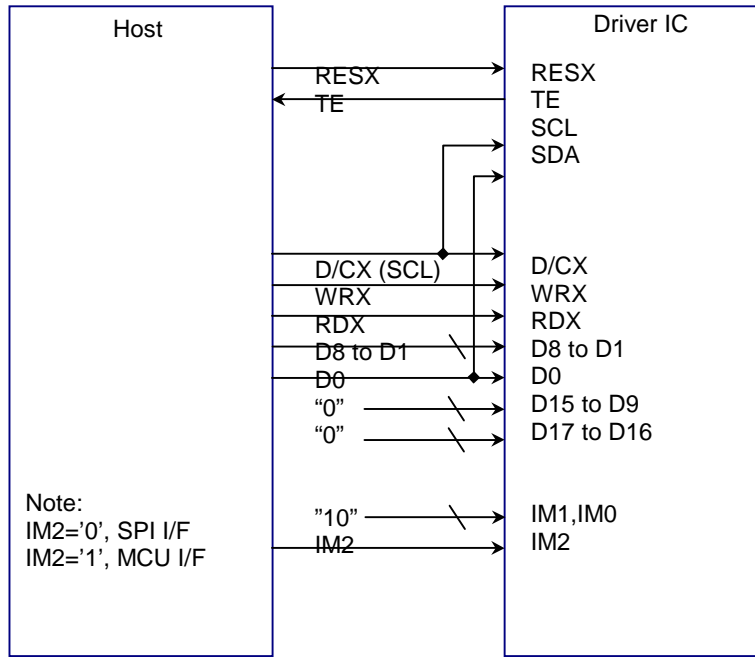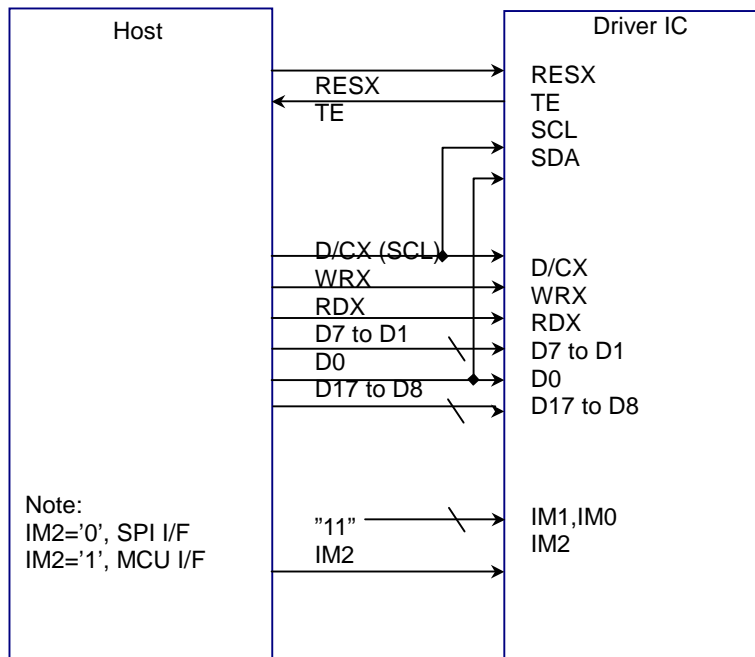### 13.3.4 8080-Series MCU Interface for 18-bit data bus (IM1, IM0="11")



Fig. 13.3.4 8080 Series MCU Interface for 18-bit data bus

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## 14 Revision History

| ST7735 Specification Revision History | | |
|---|---|---|
| Version | Date | Description |
| 1.0 | 2008/11/27 | First issue. |
| 1.1 | 2009/01/05 | Modify address counter description (P58)<br>Modify DISPOFF(28h) and DISPON(29h) command description (P97~98)<br>Modify frame rate control command (B1~B3h) description (P122~124)<br>Modify ROM code default value (P122~140)<br>Modify external components table, AVDD capacitance value change and schottky diode remove. (P154~155) |
| 1.2 | 2009/03/09 | Modify VCC maximum absolute operating voltage (P18)<br>Modify power consumption condition (P20)<br>Modify VMCTR1(C5h) command restriction (P138) |
| 1.3 | 2009/08/05 | Modify the parameter of command 0xDF(P145) |
| 1.4 | 2009/08/28 | Add AVDD, VCI1 voltage.(P16,P128, P154)<br>Add fOSC value (P122, P123, P124)<br>Modify the setting values of VCOM table with HEX. |
| 1.5 | 2009/09/01 | Modify AVDD voltage.( P154)<br>Modify the descriptions in command table with HEX. |
| 1.6 | 2009/09/23 | Modify EXTC description.(P14)<br>Modify VCI1 description to Hi-Z.(P16) |
| 1.7 | 2009/12/04 | Modify DISSET5 (B6h) command (P126) |

## ST7735