300-W STEREO / 400-W MONO PurePath™ HD ANALOG-INPUT POWER STAGE

Check for Samples: TAS5630B

FEATURES

- **PurePath™ HD Enabled Integrated Feedback Provides:**
  - **Signal Bandwidth up to 80 kHz for High-Frequency Content From HD Sources**
  - **Ultralow 0.03% THD at 1 W into 4 Ω**
  - **Flat THD at all Frequencies for Natural Sound**
  - **80-dB PSRR (BTL, No Input Signal)**
  - **>100-dB (A-weighted) SNR**
  - **Click- and Pop-Free Start-Up**
- **Multiple Configurations Possible on the Same PCB With Stuffing Options:**
  - **Mono Parallel Bridge-Tied Load (PBTL)**
  - **Stereo Bridge-Tied Load (BTL)**
  - **2.1 Single-Ended Stereo Pair and Bridge-Tied Load Subwoofer**
  - **Quad Single-Ended Outputs**
- **Total Output Power at 10% THD+N**
  - **400 W in Mono PBTL Configuration**
  - **300 W per Channel in Stereo BTL Configuration**
  - **145 W per Channel in Quad Single-Ended Configuration**
- **High-Efficiency Power Stage (>88%) With 60-mΩ Output MOSFETs**
- **Two Thermally Enhanced Package Options:**
  - **PHD (64-Pin QFP)**
  - **DKD (44-Pin PSOP3)**
- **Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short-Circuit Protection) With Error Reporting**
- **EMI Compliant When Used With Recommended System Design**

APPLICATIONS

- **Mini Combo System**
- **AV Receivers**
- **DVD Receivers**
- **Active Speakers**

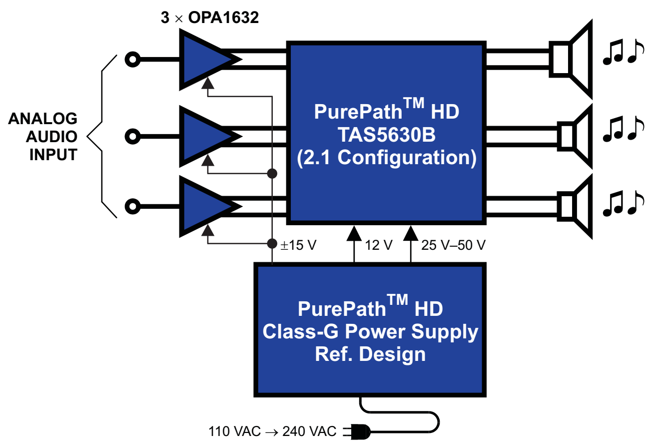
DESCRIPTION

The TAS5630B is a high-performance analog-input class-D amplifier with integrated closed-loop feedback technology (known as PurePath HD technology) with the ability to drive up to 300 W (1) stereo into 4-Ω to 8-Ω speakers from a single 50-V supply.

PurePath HD technology enables traditional AB-amplifier performance (<0.03% THD) levels while providing the power efficiency of traditional class-D amplifiers.

Unlike traditional class-D amplifiers, the distortion curve does not increase until the output levels move into clipping.

PurePath HD technology enables lower idle losses, making the device even more efficient. Coupled with TI's class-G power-supply reference design for TAS563x, industry-leading levels of efficiency can be achieved.



(1) Achievable output power levels are dependent on the thermal configuration of the target application. A high-performance thermal interface material between the exposed package heat slug and the heat sink should be used to achieve high output power levels.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

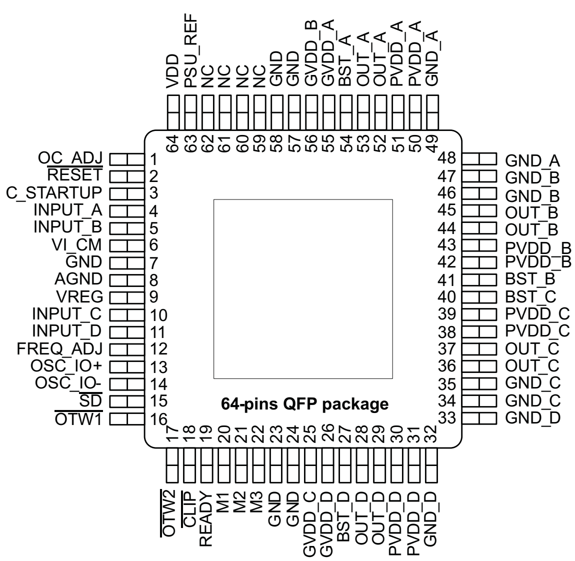
Terminal Assignment

The TAS5630B is available in two thermally enhanced packages:

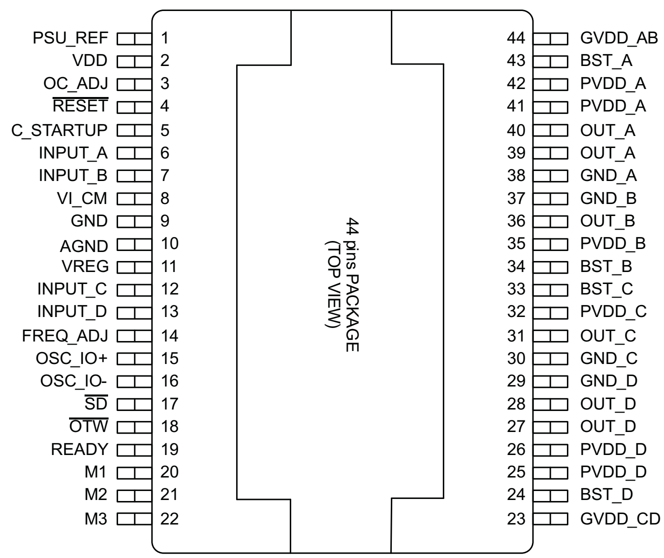
- 64-Pin QFP (PHD) power package
- 44-Pin PSOP3 package (DKD)

The package types contain heat slugs that are located on the top side of the device for convenient thermal coupling to the heat sink.

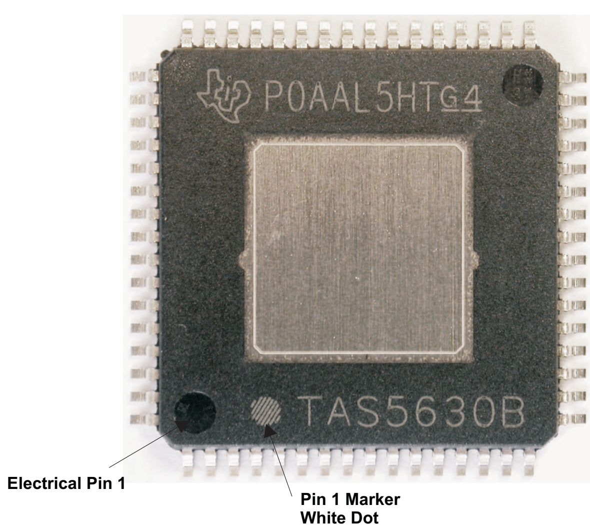
PHD PACKAGE
(TOP VIEW)



DKD PACKAGE
(TOP VIEW)



PIN ONE LOCATION PHD PACKAGE



MODE SELECTION PINS

<table>
<tr><th colspan="3">MODE PINS</th><th rowspan="2">ANALOG INPUT</th><th rowspan="2">OUTPUT CONFIGURATION</th><th colspan="3" rowspan="2">DESCRIPTION</th></tr>
<tr><th>M3</th><th>M2</th><th>M1</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Differential</td><td>2 × BTL</td><td colspan="3">AD mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>—</td><td>—</td><td colspan="3">Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Differential</td><td>2 × BTL</td><td colspan="3">BD mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Differential single-ended</td><td>1 × BTL +2 ×SE</td><td colspan="3">BD mode, BTL differential</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Single-ended</td><td>4 × SE</td><td colspan="3">AD mode</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">0</td><td rowspan="3">1</td><td rowspan="3">Differential</td><td rowspan="3">1 × PBTL</td><th>INPUT_C (1)</th><th>INPUT_D (1)</th><th></th></tr>
<tr><td>0</td><td>0</td><td>AD mode</td></tr>
<tr><td>1</td><td>0</td><td>BD mode</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td colspan="5" rowspan="2">Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>

(1) INPUT_C and D are used to select between a subset of AD and BD mode operations in PBTL mode (1=VREG and 0=AGND).

THERMAL INFORMATION

THERMAL METRIC [1][2]		TAS5630B PHD (64 Pins)	TAS5630B DKD (44 Pins)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	8.5	9.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	0.6	
θ_{JB}	Junction-to-board thermal resistance	20.6	3.7	
ψ_{JT}	Junction-to-top characterization parameter	0.2	1.3	
ψ_{JB}	Junction-to-board characterization parameter	0.73	3.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	8.2	19.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal model data was performed using a 40 x 40 x 90mm heat-sink

Table 1. ORDERING INFORMATION [1]

T_A	PACKAGE	DESCRIPTION
0°C–70°C	TAS5630BPHD	64-pin HTQFP
0°C–70°C	TAS5630BDKD	44-pin PSOP3

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

		VALUE	UNIT
VDD to AGND		–0.3 to 13.2	V
GVDD to AGND		–0.3 to 13.2	V
PVDD_X to GND_X (2)		–0.3 to 69	V
OUT_X to GND_X (2)		–0.3 to 69	V
BST_X to GND_X (2)		–0.3 to 82.2	V
BST_X to GVDD_X (2)		–0.3 to 69	V
VREG to AGND		–0.3 to 4.2	V
GND_X to GND		–0.3 to 0.3	V
GND_X to AGND		–0.3 to 0.3	V
OC_ADJ, M1, M2, M3, OSC_IO+, OSC_IO–, FREQ_ADJ, VI_CM, C_STARTUP, PSU_REF to AGND		–0.3 to 4.2	V
INPUT_X		–0.3 to 7	V
$\overline{RESET}$, $\overline{SD}$, $\overline{OTW1}$, $\overline{OTW2}$, $\overline{CLIP}$, $\overline{READY}$ to AGND		–0.3 to 7	V
Continuous sink current ($\overline{SD}$, $\overline{OTW1}$, $\overline{OTW2}$, $\overline{CLIP}$, $\overline{READY}$)		9	mA
Operating junction temperature range, T_J		0 to 150	°C
Storage temperature, T_{stg}		–40 to 150	°C
Electrostatic discharge	Human-body model (3) (all pins)	±2	kV
	Charged-device model (3) (all pins)	±500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.
(3) Failure to follow good anti-static ESD handling during manufacture and rework contributes to device malfunction. Ensure operators handling the device are adequately grounded through the use of ground straps or alternative ESD protection.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	25	50	52.5	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance (1)	Output filter according to schematics in the application information section	3.5	4		Ω
R_L(SE) (2)			1.8	2		
R_L(PBTL) (2)			2.4	3		
L_{OUTPUT}(BTL)	Output filter inductance (1)	Minimum output inductance at I_{OC}	7	10		μH
L_{OUTPUT}(SE) (2)			7	15		
L_{OUTPUT}(PBTL) (2)			7	10		
f_{PWM}	PWM frame rate selectable for AM interference avoidance; 1% resistor tolerance.	Nominal	385	400	415	kHz
		AM1	315	333	350	
		AM2	260	300	335	
R_{FREQ_ADJ}	PWM frame-rate-programming resistor	Nominal; master mode	9.9	10	10.1	kΩ
		AM1; master mode	19.8	20	20.2	
		AM2; master mode	29.7	30	30.3	
V_{FREQ_ADJ}	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
R_{OCP}	Overcurrent-protection-programming resistor, cycle-by-cycle mode	64-pin QFP package (PHD)	22		33	kΩ
		44-Pin PSOP3 package (DKD)	24		33	
	Overcurrent-protection-programming resistor, latching mode	PHD or DKD	47		68	
T_J	Junction temperature		0		125	°C

(1) Values are for actual measured impedance over all combinations of tolerance, current and temperature and not simply the component rating.
(2) See additional details for SE and PBTL in the System Design Considerations section.

PIN FUNCTIONS

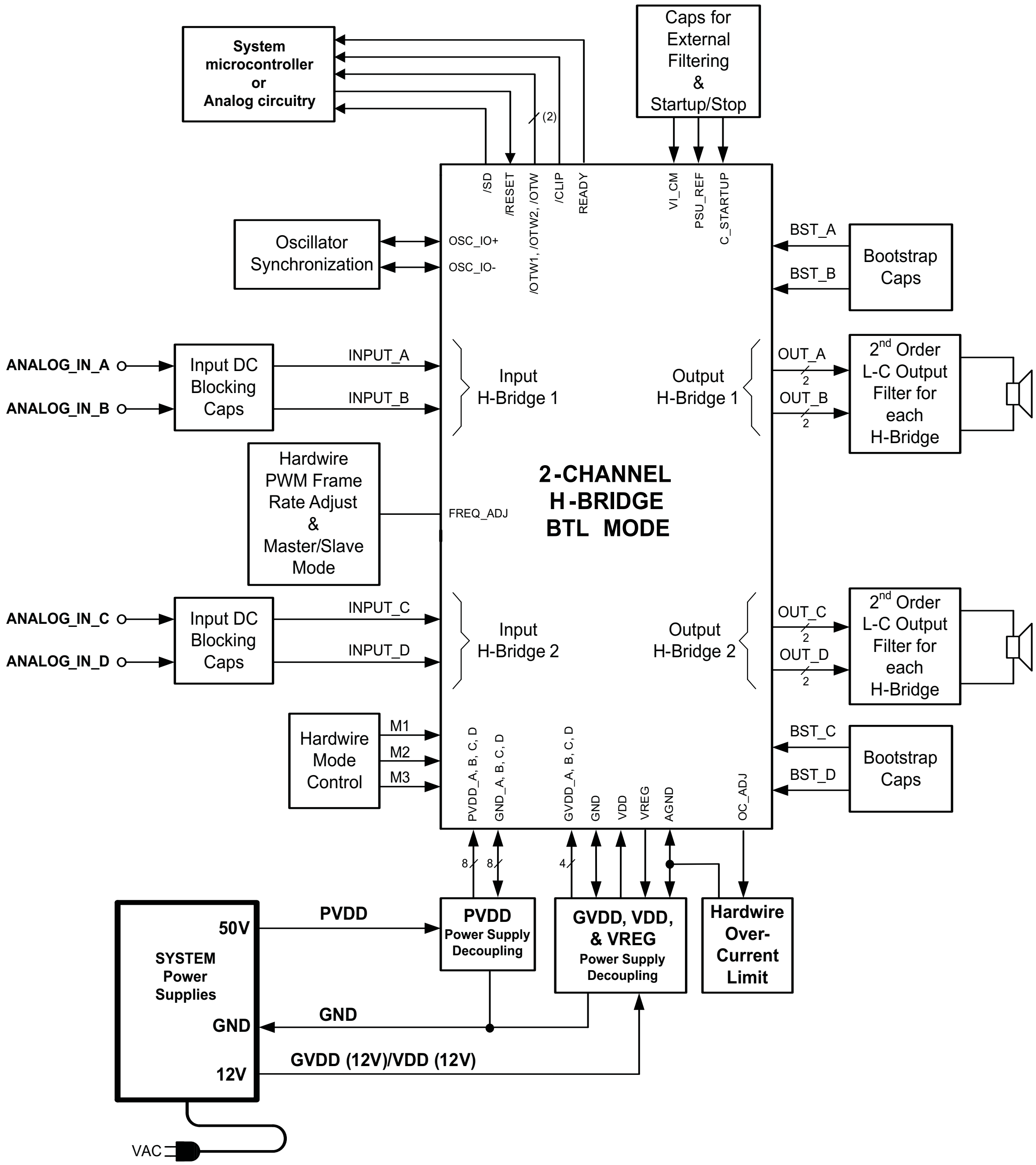
PIN			Function (1)	DESCRIPTION
NAME	PHD NO.	DKD NO.		
AGND	8	10	P	Analog ground
BST_A	54	43	P	HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_A required.
BST_B	41	34	P	HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_B required.
BST_C	40	33	P	HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_C required.
BST_D	27	24	P	HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_D required.
$\overline{\text{CLIP}}$	18	—	O	Clipping warning; open drain; active-low
C_STARTUP	3	5	O	Start-up ramp requires a charging capacitor of 4.7 nF to AGND in BTL mode
FREQ_ADJ	12	14	I	PWM frame-rate-programming pin requires resistor to AGND
GND	7, 23, 24, 57, 58	9	P	Ground
GND_A	48, 49	38	P	Power ground for half-bridge A
GND_B	46, 47	37	P	Power ground for half-bridge B
GND_C	34, 35	30	P	Power ground for half-bridge C
GND_D	32, 33	29	P	Power ground for half-bridge D
GVDD_A	55	—	P	Gate-drive voltage supply requires 0.1-μF capacitor to GND_A
GVDD_B	56	—	P	Gate drive voltage supply requires 0.1-μF capacitor to GND_B
GVDD_C	25	—	P	Gate drive voltage supply requires 0.1-μF capacitor to GND_C
GVDD_D	26	—	P	Gate drive voltage supply requires 0.1-μF capacitor to GND_D
GVDD_AB	—	44	P	Gate drive voltage supply requires 0.22-μF capacitor to GND_A/GND_B
GVDD_CD	—	23	P	Gate drive voltage supply requires 0.22-μF capacitor to GND_C/GND_D
INPUT_A	4	6	I	Input signal for half-bridge A
INPUT_B	5	7	I	Input signal for half-bridge B
INPUT_C	10	12	I	Input signal for half-bridge C
INPUT_D	11	13	I	Input signal for half-bridge D
M1	20	20	I	Mode selection
M2	21	21	I	Mode selection
M3	22	22	I	Mode selection
NC	59–62	–	—	No connect; pins may be grounded.
OC_ADJ	1	3	O	Analog overcurrent-programming pin requires resistor to AGND. 64-pin package (PHD) = 22 kΩ. 44-pin PSOP3 (DKD) = 24 kΩ
OSC_IO+	13	15	I/O	Oscillator master/slave output/input
OSC_IO–	14	16	I/O	Oscillator master/slave output/input
$\overline{\text{OTW}}$	—	18	O	Overtemperature warning signal, open-drain, active-low
$\overline{\text{OTW1}}$	16	—	O	Overtemperature warning signal, open-drain, active-low
$\overline{\text{OTW2}}$	17	—	O	Overtemperature warning signal, open-drain, active-low
OUT_A	52, 53	39, 40	O	Output, half-bridge A
OUT_B	44, 45	36	O	Output, half-bridge B
OUT_C	36, 37	31	O	Output, half-bridge C
OUT_D	28, 29	27, 28	O	Output, half-bridge D
PSU_REF	63	1	P	PSU reference requires close decoupling of 330 pF to AGND.
PVDD_A	50, 51	41, 42	P	Power-supply input for half-bridge A requires close decoupling of 0.01-μF capacitor in parallel with 2.2-μF capacitor to GND_A.
PVDD_B	42, 43	35	P	Power-supply input for half-bridge B requires close decoupling of 0.01-μF capacitor in parallel with 2.2-μF capacitor to GND_B.
PVDD_C	38, 39	32	P	Power-supply input for half-bridge C requires close decoupling of 0.0- μF capacitor in parallel with 2.2-μF capacitor to GND_C.

(1) I = Input, O = Output, P = Power

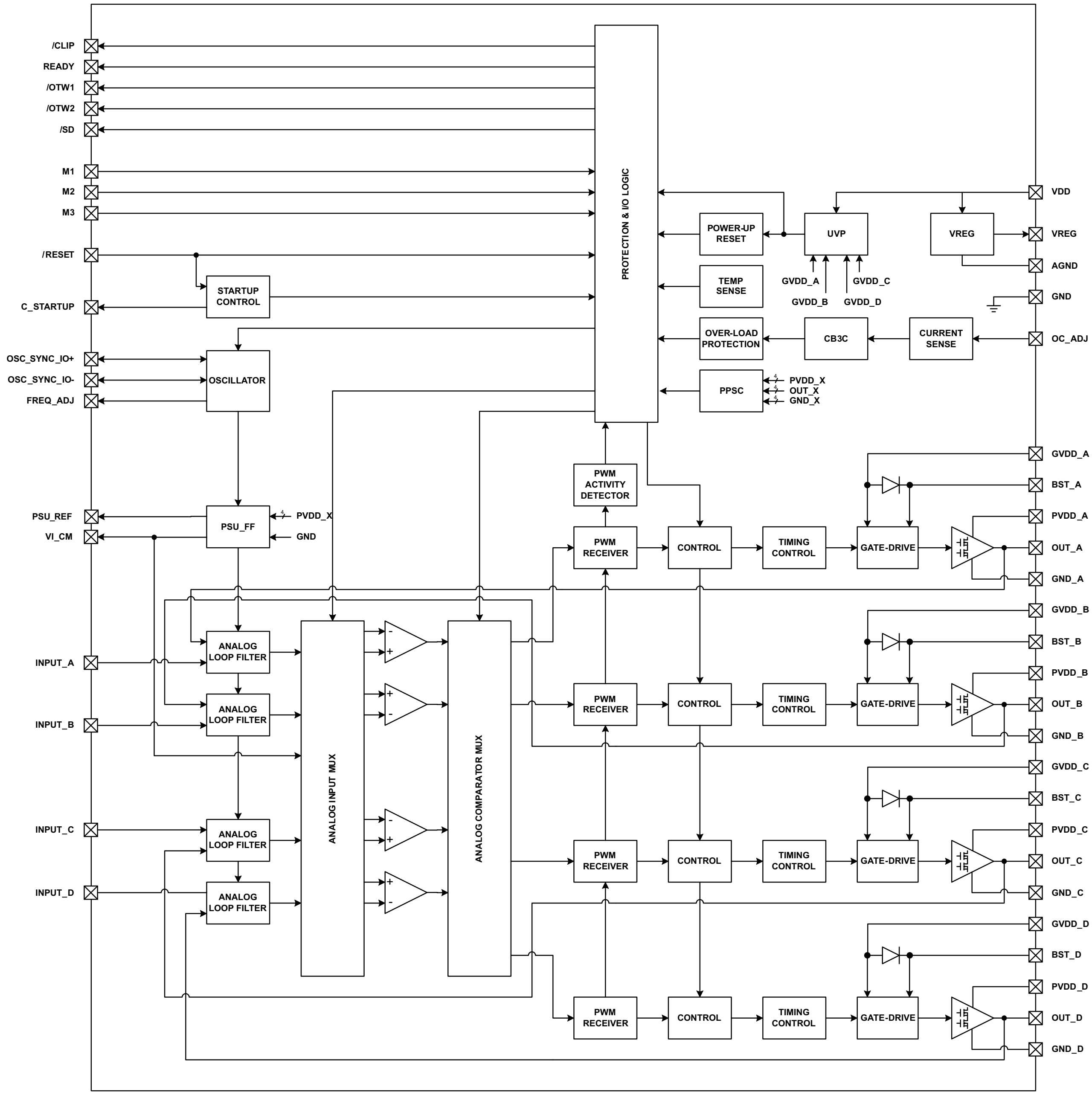
PIN FUNCTIONS (continued)

PIN			Function (1)	DESCRIPTION
NAME	PHD NO.	DKD NO.		
PVDD_D	30, 31	25, 26	P	Power-supply input for half-bridge D requires close decoupling of 0.01-μF capacitor in parallel with 2.2-μF capacitor to GND_D.
READY	19	19	O	Normal operation; open-drain; active-high
$\overline{\text{RESET}}$	2	4	I	Device reset input; active-low
$\overline{\text{SD}}$	15	17	O	Shutdown signal, open-drain, active-low
VDD	64	2	P	Power supply for digital voltage regulator requires a 10-μF capacitor in parallel with a 0.1-μF capacitor to GND for decoupling.
VI_CM	6	8	O	Analog comparator reference node requires close decoupling of 1 nF to AGND.
VREG	9	11	P	Digital regulator supply filter pin requires 0.1-μF capacitor to AGND.

TYPICAL SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



AUDIO CHARACTERISTICS (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 400 kHz, R_{OC} = 22 kΩ, T_C = 75°C; output filter: L_{DEM} = 7 μH, C_{DEM} = 680 nF, MODE = 010, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 4 Ω, 10% THD+N, clipped output signal		300		W
		R_L = 6 Ω, 10% THD+N, clipped output signal		210		
		R_L = 8 Ω, 10% THD+N, clipped output signal		160		
		R_L = 4 Ω, 1% THD+N, unclipped output signal		240		
		R_L = 6 Ω, 1% THD+N, unclipped output signal		160		
		R_L = 8 Ω, 1% THD+N, unclipped output signal		125		
THD+N	Total harmonic distortion + noise	1 W		0.03%		
V_n	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded		270		μV
$\|V_{OS}\|$	Output offset voltage	Inputs ac-coupled to AGND		20	50	mV
SNR	Signal-to-noise ratio (1)	A-weighted, AES17 filter		100		dB
DNR	Dynamic range	A-weighted, AES17 filter		100		dB
P_{idle}	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0, four channels switching (2)		2.7		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

AUDIO SPECIFICATION (Single-Ended Output)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 400 kHz, R_{OC} = 22 kΩ, T_C = 75°C; output filter: L_{DEM} = 15 μH, C_{DEM} = 470 μF, MODE = 100, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N, clipped output signal		145		
		R_L = 3 Ω, 10% THD+N, clipped output signal		100		W
		R_L = 4 Ω, 10% THD+N, clipped output signal		75		
		R_L = 2 Ω, 1% THD+N, unclipped output signal		110		
		R_L = 3 Ω, 1% THD+N, unclipped output signal		75		
		R_L = 4 Ω, 1% THD+N, unclipped output signal		55		
THD+N	Total harmonic distortion + noise	1 W		0.07%		
V_n	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded		340		μV
SNR	Signal-to-noise ratio (1)	A-weighted, AES17 filter		93		dB
DNR	Dynamic range	A-weighted, AES17 filter		93		dB
P_{idle}	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0, four channels switching (2)		2		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

AUDIO SPECIFICATION (PBTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 3 Ω, f_S = 400 kHz, R_{OC} = 22 kΩ, T_C = 75°C; output filter: L_{DEM} = 7 μH, C_{DEM} = 1.5 μF, MODE = 101-10, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N, clipped output signal		400		W
		R_L = 4 Ω, 10% THD+N, clipped output signal		300		
		R_L = 3 Ω, 1% THD+N, unclipped output signal		310		
		R_L = 4 Ω, 1% THD+N, unclipped output signal		230		
THD+N	Total harmonic distortion + noise	1 W		0.05%		
V_n	Output integrated noise	A-weighted		260		μV
SNR	Signal to noise ratio(1)	A-weighted		100		dB
DNR	Dynamic range	A-weighted		100		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, four channels switching(2)		2.7		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

ELECTRICAL CHARACTERISTICS

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 400 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
VREG	Voltage regulator, only used as reference node, VREG	VDD = 12 V	3	3.3	3.6	V
VI_CM	Analog comparator reference node, VI_CM		1.75	2	2.15	V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		22.5		mA
		Idle, reset mode		22.5		
I_{GVDD_X}	GVDD_x gate-supply current per half-bridge	50% duty cycle		12.5		mA
		Reset mode		1.5		
I_{PVDD_X}	Half-bridge supply current	50% duty cycle with recommended output filter		13.3		mA
		Reset mode, No switching		870		μA
ANALOG INPUTS						
R_{IN}	Input resistance	READY = HIGH		33		kΩ
V_{IN}	Maximum input voltage with symmetrical output swing			5		V_{PP}
I_{IN}	Maximum input current			342		μA
G	Voltage gain (V_{OUT}/V_{IN})			23		dB
OSCILLATOR						
f_{OSC_IO+}	Nominal, master mode	F_{PWM} × 10	3.85	4	4.15	MHz
	AM1, master mode		3.15	3.33	3.5	
	AM2, master mode		2.6	3	3.35	
V_{IH}	High level input voltage		1.86			V
V_{IL}	Low level input voltage				1.45	V
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, excludes metallization resistance, GVDD = 12 V		60	100	mΩ
	Drain-to-source resistance, high side (HS)			60	100	mΩ

ELECTRICAL CHARACTERISTICS (continued)

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 400 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O PROTECTION						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_x and VDD			9.5		V
$V_{uvp,hyst}$ (1)				0.6		V
OTW1(1)	Overtemperature warning 1		95	100	105	°C
OTW2(1)	Overtemperature warning 2		115	125	135	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for OTW to be inactive after OTW event			25		°C
OTE(1)	Overtemperature error		145	155	165	°C
	OTE-OTW differential			30		°C
OTE_{hyst} (1)	A reset must occur for SD to be released following an OTE event.			25		°C
OLPC	Overload protection counter	f_{PWM} = 400 kHz		2.6		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1-Ω load, 64-pin QFP package (PHD) R_{OCP} = 22 kΩ		15		A
		Resistor – programmable, nominal peak current in 1-Ω load, 44-Pin PSOP3 package (DKD), R_{OCP} = 24 kΩ		15		A
	Overcurrent limit protection, latched	Resistor – programmable, nominal peak current in 1-Ω load, R_{OCP} = 47 kΩ		15		A
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent		150		ns
I_{PD}	Internal pulldown resistor at output of each half-bridge	Connected when RESET is active to provide bootstrap charge. Not used in SE mode		3		mA
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High-level input voltage	M1, M2, M3, RESET	2			V
V_{IL}	Low-level input voltage	M1, M2, M3, RESET			0.8	V
I_{lkg}	Input leakage current				100	μA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistance, OTW, OTW1, OTW2, CLIP, READY, SD to VREG		20	26	32	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	V
V_{OL}	Low-level output voltage	I_O = 4 mA		200	500	mV
FANOUT	Device fanout OTW, OTW1, OTW2, SD, CLIP, READY	No external pullup		30		devices

(1) Specified by design.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

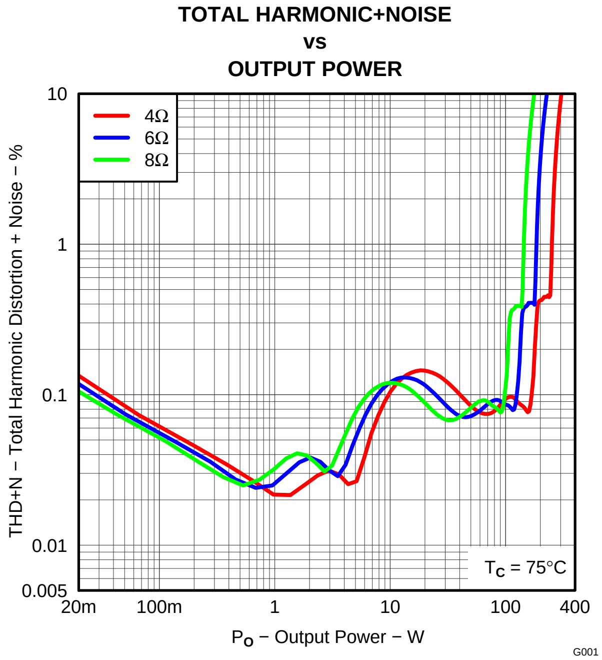


Figure 1.

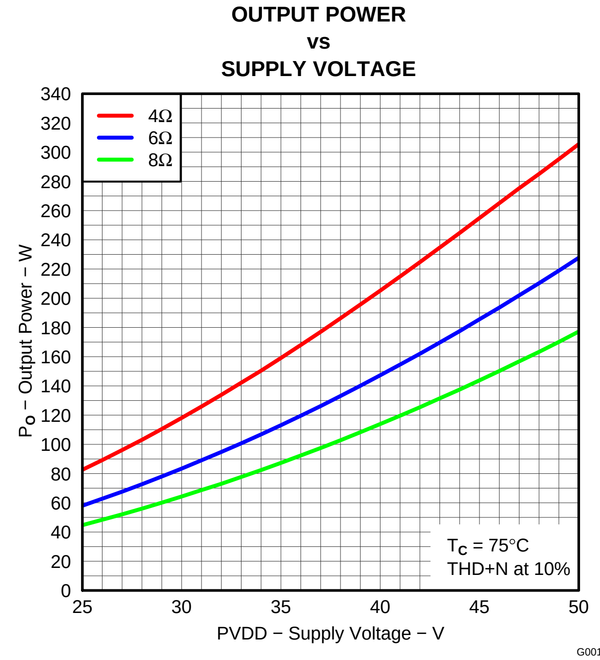


Figure 2.

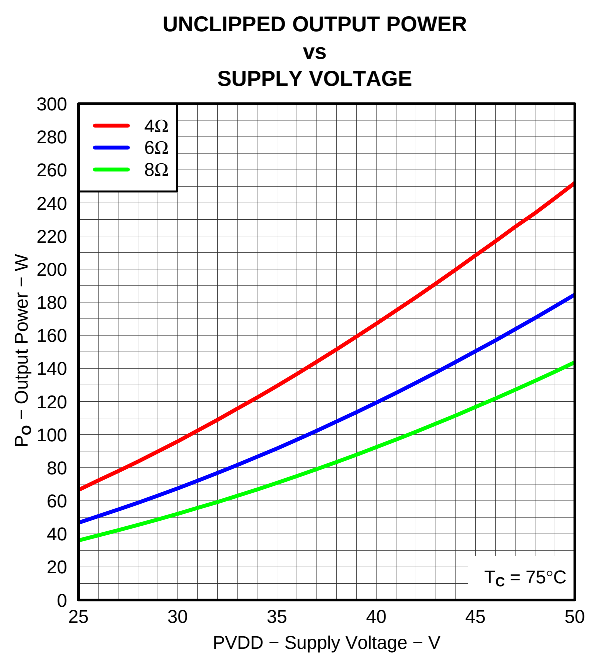


Figure 3.

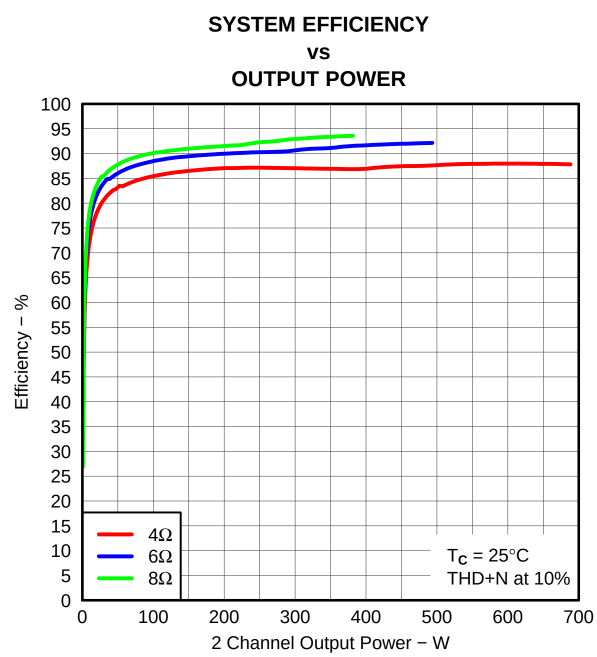


Figure 4.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

SYSTEM POWER LOSS vs OUTPUT POWER

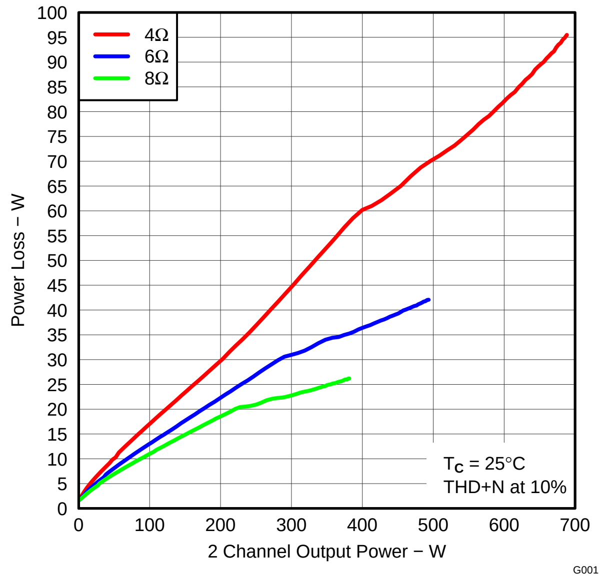


Figure 5.

OUTPUT POWER vs CASE TEMPERATURE

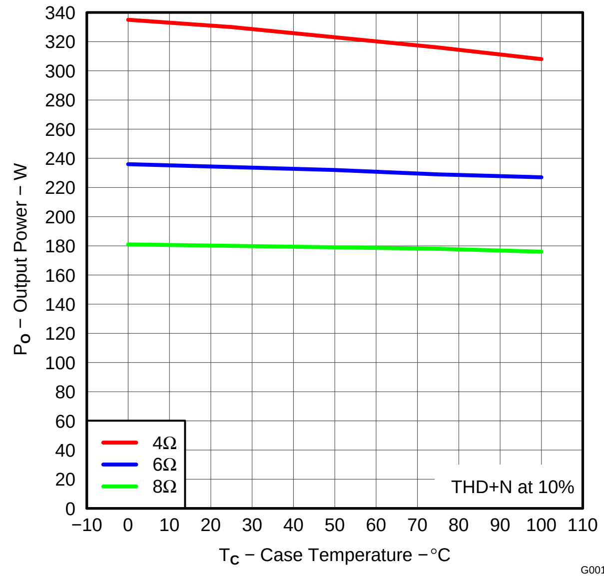


Figure 6.

NOISE AMPLITUDE vs FREQUENCY

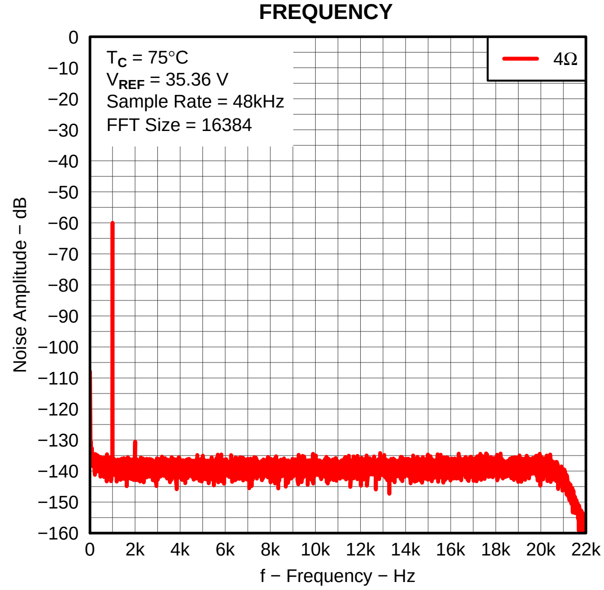


Figure 7.

TYPICAL CHARACTERISTICS, SE CONFIGURATION

1 Channel Driven

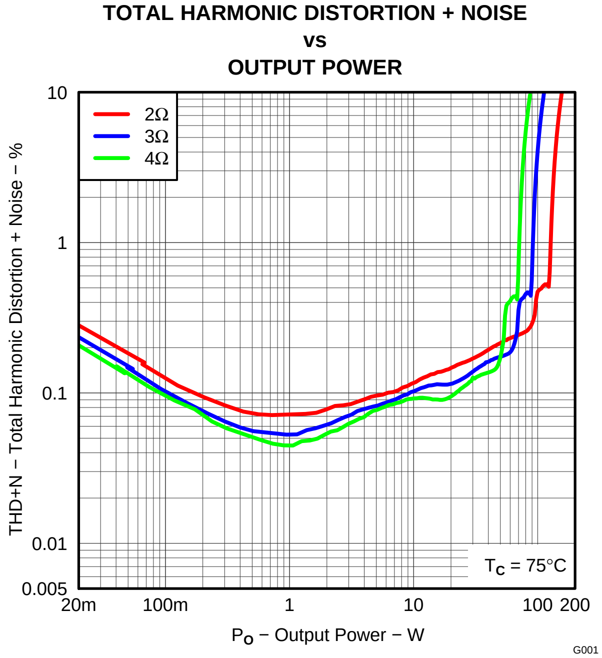


Figure 8.

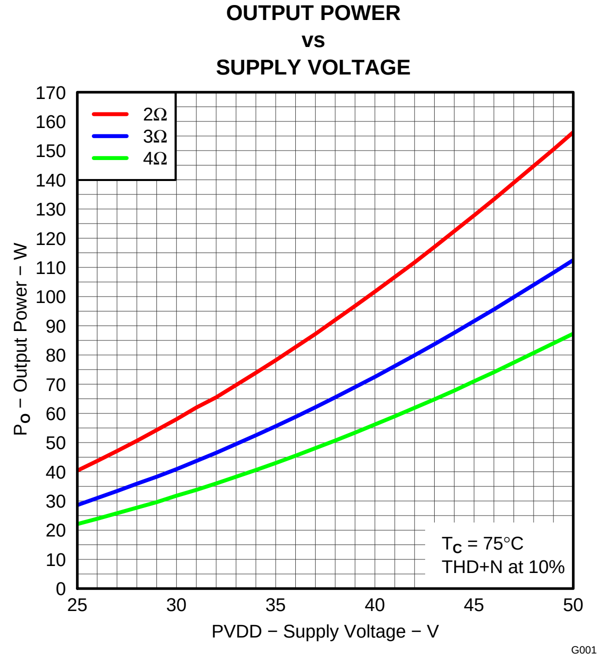


Figure 9.

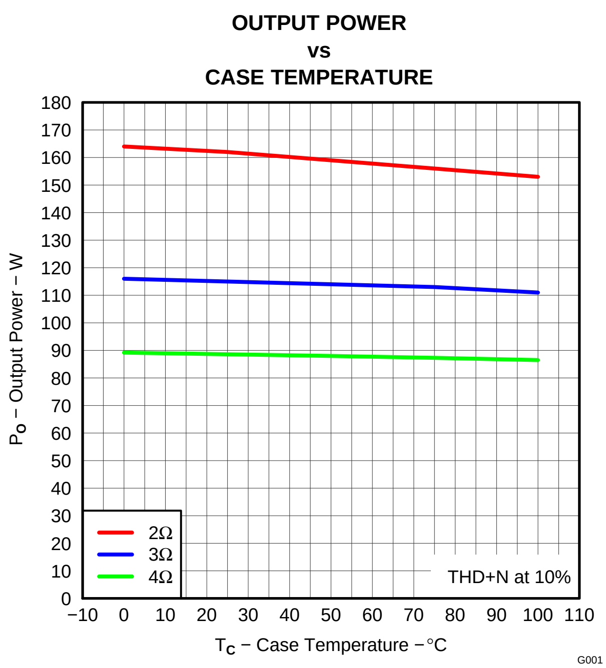


Figure 10.

TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

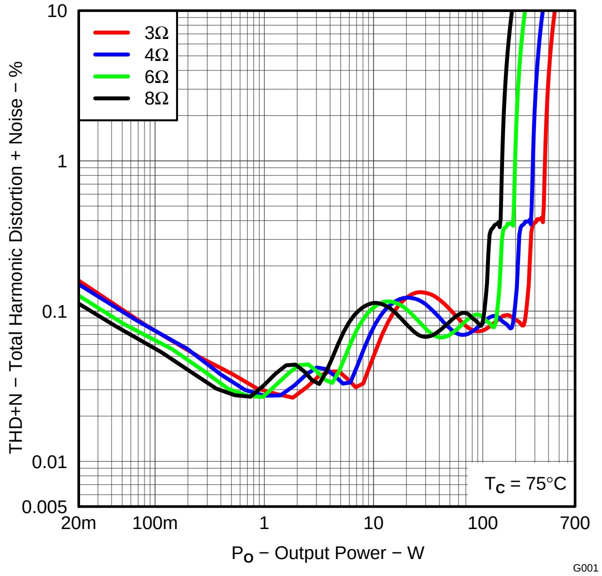


Figure 11.

OUTPUT POWER vs SUPPLY VOLTAGE

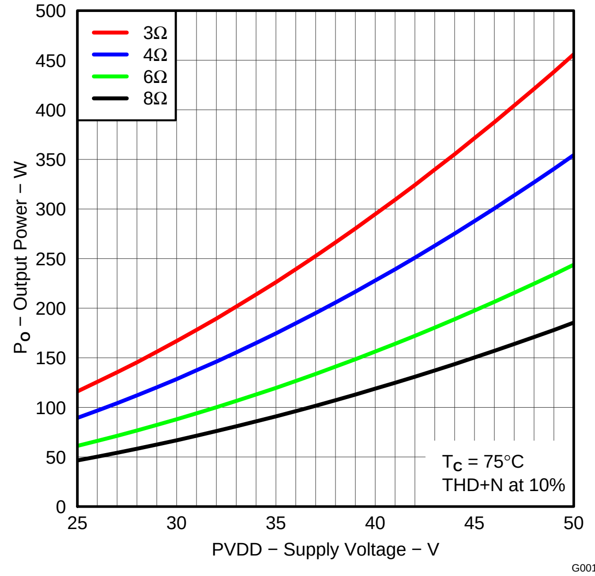


Figure 12.

OUTPUT POWER vs CASE TEMPERATURE

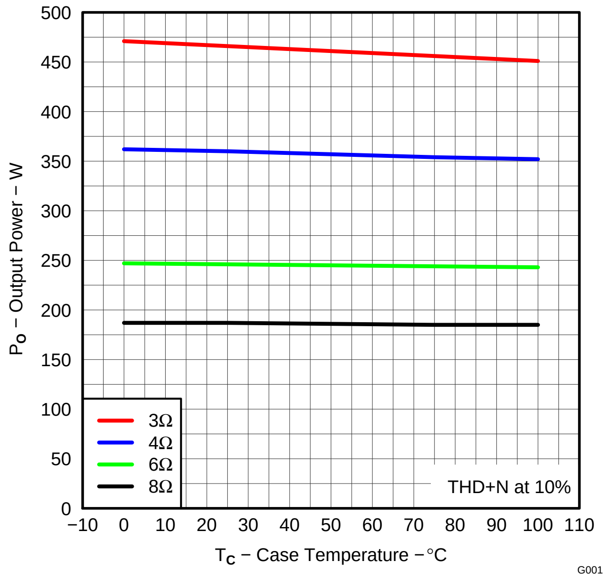


Figure 13.

APPLICATION INFORMATION

PCB MATERIAL RECOMMENDATION

FR-4 2-oz. (70-μm) glass epoxy material is recommended for use with the TAS5630B. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace resistance).

PVDD CAPACITOR RECOMMENDATION

The large capacitors used in conjunction with each full bridge are referred to as the PVDD capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed system power supply, 1000 μF, 63-V supports more applications. The PVDD capacitors should be the low-ESR type, because they are used in a circuit associated with high-speed switching.

DECOUPLING CAPACITOR RECOMMENDATIONS

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 2.2-μF capacitor that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 63 V is required for use with a 50-V power supply.

SYSTEM DESIGN RECOMMENDATIONS

The following schematics and PCB layouts illustrate *best practices* used for the TAS5630B.

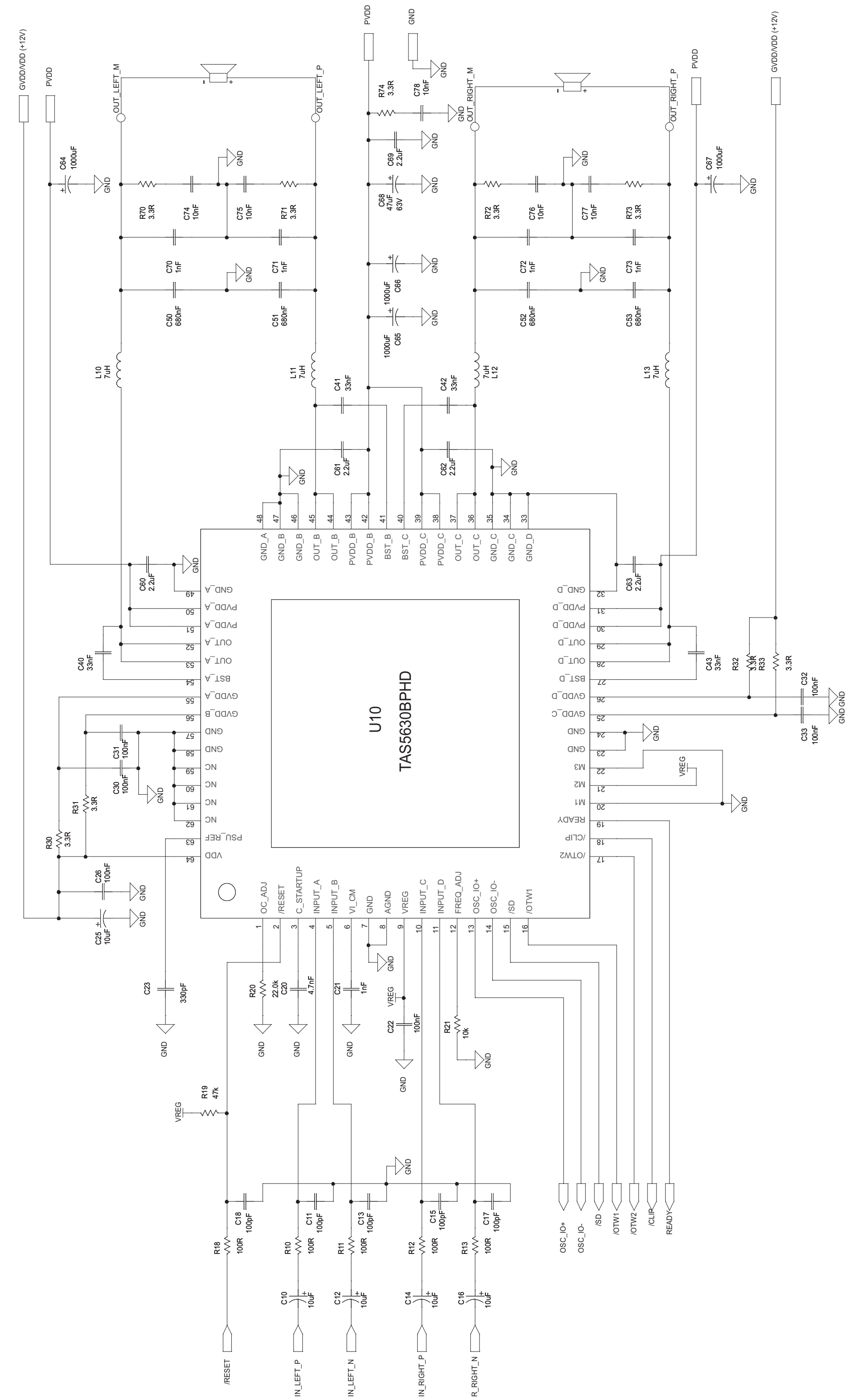


Figure 14. Typical Differential-Input BTL Application With BD Modulation Filters

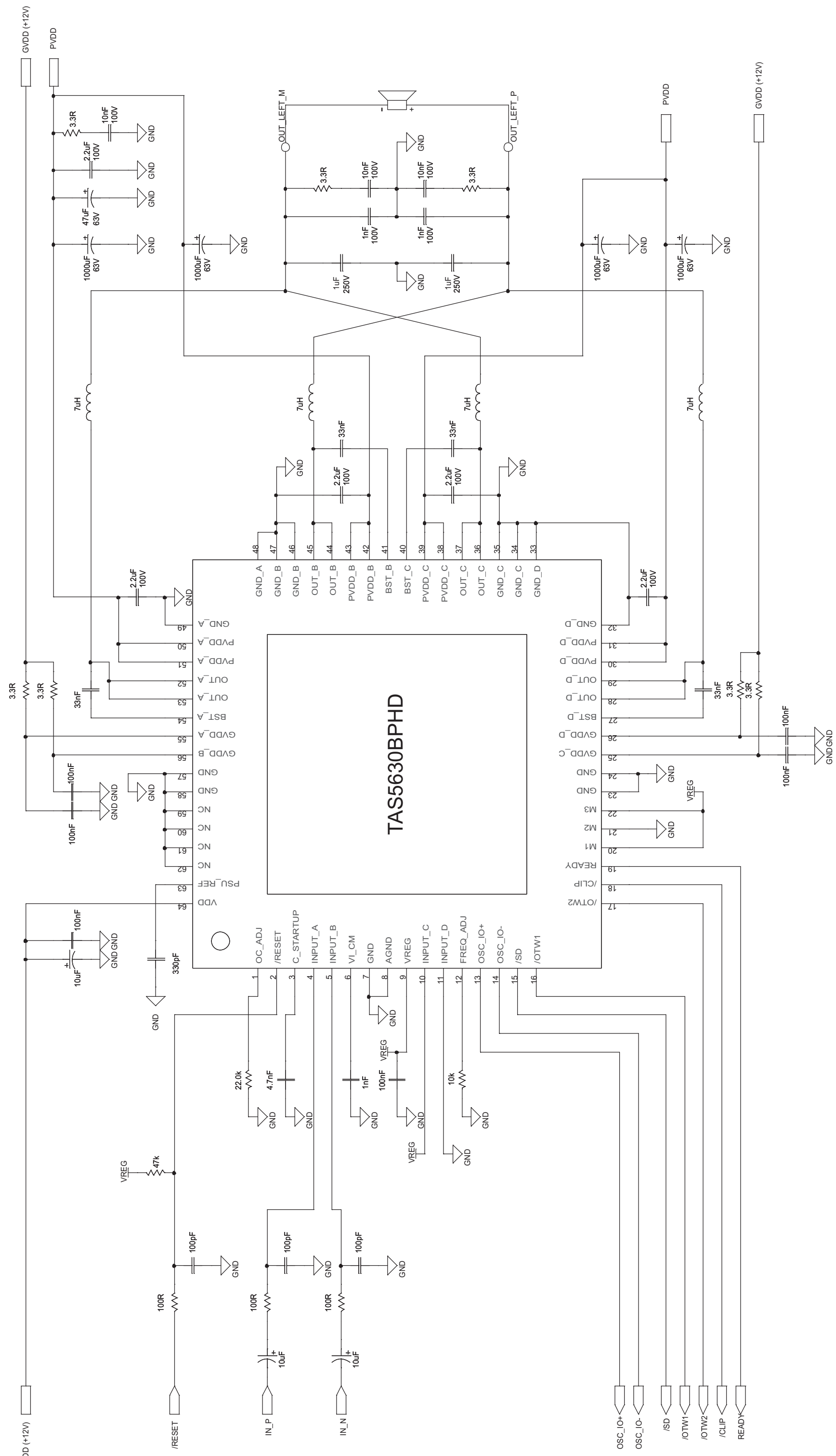
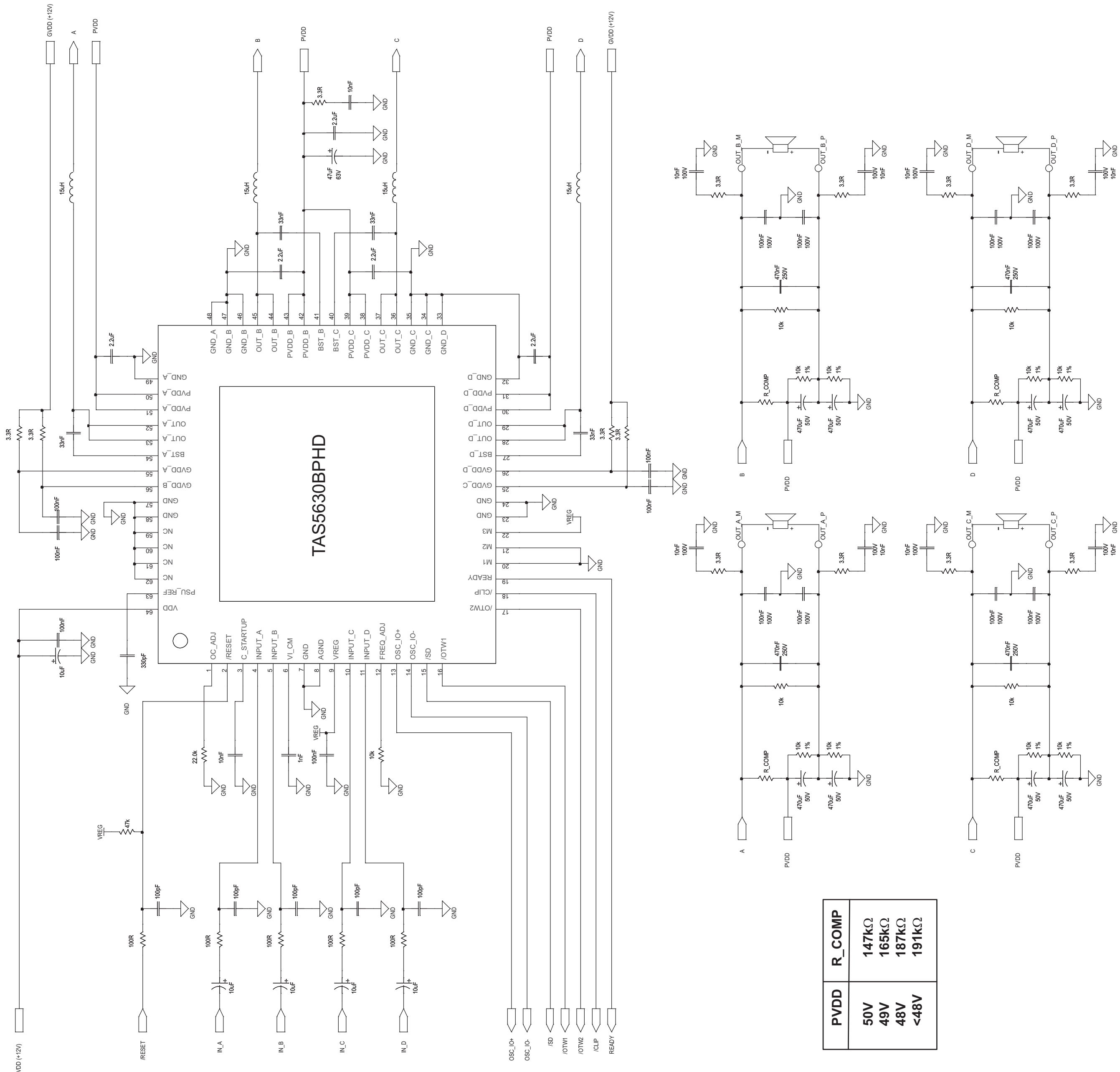


Figure 15. Typical Differential (2N) PBTL Application With BD Modulation Filters



PVDD	R_COMP
50V	147kΩ
49V	165kΩ
48V	187kΩ
<48V	191kΩ

Figure 16. Typical SE Application

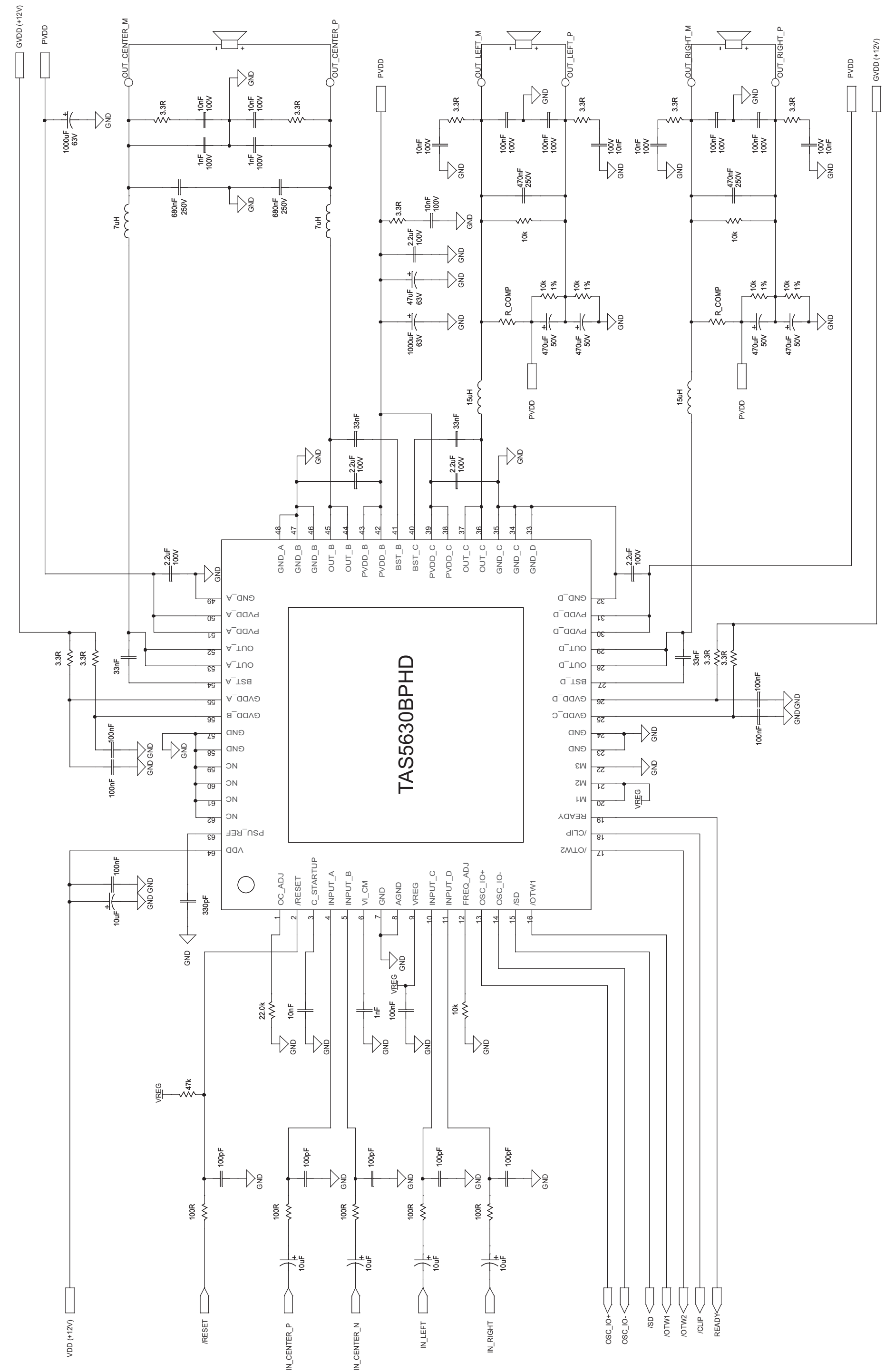


Figure 17. Typical 2.1 System Differential-Input BTL and Unbalanced-Input SE Application

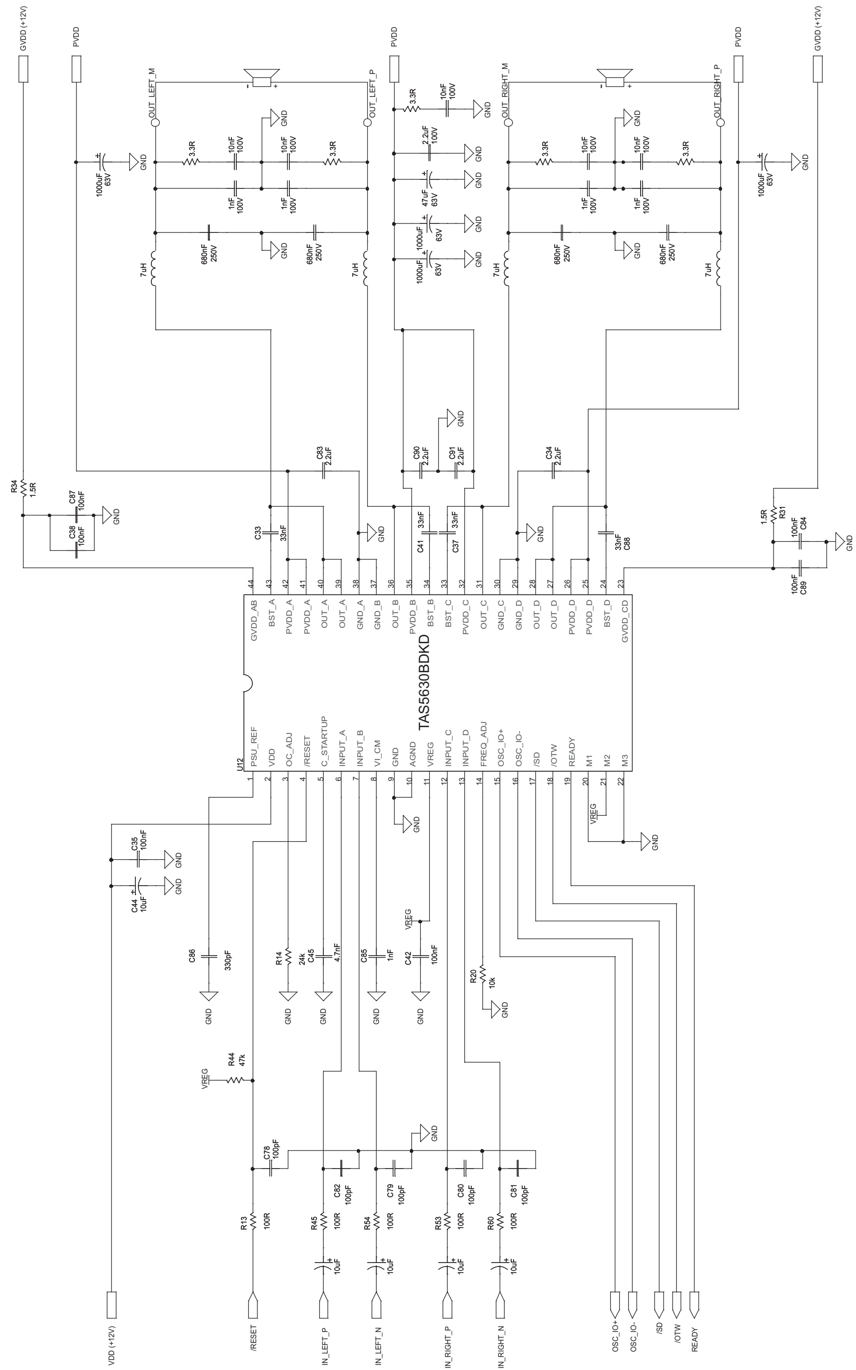


Figure 18. Typical Differential-Input BTL Application With BD Modulation Filters, DKD Package

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5630B needs only a 12-V supply in addition to the (typical) 50-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

To provide outstanding electrical and acoustical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply pins (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300 kHz to 400 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 2.2-μF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5630B reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5630B is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the Recommended Operating Conditions table of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5630B does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The TAS5630B does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops or clicks.

ERROR REPORTING

The $\overline{\text{SD}}$, $\overline{\text{OTW}}$, $\overline{\text{OTW1}}$ and $\overline{\text{OTW2}}$ pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{SD}}$ pin going low. Likewise, $\overline{\text{OTW}}$ and $\overline{\text{OTW2}}$ go low when the device junction temperature exceeds 125°C and $\overline{\text{OTW1}}$ goes low when the junction temperature exceeds 100°C (see the following table).

$\overline{\text{SD}}$	$\overline{\text{OTW1}}$	$\overline{\text{OTW2}}$, $\overline{\text{OTW}}$	DESCRIPTION
0	0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	0	1	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)
0	1	1	Overload (OLP) or undervoltage (UVP)
1	0	0	Junction temperature higher than 125°C (overtemperature warning)
1	0	1	Junction temperature higher than 100°C (overtemperature warning)
1	1	1	Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overline{\text{RESET}}$ low forces the $\overline{\text{SD}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{\text{SD}}$ and $\overline{\text{OTW}}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* table of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5630B contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5630B responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the SD pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

The device functions on errors, as shown in the following table.

<table>
<tr><th colspan="2">BTL Mode</th><th colspan="2">PBTL Mode</th><th colspan="2">SE Mode</th></tr>
<tr><th>Local error in</th><th>Turns Off or in</th><th>Local error in</th><th>Turns Off or in</th><th>Local error in</th><th>Turns Off or in</th></tr>
<tr><td>A</td><td rowspan="2">A + B</td><td>A</td><td rowspan="4">A + B + C + D</td><td>A</td><td rowspan="2">A + B</td></tr>
<tr><td>B</td><td>B</td><td>B</td></tr>
<tr><td>C</td><td rowspan="2">C + D</td><td>C</td><td>C</td><td rowspan="2">C + D</td></tr>
<tr><td>D</td><td>D</td><td>D</td></tr>
</table>

Bootstrap UVP does not shut down according to the table; it shuts down the respective half-bridge.

PIN-TO-PIN SHORT-CIRCUIT PROTECTION (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter, whereas PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup, i.e., when VDD is supplied; consequently, a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two-step sequence. The first step ensures that there are no shorts from OUT_X to GND_X; the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is <15 ms/μF. While the PPSC detection is in progress, SD is kept low, and the device does not react to changes applied to the RESET pins. If no shorts are present the PPSC detection passes, and SD is released, a device reset does not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations; the detection is not performed in SE mode. To make sure the PPSC detection system is not tripped, it is recommended not to insert resistive load between OUT_X and GND_X or PVDD_X.

OVERTEMPERATURE PROTECTION

The two different package options have individual overtemperature protection schemes.

PHD Package:

The TAS5630B PHD package option has a three-level temperature-protection system that asserts an active-low warning signal (OTW1) when the device junction temperature exceeds 100°C (typical), (OTW2) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation. For highest reliability, the RESET should not be asserted until OTW1 has cleared.

DKD Package:

The TAS5630B DKD package option has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and SD being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. It is recommended to wait until OTW has cleared before asserting RESET. Thereafter, the device resumes normal operation.

UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5630B fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach the levels stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and SD being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

When RESET is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high-impedance state when asserting the reset input low. Asserting reset input low removes any fault information to be signaled on the SD output; i.e., SD is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of SD.

SYSTEM DESIGN CONSIDERATIONS

A rising-edge transition on the reset input allows the device to execute the startup sequence and starts switching.

Apply audio only when the state of READY is high; that starts and stops the amplifier without having audible artifacts that are heard in the output transducers. If an overcurrent protection event is introduced, the READY signal goes low; hence, filtering is needed if the signal is intended for audio muting in non-microcontroller systems.

The CLIP signal indicates that the output is approaching clipping. The signal can be used either to activate a volume decrease or to signal an intelligent power supply to increase the rail voltage from low to high for optimum efficiency.

The device inverts the audio signal from input to output.

The VREG pin is not recommended to be used as a voltage source for external circuitry.

Click and Pop in SE-Mode

The BTL startup has low click and pop due to the trimmed output dc offset, see the AUDIO CHARACTERISTICS (BTL) table.

The startup of the BTL+2 x SE system (Figure 17) or 4xSE (Figure 16) is more difficult to get click and pop free, than the pure BTL solution; therefore, evaluating the resulting click and pop before designing in the device is recommended.

PBTL Overload and Short Circuit

The TAS5630B has extensive overload and short circuit protection. In BTL and SE mode, it is fully protected against speaker terminal overloads, terminal-to-terminal short circuit, and short circuit to GND or PVDD. The protection works by limiting the current, by flipping the state of the output MOSFET's; thereby, ramping currents down in the inductor. This only works when the inductor is NOT saturated, the recommended minimum inductor values are listed in RECOMMENDED OPERATING CONDITIONS table. In BTL mode, the short circuit currents can reach more than 15A, so when connecting the device in PBTL mode (Mono), the currents double – that is more than 30A, and with these high currents, the protection system will limit PBTL speaker overloads, terminal-to-terminal shorts, and terminal-to-GND shorts. PBTL mode short circuit to PVDD is not recommended.

OSCILLATOR

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

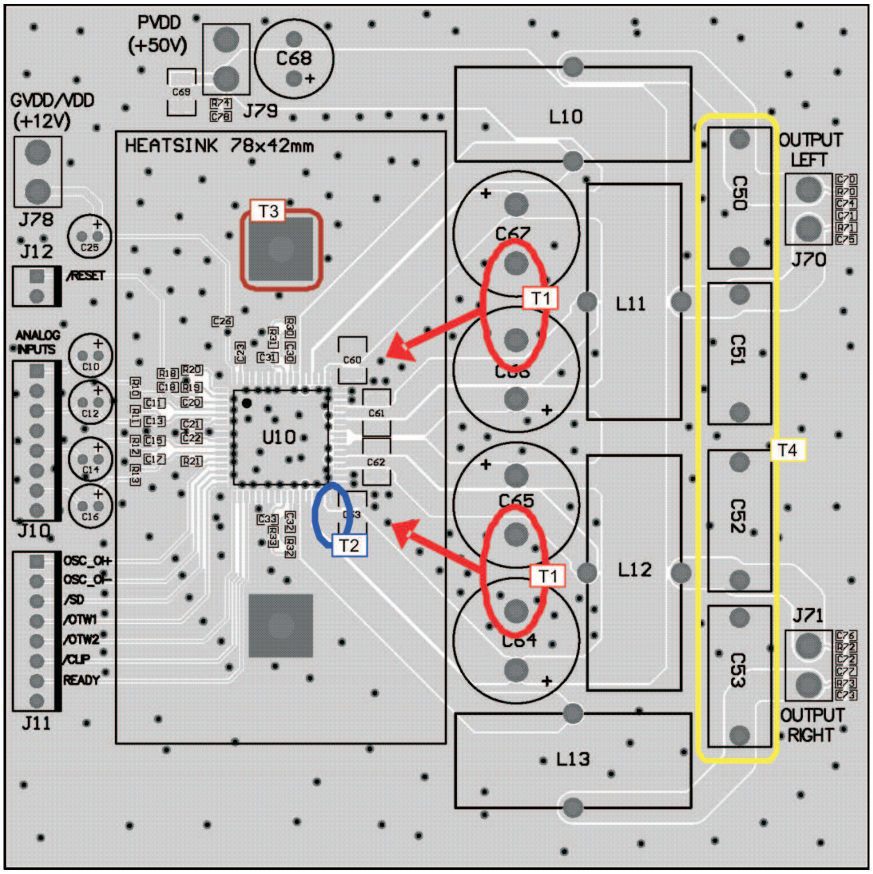
To reduce interference problems while using a radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower values. These values should be chosen such that the nominal and the lower-value switching frequencies together result in the fewest cases of interference throughout the AM band, and can be selected by the value of the FREQ_ADJ resistor connected to AGND in master mode.

For slave-mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to VREG. This configures the OSC_I/O pins as inputs, which must be slaved from an external clock.

PRINTED CIRCUIT BOARD RECOMMENDATION

Use an unbroken ground plane to have a good low-impedance and -inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high, fast-switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing of the audio input should be kept short and together with the accompanying audio-source ground. A local ground area underneath the device is important to keep solid to minimize ground bounce. It is always good practice to follow the EVM layout as a guideline.

Netlist for this printed circuit board is generated from the schematic in Figure 14.



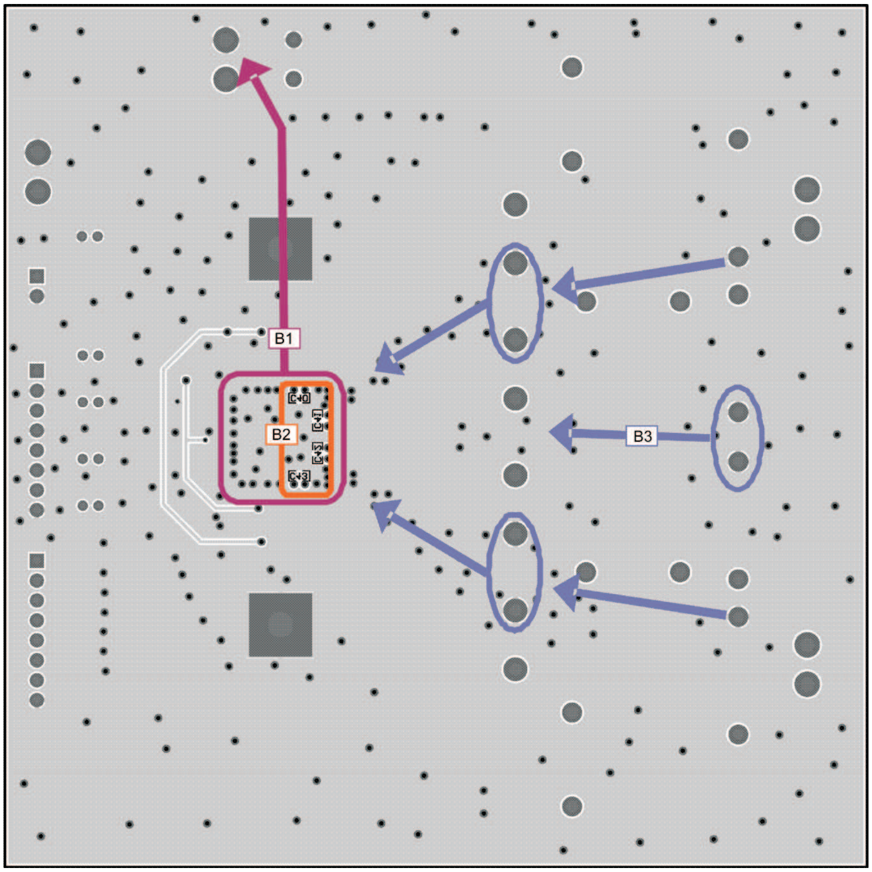
Note T1: PVDD bulk decoupling capacitors C60–C64 should be as close as possible to the PVDD_X and GND_X pins; the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

Note T2: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins. This is valid for C60, C61, C62, and C63.

Note T3: Heat sink must have a good connection to PCB ground.

Note T4: Output filter capacitors must be linear in the applied voltage range, preferably metal film types.

Figure 19. Printed Circuit Board – Top Layer



Note B1: It is important to have a direct-low impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

Note B2: Bootstrap low-impedance X7R ceramic capacitors placed on bottom side provide a short, low-inductance current loop.

Note B3: Return currents from bulk capacitors and output filter capacitors

Figure 20. Printed Circuit Board – Bottom Layer

REVISION HISTORY

Changes from Original (November 2010) to Revision A **Page**

- Changed Title From: 600-W MONO To 400-W MONO 1
- Changed Feature From: 600 W per Channel in Mono PBTL Configuration To: 400 W per Channel in Mono PBTL Configuration 1
- Changed the Pin One Location Package image 2
- Replaced the PACKAGE HEAT DISSIPATION RATINGS table with the THERMAL INFORMATION table 3
- Changed R_L(PBTL) Load Impedance Min value From: 1.6 Ω To: 2.4 Ω, and Typ value From 2 To: 3 Ω 4
- Added footnotes (1) and (2) to the ROC table 4
- Added R_{OCP} information to the ROC Table 4
- Deleted - R_L = 2 Ω, 10%, THD+N, clipped input signal From P_O in the Audio Specification (PBTL) table 10
- Changed the I_{OC} Typical Value From: 19 A To: 15 A 11
- Replaced the TYPICAL CHARACTERISTICS, PBTL CONFIGURATION graphs 15
- Added section - Click and Pop in SE-Mode 25
- Added section - PBTL Overload and Short Circuit 25

(1) See additional details for SE and PBTL in the System Design Considerations section.
(2) Values are for actual measured impedance over all combinations of tolerance, current and temperature and not simply the component rating.

Changes from Revision A (November 2011) to Revision B **Page**

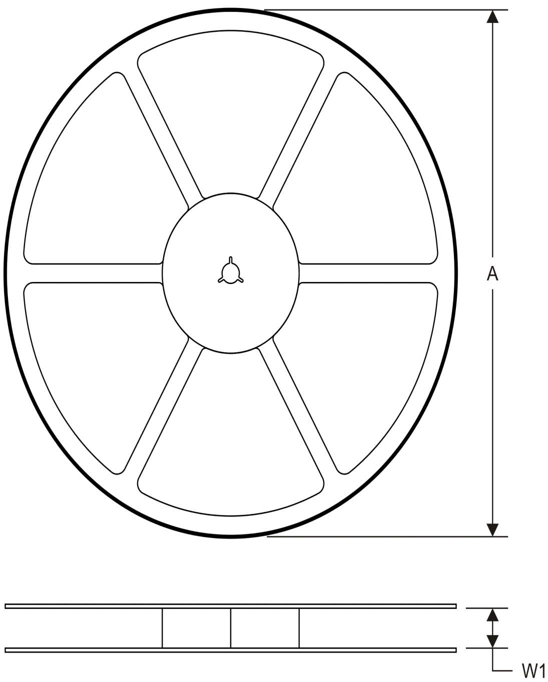
- Changed the R_{INT_PU} parameters From: $\overline{\text{OTW1}}$ to VREG, $\overline{\text{OTW2}}$ to VREG, $\overline{\text{SD}}$ to VREG To: $\overline{\text{OTW}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, READY, $\overline{\text{SD}}$ to VRE 11
- Added text to the PHD Package section. 24
- Added text to the DKD Package section 24

Changes from Revision B (November 2011) to Revision C **Page**

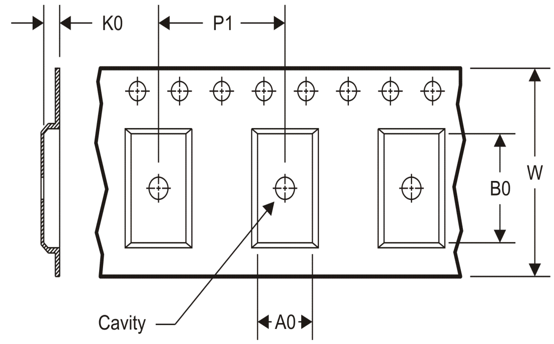
- Deleted - R_L = 2 Ω, 1% THD+N, unclipped output signal From P_O in the Audio Specification (PBTL) table 10
- Changed Analog comparator reference node, VI_CM Vlaues From: MIN = 1.5 TYP = 1.75 MAX = 1.9 To: MIN = 1.75 TYP = 2 MAX = 2.15 10
- Changed ANALOG INPUTS - V_{IN} TYP value From 3.5 to 5 V_{PP} 10
- Changed the V_{IH} and V_{IL} Test Conditions From: INPUT_X, M1, M2, M3, RESET To: M1, M2, M3, RESET 11

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



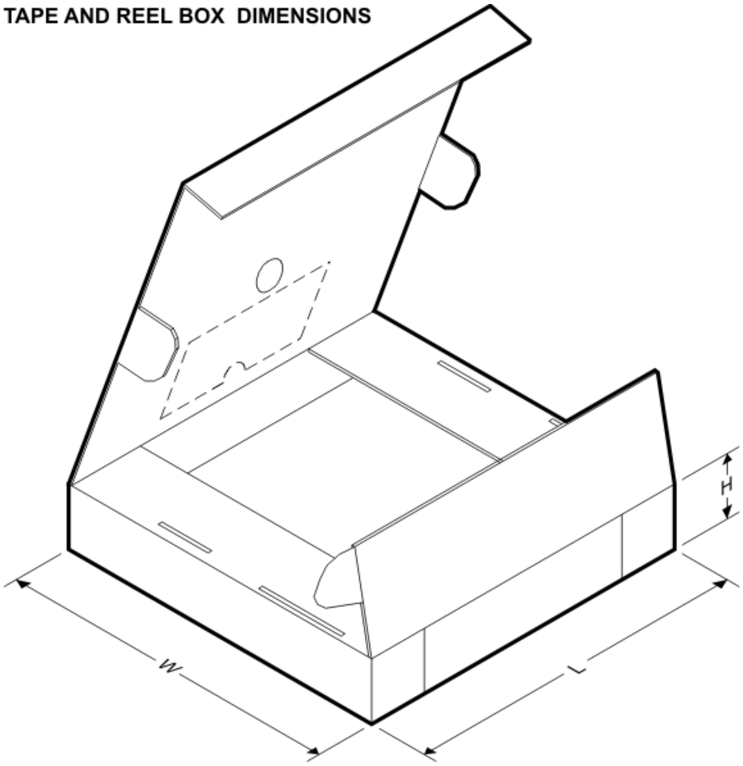
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5630BDKDR	HSSOP	DKD	44	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1
TAS5630BPHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

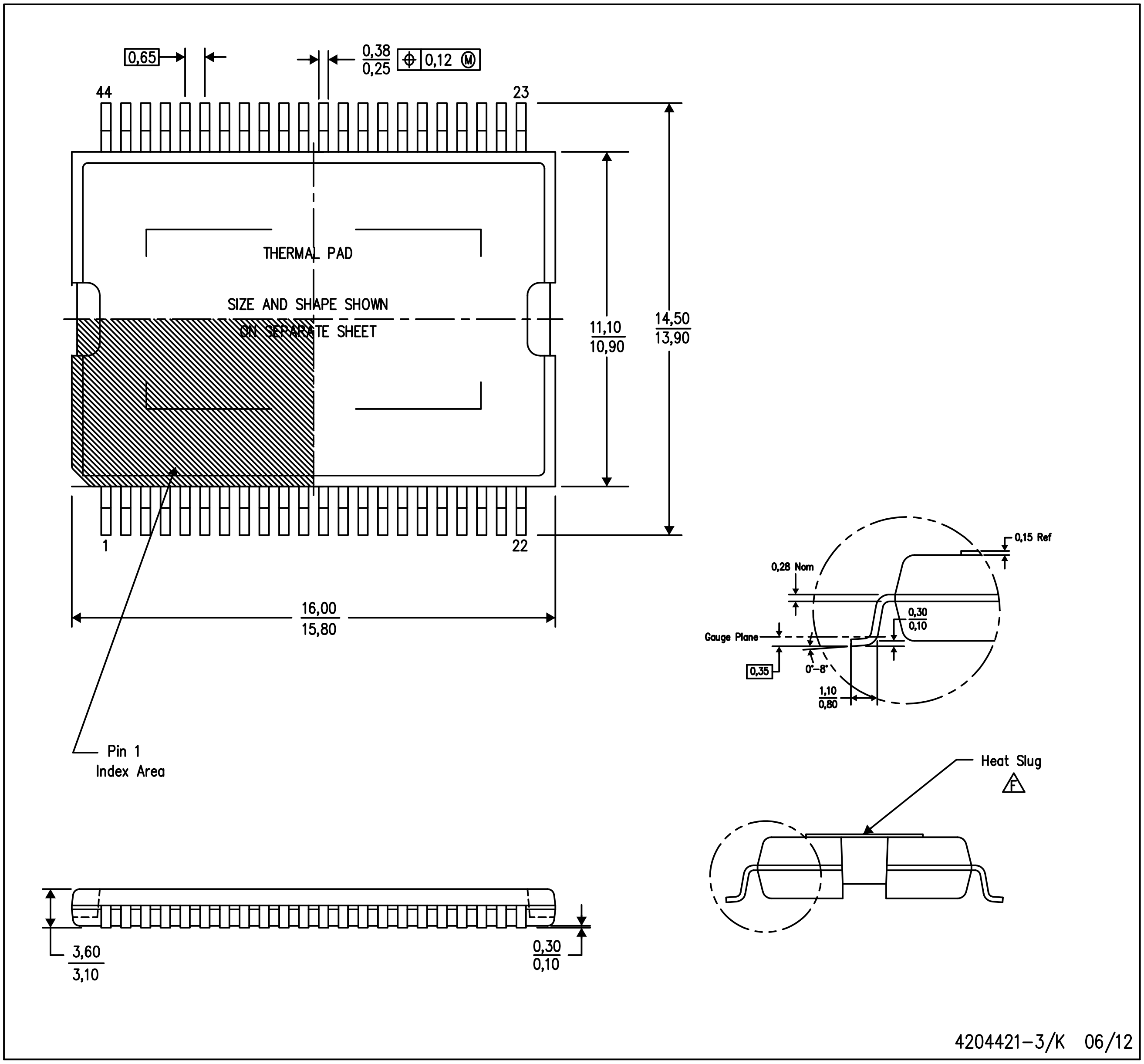
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5630BDKDR	HSSOP	DKD	44	500	367.0	367.0	45.0
TAS5630BPHDR	HTQFP	PHD	64	1000	367.0	367.0	45.0

DKD (R–PDSO–G44) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.15mm.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. The package thermal performance is optimized for conductive cooling with attachment to an external heat sink.

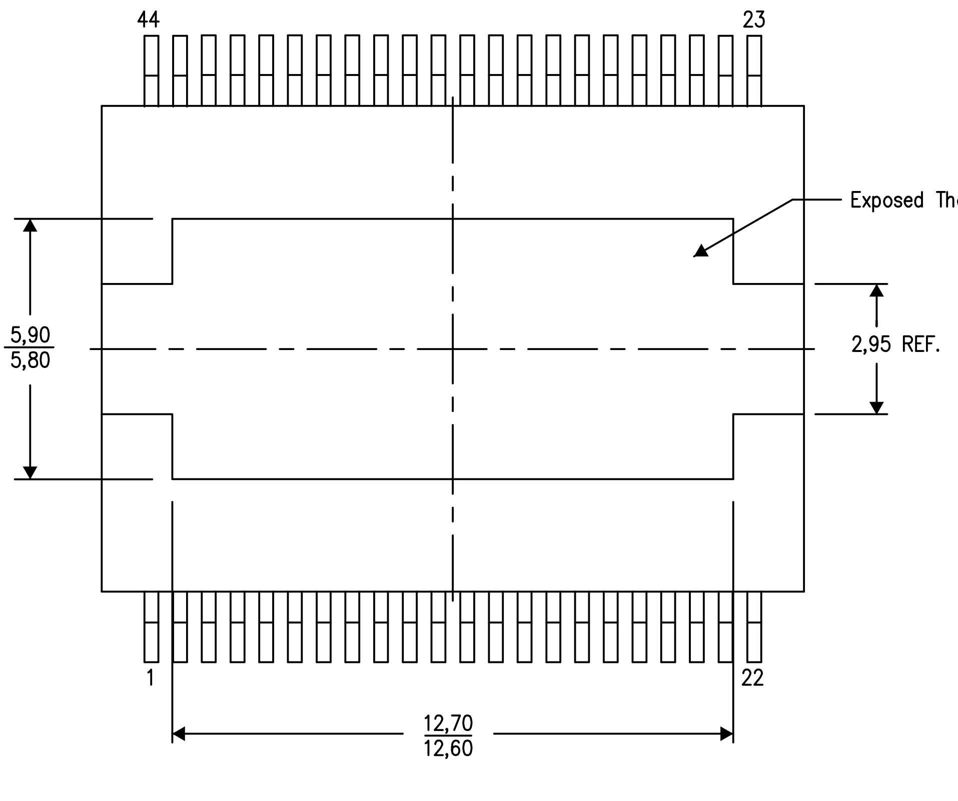
DKD (R-PDSO-G44) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

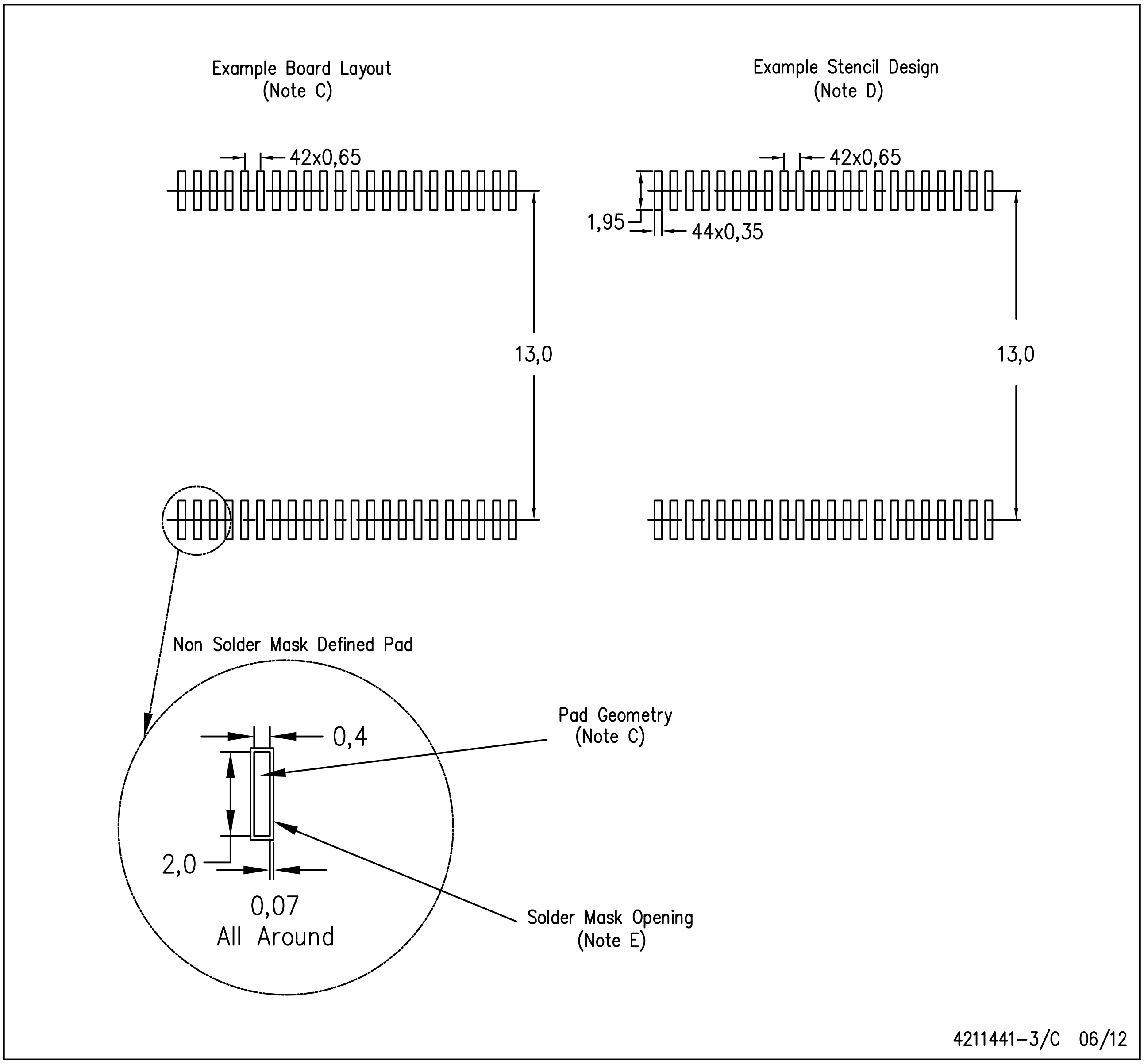


Exposed Thermal Pad Dimensions

4210894-3/E 06/12

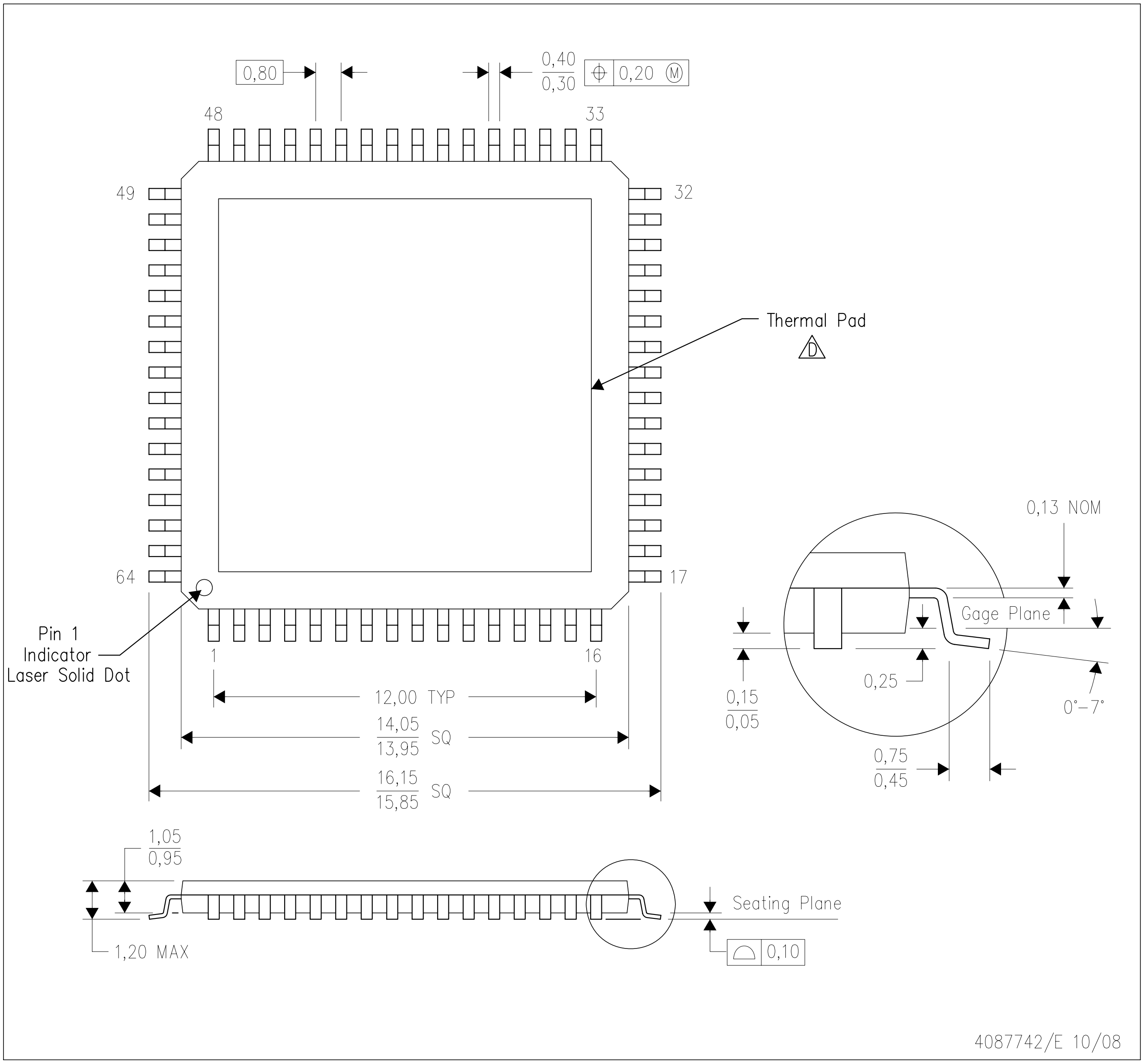
NOTE: All linear dimensions are in millimeters

DKD (R–PDSO–G44) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PHD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

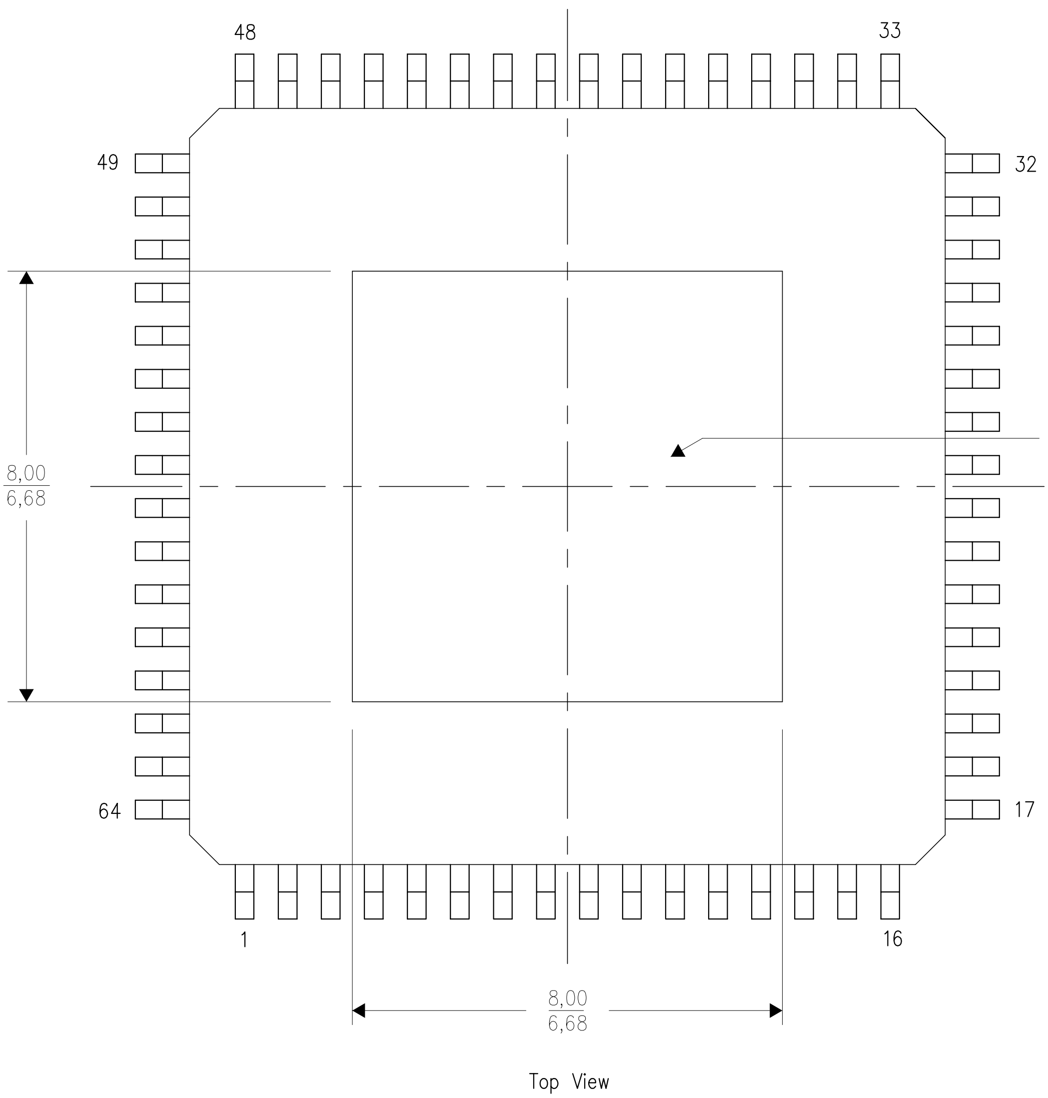
PHD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206328-3/H 04/11

NOTE: A. All linear dimensions are in millimeters

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