DATA SHEET

SunplusIT

SPIF223A

ATA to Serial ATA Bi-direction Bridge

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ATA TO SERIAL ATA BI-DIRECTION BRIDGE

1.GENERAL DESCRIPTION

The SunplusIT SPIF223A is a single-chip solution for bi-direction of ATA to Serial ATA and Serial ATA to ATA device bridge. It is able to accept ATA commands through both ATA and SATA interface as well as decoding the commands and converts them into ATA commands to the device. Response from the device through the serial ATA or ATA bus are deciphered, processed and converted to ATA protocol and sent to the host. The SPIF223A supports the Serial ATA generation 1 transfer rate of 1.5Gb/s (150MB/s) on the serial side and is compatible with Ultra133 on the ATA side.

2.FEATURES

- **Overall Features**
  - Bi-Direction of ATA to Serial ATA bridge chip.
  - Compliant with ATA specification.
  - Compliant with SATA 1.0a specification.
  - Compatible with Ultra ATA 133.
  - Available in a 64-pin TQFP and 64-pin LQFP package.
  - PHY isolation debug mode
  - Full scan for high production test coverage
  - Build-in 8051 uP to control data flow.
  - Supports UART, SPI, I2C bus for internal used only.
  - Supports ATA bus skew-rate programming by UART/SPI interface.[1]

- **Serial ATA Features**
  - Integrated Serial ATA Link and PHY logic.
  - Compliant with Serial ATA 1.0A specifications.
  - Supports Serial ATA Generation 1 transfer rate of 1.5Gb/s.
  - Supports Serial ATA power saving mode: Partial, and Slumber.

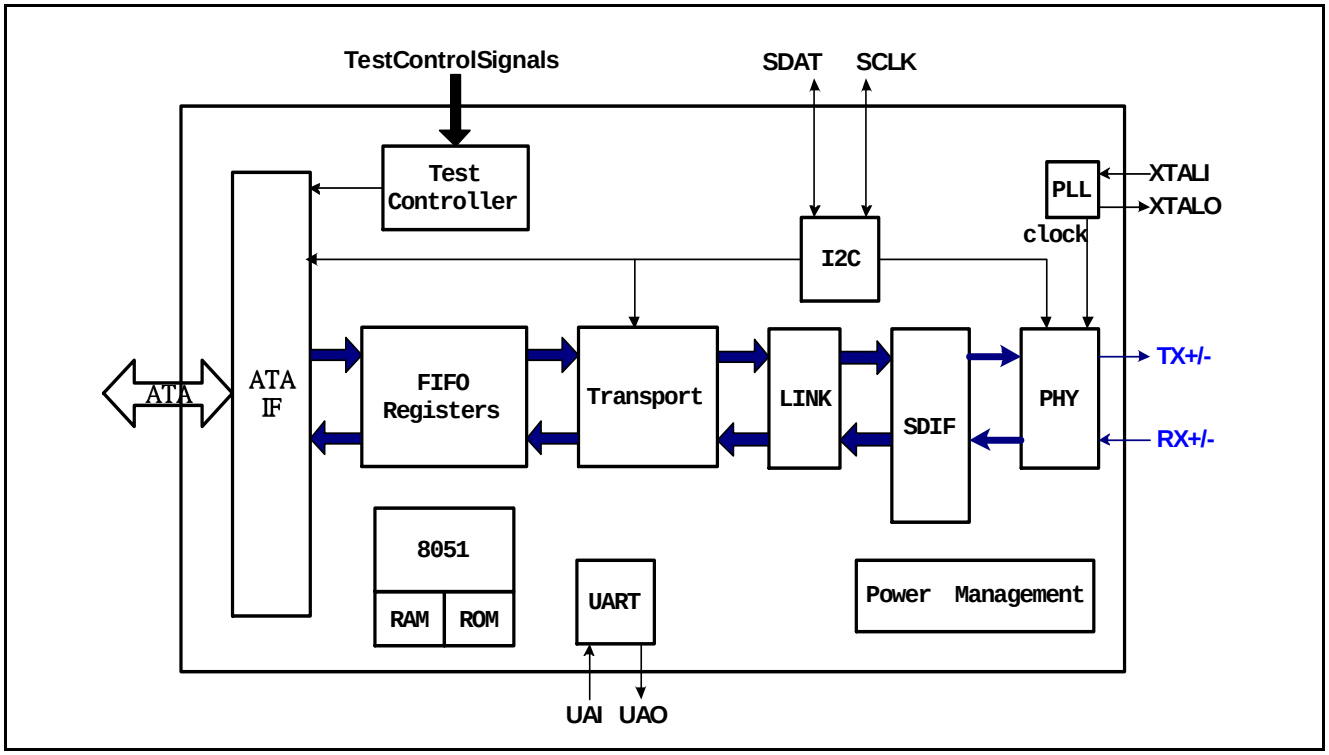
- **ATA Features**
  - Compliant with ATA specifications.
  - Compatible with Ultra ATA 133.
  - Supports PIO mode 0,1,2,3,4, MDMA0,1,2 and Ultra DMA mode 0,1,2,3,4,5,6
  - Supports ATA device master/slave/Chip select emulation.
  - Supports ATA bus timing control.
  - Supports ATA and ATAPI devices, i.e. HDD and ODD, Tape.

3.REFERENCES

For more details about Serial ATA and ATA technology, please refer to the following industry specifications:

- Serial ATA / High Speed Serialized ATA Attachment specification, Revision 1.0a.
- http://www.T13.org/ ATA/ATAPI specifications.

4.FUNCTIONAL BLOCK DIAGRAM



5.SIGNAL DESCRIPTIONS

5.1. Pin Descriptions

Table 5-1: Pin Types

Pin Type	Description
I/O	Bi-directional Pin
I	Regular input
O	Output Pin
A	Analog pin
S	SATA signal pin
PWR	Power pin
GND	Ground pin

Pin resistor	Description
PD	Pin with internal Pull-Down resistor
PU	Pin with internal Pull-Up resistor
PF	Pin floating (without internal resistor)

5.2. Pin List

Table 5-2: SPIF223A Pin Listing

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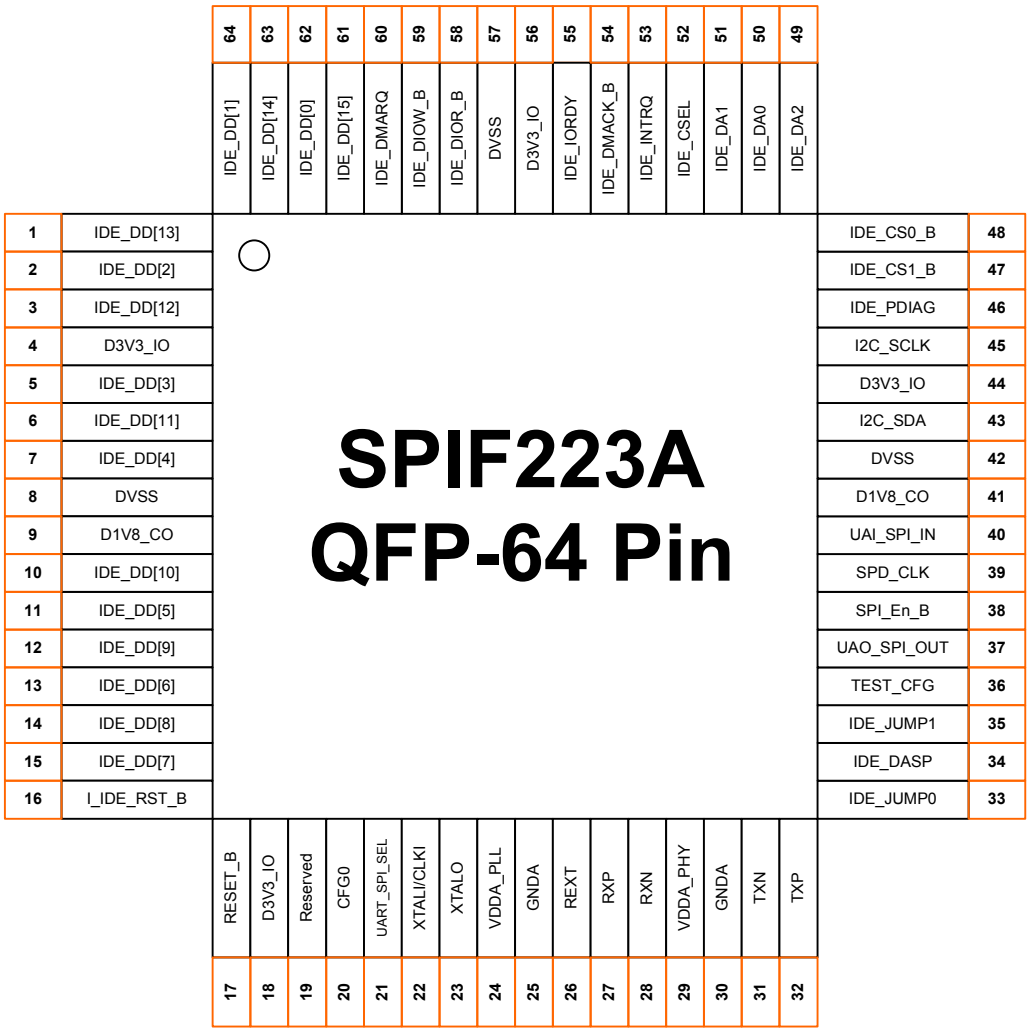
5.3. SPIF223A Pin Diagram



6.ELECTRONICAL SPECIFICATION

6.1. Power Requirement

Table 6-1 : Total Power Dissipation (Typical, 3.3V/1.8V,T_A =25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_{D3V3_IO}	Power supply for digital I/O	3.3v		5	14	mA
I_{D1V8_CO} I_{VDDA_PLL} I_{VDDA_PHY}	Power supply for digital core and analogy power	1.8v		80	85	mA

6.2. Absolute Maximum Ratings

Table 6-2 : Absolute Maximum Ratings (Typical, T_A =25℃)

Symbol	Parameter	Rating		Unit
V_{D3V3_IO}	Digital I/O pad power supply voltage	-0.5	5.5	V
V_{D1V8_CO}	Digital power supply	-0.5	3.3	V
V_{VDDA_PLL}	Analog PLL power supply voltage	-0.5	3.3	V
V_{VDDA_PPHY}	Analog PHY power supply voltage	-0.5	3.3	V
V_I	input signal voltage	-0.5	5.5	V
V_{CLK}	Absolute input signal voltage for XTALI/CLKI	-0.5	3.3	V
T_{STR}	Absolute storage temperature		-65~ 150	℃

6.3. Recommended/Typical Operating Conditions

Table 6-3 : Recommended/Typical Operating Conditions(Typical, 3.3V/1.8V,T_A =25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CORE}	Operating digital power supply voltage		1.71	1.8	1.89	V
V_{IO}	Operating digital I/O pad supply voltage		3.0	3.3	3.6	V
V_{VDDA_PLL}	Operating analog power supply voltage for PLL		1.71	1.8	1.89	V
V_{VDDA_PPHY}	Operating analog power supply voltage for PHY		1.71	1.8	1.89	V
V_I	Operating Input signal voltage		3.0	3.3	3.6	V
T_{OPE}	Operating temperature		0	25	70	℃

6.4. DC Characteristics

Table 6-4 : DC Characteristics(Typical, 3.3V/1.8V,T_A =25℃)

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6.5. SATA Reference resistor Requirement

Table 6-5 : SATA Reference resistor Requirements (Typical, , 3.3V/1.8V , 25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R_{REXT}	REXT of SATA	F_{XTAL} = 25MHz	0.99	1	1.01	K ohm

6.6. Reference Clock Input Requirements

Table 6-6 : Reference clock input spec. (Typical, 3.3V/1.8V,T_A =25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
F_{CLK}	Nominal frequency			25		MHz
V_{CLK}	Operating clock input voltage		1.71	1.8	1.89	V
V_{CLK_IH}	Input high voltage		1.5			V
V_{CLK_IL}	Input low voltage				0.3	V
T_{CLK_J}	CLK frequency tolerance		-50		+50	ppm
T_{CLK_SR}	CLK slew rate		0.2			V/ns
T_{CLK_DUTY}	CLK duty cycle		45		55	%

7.Function description

7.1. SPIF223A UART and SPI interface select:

SPIF223A supports 2 IO interface : UART and SPI. It can be configured by pin21 (UART_SPI_SEL)

UART_SPI_SEL = 0 : Using UART interface.

UART_SPI_SEL= 1 : Using SPI interface.

7.2. SPIF223A direction select:

SPIF223A supports both directions: Serial ATA to ATA host bridge and ATA to Serial ATA host bridge. We could use pin20 (H_D_SEL).

H_D_Sel = 0 : Serial ATA device to ATA host mode (Connecting to ATA HDD).

H_D_Sel = 1 : ATA device to Serial ATA host mode (Connecting to Serial ATA HDD).

7.3. SPIF223A ATA device mode select:

When SPIF223A is selected to H_D_SEL = 1, it will use as ATA device mode. For ATA device, SPIF223A is able to support master, slave and cable select. It is also can be configured by:

Mode	IDE_JUMP0	IDE_JUMP1
Master	0	0
Slave	1	0
Cable Select	1	1

7.4. SPIF223A Serial ATA bus Tri-state feature:

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7.5. SPIF223A ATA bus tri-state feature:

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8.COMMAND LIST

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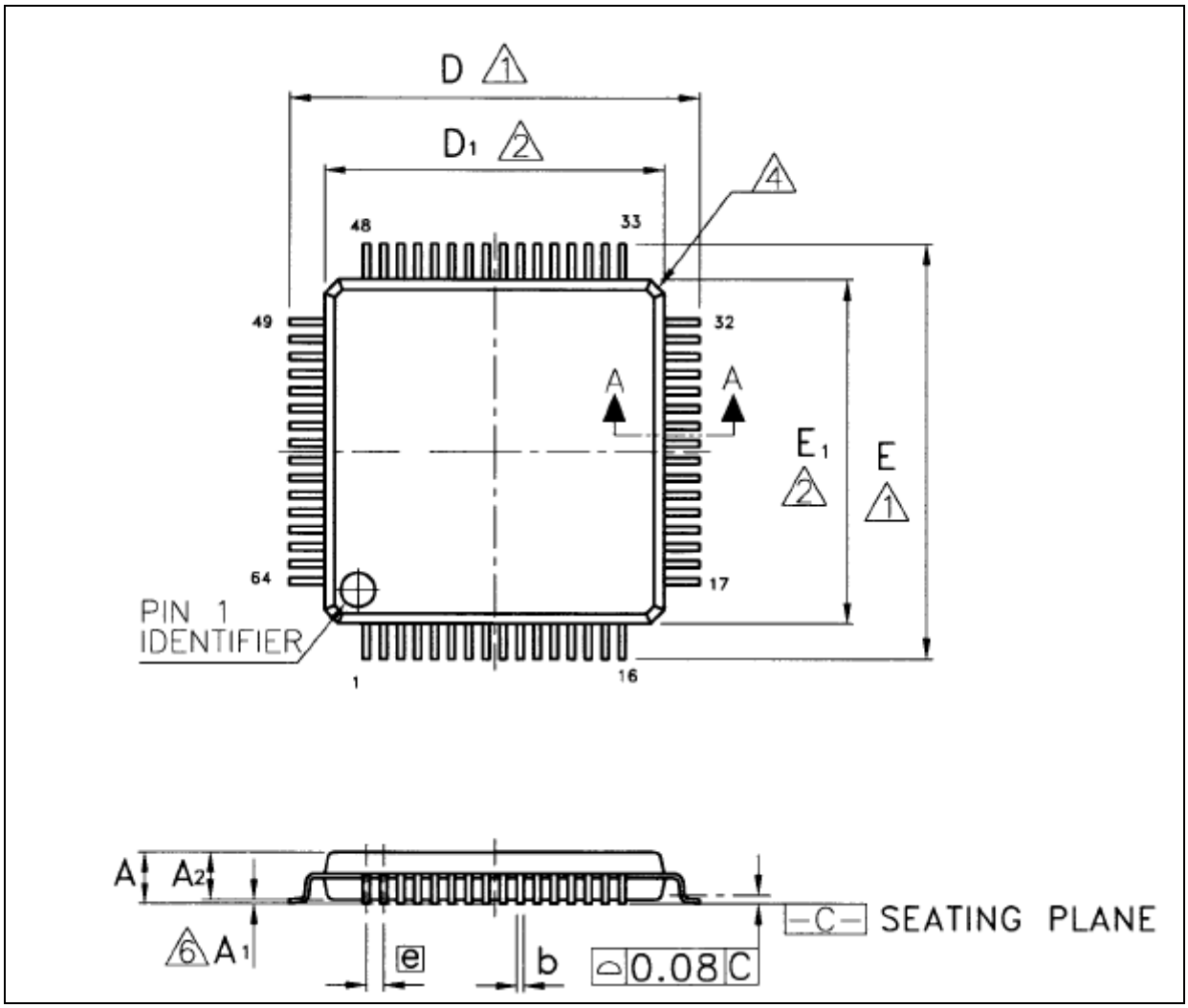
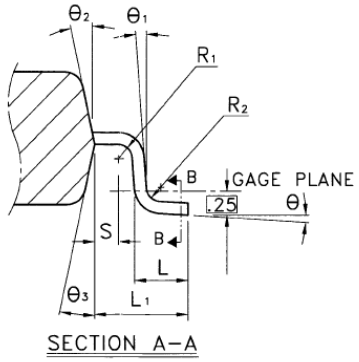
9.PACKAGE/PAD LOCATIONS

9.1. Package Information

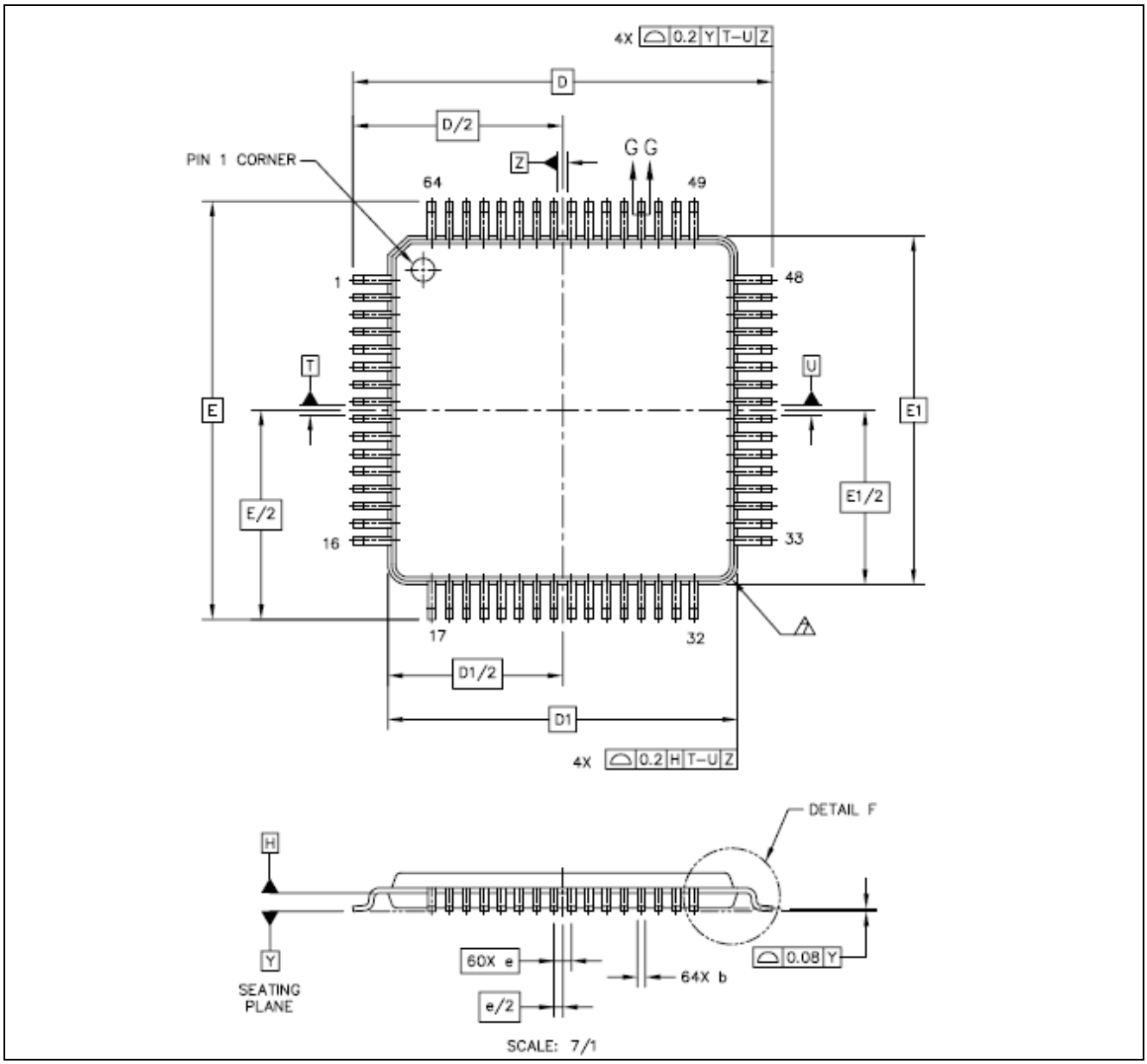
9.1.1. 64 pin LQFP

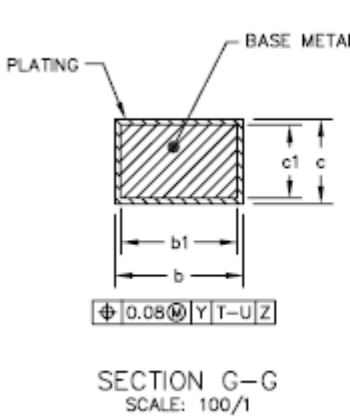


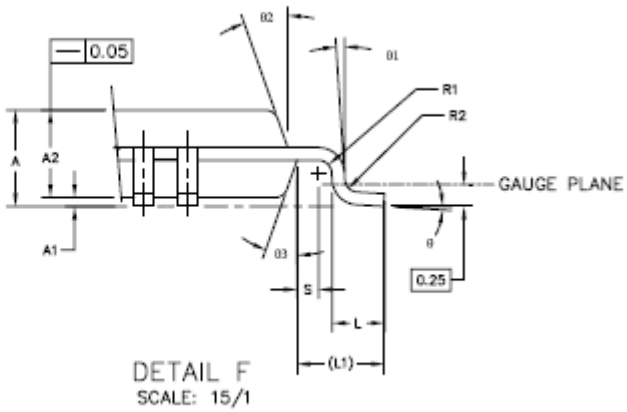


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D_1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E_1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		

9.1.2. 64 pin TQFP







DIM	MIN		MAX
A	---		1.2
A1	0.05		0.15
A2	0.95	1	1.05
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		12 BSC	
D1		10 BSC	
e		0.5 BSC	
E		12 BSC	
E1		10 BSC	
L	0.45	0.6	0.75

DIM	MIN		MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

Fig 9-1: SPIF223A in TQFP package

10. ORDERING INFORMATION

10.1. Part number

Product Number	Package Type
SPIF223A - HF022	Green Package form – TQFP 64 (Without e-PAD)
SPIF223A - HL022	Green Package form – LQFP 64 (without e-PAD)

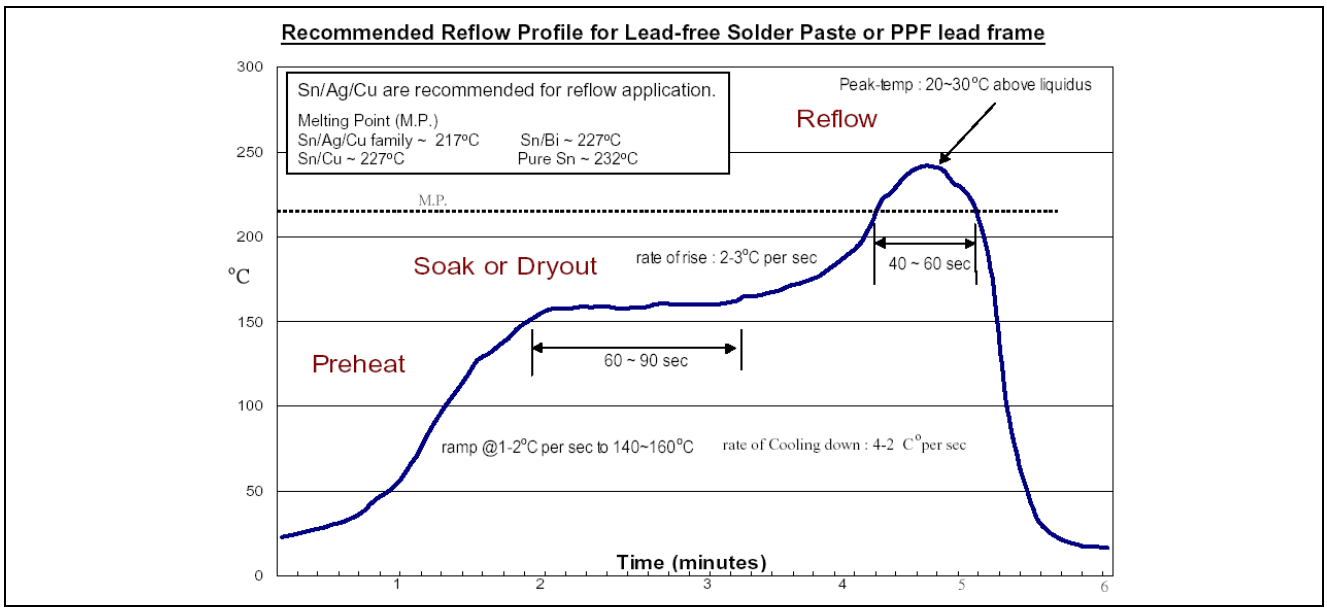
10.2. Storage Condition and Period for Package

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
TQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes
LQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JESD22-A112, or the "CAUTION Note" on dry pack bag.

10.3. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of SUNPLUSIT lead-frame base product choice Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



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12. REVISION HISTORY

Date	Revision #	Description	Page
Nov.30, 2010	2.1_Web	This version is short version from V2.1 for website download purpose. Some chapters keep blank. If Customer want get formal document, please contact agent for service.	
Dec. 31.2008	2.1	Removed statement : Supports Spread Spectrum in receiver Modified/Added Default value and Voltage level in pin list Modified electrical specification Removed QFN64 package and TQFP64 with E-PAD package Modified ordering information.	3 5~8 9~10 16~18 19
JUN. 13 , 2008	2.0	Removed PIO mode 5,6 support Removed ATA invert function support Changed Pin 19 as Reserved pin Modify input type to be regular input Modify V_{IL} and V_{IH} value for regular input type	3,5,6,7,9