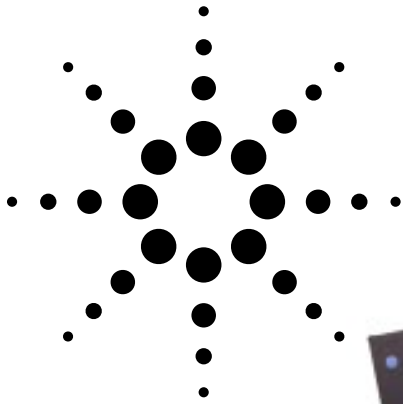


Agilent HDMP-1685A 1.25 Gbps Four Channel SerDes with 5-pin DDR SSTL_2 Parallel Interface Data Sheet



Functional Description

This data sheet describes HDMP-1685A, a 1.25 Gbps, four-channel, 5-pin per channel parallel interface SERDES device. The HDMP-1685A 5-pin parallel interface device enables a single ASIC to drive twice as many channels using half as many parallel lines. This is accomplished without increasing the clock frequency by utilizing the bandwidth on the parallel interface more efficiently.

The HDMP-1685A SERDES is a single silicon bipolar integrated circuit packaged in a 208-pin BGA. This integrated circuit provides a low-cost, small-form-factor physical-layer solution for multi-link 1.25 Gbps cables or optical transceivers. Each IC contains transmit and receive channel circuitry for all four channels.

A 125 MHz LVTTTL reference clock must be supplied to the reference clock input pin, RFCT.

The transmitter section accepts four, 5-bit-wide parallel SSTL_2 data (TX [0:3] [0:4]), a 125 MHz SSTL_2 byte clock (TC) and serializes them into four high-speed serial streams. The parallel data is expected to be “8B/10B” encoded data, or equivalent. TX and TC are source synchronous. New data are accepted on both edges of TC; this is called Double Data Rate (DDR). HDMP-1685A finds a sampling window in between the two edges of TC to latch TX [0:3] [0:4] data into the input register of the transmitter section.

This timing scheme assumes that the driving ASIC and HDMP-1685A operate in the same clock domain. 8B/10B encoded data comes in 10-bit characters. This data is latched onto the 5 TX pins of each channel in 5-bit groups. It is expected that the beginning half of each 10-bit character is latched on the rising edge of TC.

Features

- 5-bit wide Tx, Rx bus pairs
- 208-ball, 23 mm TBGA package
- Parallel data I/O and clocks compatible with SSTL_2 (EIA/JESD8-9)
- 125 MHz TC, RC clocks
- One TC clock for 4 channels
- Single or paired RC clocks
- LVTTTL RefClk input
- Source synchronous clocking of transmit data
- Source centered clocking of receive data
- Double data rate (DDR) parallel transfers
- Parallel loopback
- Differential BLL serial I/O
- Single +3.3 V power supply
- Copper drive capability

Applications

- High density fast ports
- Fast serial backplanes
- Clusters of computers
- Clusters of network units
- Link aggregation, trunks

The transmitter section's PLL locks to the 125 MHz TC. This clock is then multiplied by 10 to generate the 1250 MHz serial clock for the high-speed serial outputs. The high-speed outputs are capable of interfacing directly to copper cables for electrical transmission or to a separate fiber optic module for optical transmission.



The receiver section accepts four serial electrical data streams at 1250 MBd and recovers the respective original 10-bit-wide data for each channel over a 5-pin parallel interface. The receiver PLL locks onto the incoming serial signal and recovers the high-speed serial clock and data. The serial data is converted back into 10-bit parallel data, optionally recognizing the 8B/10B comma character to establish byte alignment. If comma character detection is enabled by raising the SYNC signal high, the receiver section is able to detect comma characters and indicate their presence on each channel with the appropriate SYN [0:3] signal(s).

The recovered parallel data are presented at SSTL_2-compatible outputs RX [0:3] [0:4], and a pair of 125 MHz SSTL_2 clocks, RC [0:3] [1], and RC [0:3] [0], that are 180 degrees out of phase from one another and which represent the remote clock for that channel. Rising edges of RC [0:3] [1] and RC [0:3] [0] may be used to latch RX data at the destination. Alternatively, both edges of either RC [0:3] [1] or RC [0:3] [0] may be used to latch RX data (DDR). When SYNC is high, the beginning half of the comma character shows up at the rising edge of RC [0:3] [1].

The timing of transmit and receive parallel data with respect to TC and RC [0:3] [0:1] is arranged so that the upstream protocol device can generate and latch data very simply. Specifically, in the TX direction, the ASIC drives four sets of 5-pin TX lines and the TC line with the same timing. The

TC line is similar to a 6th data line that is always toggling to provide timing information to the SERDES. On the RX side, the SERDES drives four sets of 5-pin RX data centered between the edges of RC [0:3] [1] or RC [0:3] [0].

For test purposes, the transceiver provides for on-chip parallel loopback functionality controlled through an input pin. Additionally, the byte-edge alignment feature via detection of the positive comma (K28.5+) character may be disabled. This may be useful in proprietary applications that use alternative methods to align the parallel data.

HDMP-1685A Block Diagram

The HDMP-1685A (Figure 2) is designed to transmit and receive 10-bit 8B/10B character data over 5-pin-wide parallel busses via high-speed serial communication lines. The parallel data applied to the transmitter is expected to be encoded per the 8B/10B encoding scheme with special reserve characters for link management purposes. Other encoding schemes will also work as long as they provide dc balance and sufficient number of transitions. In order to accomplish this task, the HDMP-1685A incorporates the following:

- SSTL_2 Parallel Data I/O
- High-Speed Phase Locked Loops
- Parallel-to-Serial Converters
- High-Speed Serial Clock and Data Recovery Circuitry
- Comma Character Recognition Circuitry (K28.5+)
- Byte Alignment Circuitry
- Serial-to-Parallel Converter

PARALLEL INPUT LATCH

For each channel, the transmitter accepts 10-bit characters as two groups of 5-pin single-ended SSTL_2 parallel data at inputs TX [0:3][0:4]. The SSTL_2 TC clock provided by the sender of transmit data is used for all channels as the transmit byte clock. The TX [0:3][0:4] and TC signals must be properly aligned, as shown in Figure 3.

TX PLL/CLOCK GENERATOR

The transmitter Phase Locked Loop and Clock Generator (TX PLL/CLOCK GENERATOR) block generates all internal clocks needed by the transmitter section to perform its functions. These clocks are based on the transmit byte clock (TC). TC is also used to determine the sampling window for the incoming data latches. Incoming data is synchronous with TC (see Figure 3).

FRAME MUX

The FRAME MUX accepts the 10-bit-wide parallel data from the INPUT LATCH. Using internally generated high-speed clocks, this parallel data is multiplexed into the 1250 MBd serial data streams. The data bits are transmitted sequentially, from TX [0] to TX [4]. The leftmost bit of K28.5 is on TX [0].

SERIAL OUTPUT SELECT

The OUTPUT SELECT block provides a parallel loopback mode for testing purposes. In normal operation, PLUP is set low and the serialized TX [0:3] [0:4] data are placed at SO [0:3] +/-.

When parallel wrap-mode is activated by setting PLUP high, the SO [0:3]+/- pins are held static at logic 1 and the serial output signal reflecting TX [0:3] [0:4] data is internally wrapped to the INPUT SELECT block of the receiver section.

SERIAL INPUT SELECT

The INPUT SELECT block determines whether the signal at SI [0:3]+/- or the internal loopback serial signal is used to drive RX [0:3] [0:4]. In normal operation, PLUP is set low and the serial data is accepted at SI [0:3]+/-.

When PLUP is set high, the outgoing high-speed serial signal is internally looped back from the transmitter section to the receiver section. This feature allows parallel loopback testing, exclusive of the transmission medium.

RX PLL/CLOCK RECOVERY

The RX PLL/CLOCK RECOVERY block is responsible for frequency and phase locking onto the incoming serial data stream and recovering the bit and byte clocks. It does this by continually frequency locking onto the 125 MHz reference clock, and then phase locking onto the selected input data stream. An internal signal detection circuit monitors the presence of the input, and invokes the phase detection once the minimum differential input signal level is supplied (AC Electrical Specifications).

Once bit locked, the receiver generates the high-speed sampling clock at 1250 MHz for the input sampler.

SERIAL INPUT SAMPLER

The INPUT SAMPLER converts the serial input signal into a retimed bit stream. In order to accomplish this, it uses the high-speed serial clock recovered from the RX PLL/CLOCK RECOVERY block. This serial bit stream is sent to the FRAME DEMUX AND BYTE SYNC block.

FRAME DEMUX, BYTE SYNC

The FRAME DEMUX AND BYTE SYNC block is responsible for restoring the 10-bit character from the high-speed serial bit stream. This block is also responsible for recognizing the comma character (K28.5+) of positive disparity (0011111xxx). When recognized, the FRAME DEMUX AND BYTE SYNC block works with the RX PLL/CLOCK RECOVERY block to properly select the parallel data edge out of the bit stream so that the comma character starts at RX[0:3][0]. When a comma character is detected and realignment of the receiver byte clock RC[0:3][0:1] is necessary, this clock is stretched, not slivered, to the next possible correct alignment position. This clock will be fully aligned by the start of the second 2-byte or 4-byte ordered set. The second comma character received will be aligned with the rising edge of RC[0:3][1]. Comma characters of positive disparity must not be transmitted in consecutive bytes to allow the receiver byte clocks to maintain their proper recovered frequencies.

PARALLEL OUTPUT DRIVERS

The OUTPUT DRIVERS present the recovered 10-bit character in two groups onto the 5-pin RX bus, properly aligned to the receive byte clock RC [0:3] [0:1] as shown in Figure 5. These output data buffers provide single-ended SSTL_2 compatible signals. Unlike the TX, where all four channels are driven with the same transmit byte clock (TC), each receive channel provides its own clock aligned with its own data, so the recovered clocks may not be phase aligned.

SSTL_2 COMPATIBILITY

HDMP-1685A works with protocol devices whose VDDQ voltage is nominally set at 2.5 Volts. RX [0:3][0:4], RC [0:3][0:1] pins generate output voltages that are compatible with the SSTL_2 standard (EIA/JESD8-9). In addition, these devices provide a VREFR output pin allowing the receiving device to differentially detect a high or a low. The devices receive inputs on their TX [0:3][0:4] and TC pins that are also SSTL_2 compatible. The VREFT input pin is driven by a voltage divider whose supply voltage is at the same level as the VDDQ supply of the protocol device. This allows differential detection of a high or a low at TX parallel inputs.

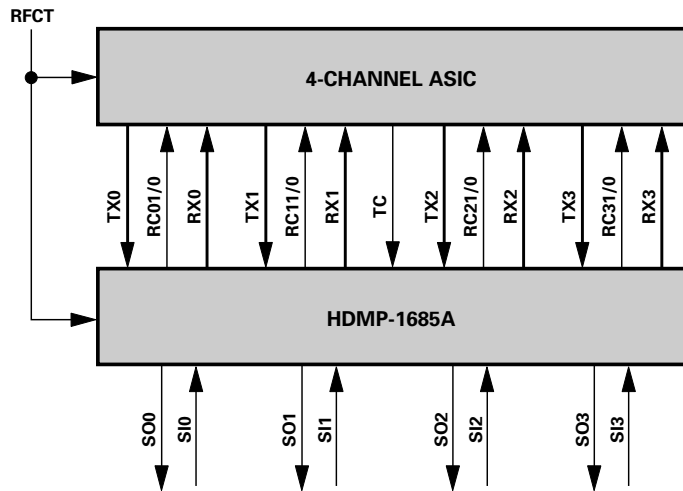


Figure 1. Typical application of the four channel SERDES.

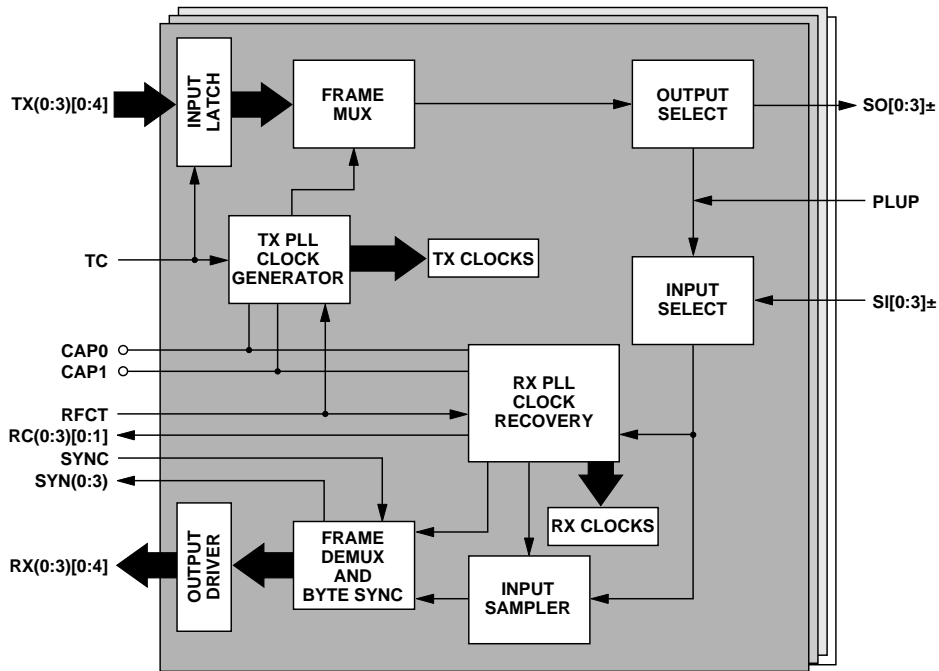


Figure 2. Block diagram of HDMP-1685A.

HDMP-1685A Timing Characteristics – Transmitter Sections

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Min. | Typ. | Max. |
|-------------------|--|-------|------|------|------|
| $t_{TXCT}^{[2]}$ | TX [0:3][0:4] Input Data and TC Clock Transition Range | ps | | | 1600 |
| $t_{TXCV}^{[2]}$ | TX [0:3][0:4] Input Data and TC Clock Valid Time | ps | 2400 | | |
| $t_{txlat}^{[1]}$ | Transmitter Latency | ns | | 4 | |
| | | bits | | 5 | |

Note:

1. The transmitter latency, as shown in Figure 4, is defined as the time between the leading edge of the first half of a parallel 10-bit word and the leading edge of the first transmitted serial output bit of that 10-bit word.
2. Agilent's HDMP-1685A internally generates another clock which is 90 degrees out of phase with the TC clock supplied. This clock, which will have its edges at the center of the data valid eye, is used to clock in the TX[0:4] data. Setup and hold times are taken care of by the HDMP-1685A provided the specifications indicated are met.

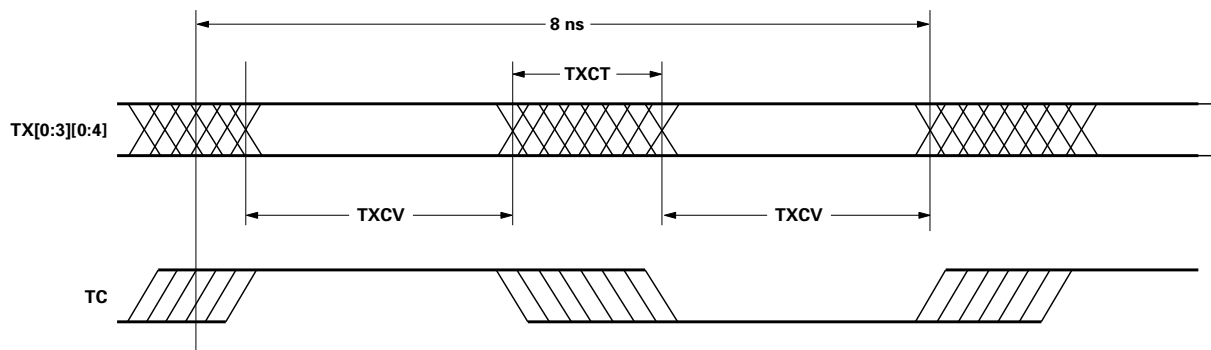


Figure 3. Transmitter section parallel input timing.

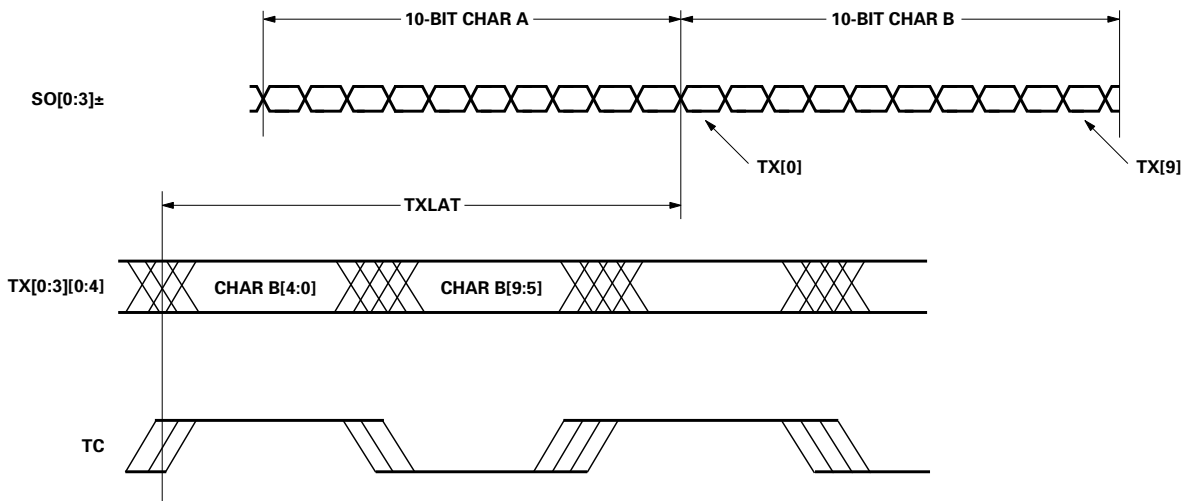


Figure 4. Transmitter section latency. TX[0] is first on serial wire.

HDMP-1685A Timing Characteristics – Receiver Sections – Rising Edge Clocking

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Min. | Typ. | Max. |
|-----------------------------------|--|---------------|------|----------|------|
| f_lock | Frequency Lock at Powerup | μs | | | 500 |
| B_sync ^[1,2] | Bit Sync Time | bits | | | 2500 |
| t _{RXS} | RX [0:3][0:4] Setup Time (Data Valid Before Clock) | ps | 1200 | | |
| t _{RXH} | RX [0:3][0:4] Hold Time (Data Valid After Clock) | ps | 800 | | |
| | RC [0:3][1] to RC [0:3][0] Skew | ns | 3.5 | | 4.5 |
| | RC [0:3][1] and RC [0:3][0] Duty Cycle | % | 40 | | 60 |
| t _{rxlat} ^[3] | Receiver Latency | ns bits | | 16 20 | |

Notes:

1. This is the recovery time for input phase jumps, per the Fibre Channel Specification X3.230-1994 FC-PH Standard, Sec 5.3.
2. Tested using $C_{PLL} = 0.1\ \mu\text{F}$.
3. The receiver latency, as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, RC [0:1]).

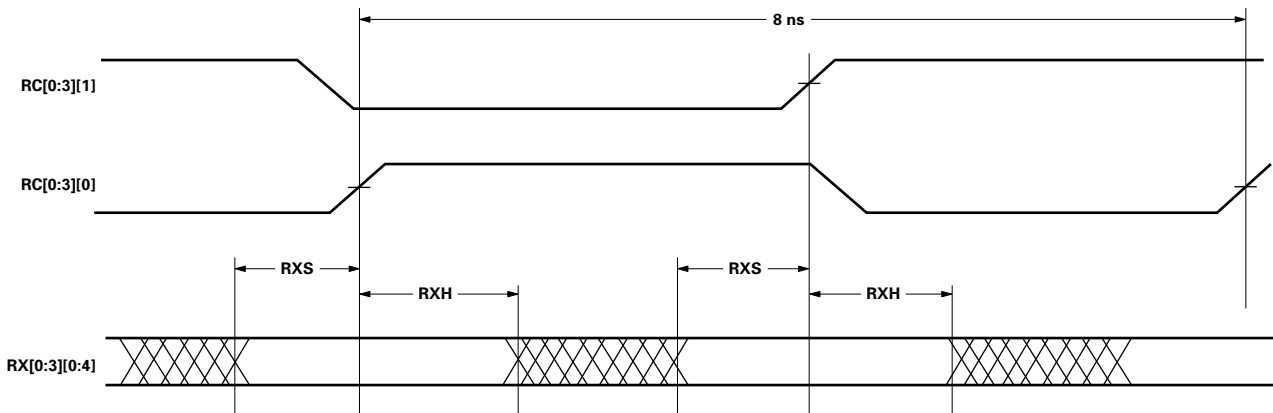


Figure 5a. Receiver section parallel output timing using rising edge of both RC[0:3][0] and RC[0:3][1].

HDMP-1685A Timing Characteristics – Receiver Sections – Rising and Falling Edge Clocking

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Min. | Typ. | Max. |
|-----------------------------------|--|---------------|------|------|------|
| f_lock | Frequency Lock at Powerup | μs | | | 500 |
| B_sync ^[1,2] | Bit Sync Time | bits | | | 2500 |
| t _{RXS} | RX [0:3][0:4] Setup Time (Data Valid Before Clock) | ps | 1000 | | |
| t _{RXH} | RX [0:3][0:4] Hold Time (Data Valid After Clock) | ps | 800 | | |
| | RC [0:3][1] and RC [0:3][0] Duty Cycle | % | 40 | | 60 |
| t _{rxlat} ^[3] | Receiver Latency | ns | | 16 | |
| | | bits | | 20 | |

Notes:

1. This is the recovery time for input phase jumps, per the Fibre Channel Specification X3.230-1994 FC-PH Standard, Sec 5.3.
2. Tested using $C_{PLL} = 0.1\ \mu\text{F}$.
3. The receiver latency, as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, RC [0:1]).

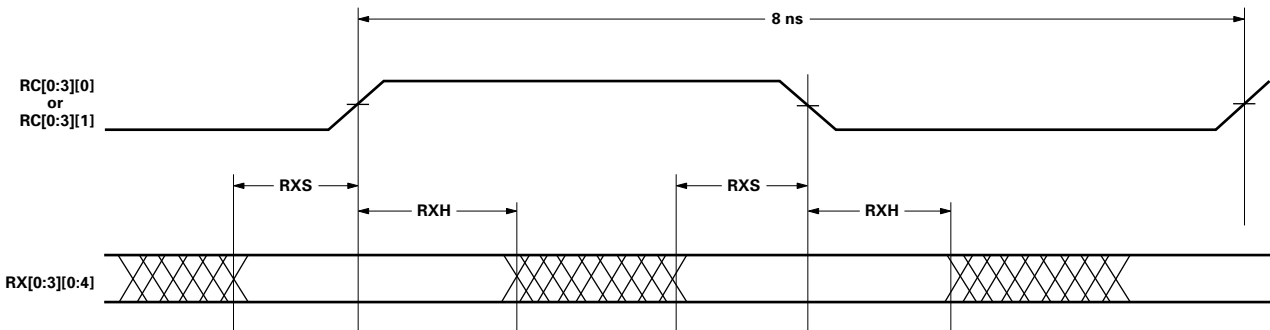


Figure 5b. Receiver section parallel output timing using rising and falling edge of either RC[0:3][0] or RC[0:3][1].

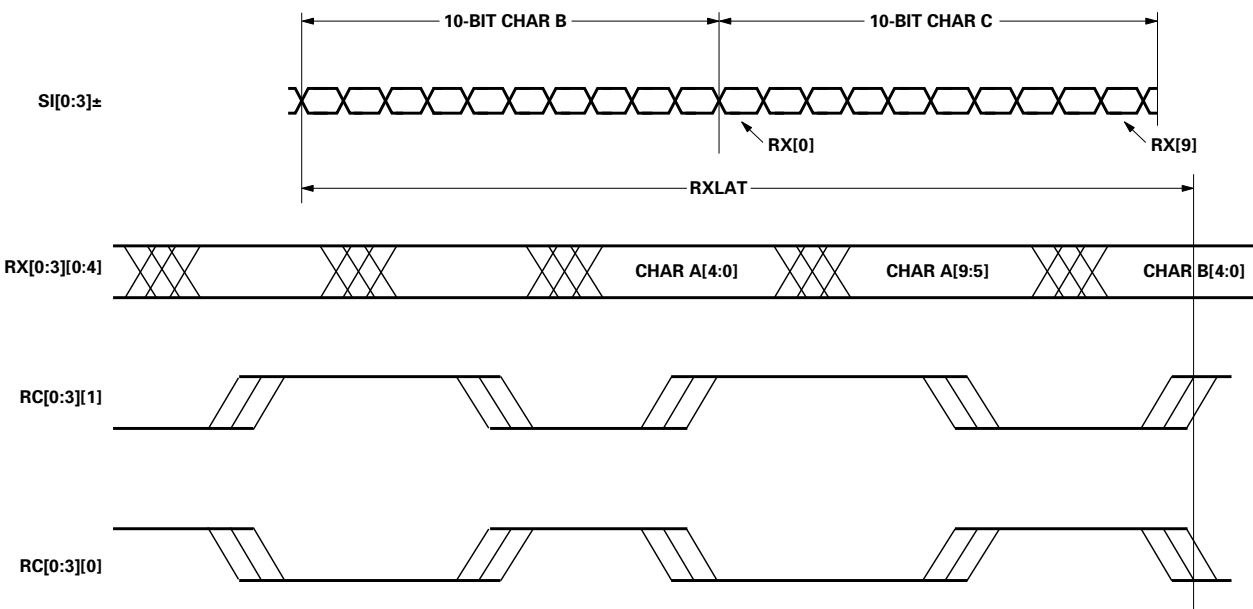


Figure 6. Receiver section latency. First bit on serial wire drives RX[0:3][0].

HDMP-1685A Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$, except as specified. Sustained operation at or beyond any of these conditions may result in long-term reliability degradation or permanent damage, and is not recommended.

| Symbol | Parameter | Units | Min. | Max. |
|-----------------|------------------------------------|------------------|------|----------------|
| V_{CC} | Supply Voltage | V | -0.5 | 5.0 |
| $V_{IN,LVTTL}$ | RFCT LVTTTL Input Voltage | V | -0.7 | $V_{CC} + 2.8$ |
| $V_{IN,SSTL}$ | SSTL Input Voltage | V | -0.7 | $V_{CC} + 0.7$ |
| V_{IN,HS_IN} | HS_IN Input Voltage (Differential) | V | | 2.2 |
| T_{stg} | Storage Temperature | $^\circ\text{C}$ | -65 | +150 |
| T_j | Junction Temperature | $^\circ\text{C}$ | 0 | +125 |
| T_C | Case Temperature | $^\circ\text{C}$ | 0 | 95 |

HDMP-1685A Guaranteed Operating Rates

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Parallel Clock Rate (MHz) | | Serial Baud Rate (MBaud) | |
|---------------------------|-------|--------------------------|------|
| Min. | Max. | Min. | Max. |
| 124.0 | 126.0 | 1240 | 1260 |

HDMP-1685A Reference Clock and Transmit Byte Clock Requirements

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Min. | Typ. | Max. |
|--------------|---|-------|------|------|------|
| f | Nominal Frequency | MHz | | 125 | |
| F_{tol} | Frequency Tolerance | ppm | -100 | | +100 |
| $Symm_{RFC}$ | Symmetry (Duty Cycle) Reference Clock | % | 40 | | 60 |
| $Symm_{TC}$ | Symmetry (Duty Cycle) Transmit Byte Clock | % | 40 | | 60 |

HDMP-1685A LVTTTL I/O DC Electrical Specifications

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Min. | Typ. | Max. |
|----------------|--|---------------|------|------|----------|
| $V_{IH,LVTTL}$ | LVTTTL Input High Voltage Level, Guaranteed High Signal for All Inputs | V | 2 | | 5.5 |
| $V_{IL,LVTTL}$ | LVTTTL Input Low Voltage Level, Guaranteed Low Signal for All Inputs | V | 0 | | 0.8 |
| $V_{OH,LVTTL}$ | LVTTTL Output High Voltage Level, $I_{OH} = -400\ \mu\text{A}$ | V | 2.2 | | V_{CC} |
| $V_{OL,LVTTL}$ | LVTTTL Output Low Voltage Level, $I_{OL} = 1\text{ mA}$ | V | 0 | | 0.5 |
| $I_{IH,LVTTL}$ | Input High Current, $V_{IN} = 2.4\text{ V}$, $V_{CC} = 3.45\text{ V}$ | μA | | | 40 |
| $I_{IL,LVTTL}$ | Input Low Current, $V_{IN} = 0.4\text{ V}$, $V_{CC} = 3.45\text{ V}$ | μA | | | -600 |

HDMP-1685A SSTL_2 I/O DC Electrical Parameters

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V , $V_{DDQ} = 2.30\text{ V}$ to 2.70 V . V_{DDQ} is the FC-1/MAC device I/O supply voltage. SSTL-2 inputs can receive LVTTTL signals successfully. SSTL-2 outputs do not output LVTTTL compliant levels.

| Symbol | Parameter | Units | Min. | Typ. | Max. |
|----------|---------------------------------|-------|-------------|------|-------------|
| VREFT | SSTL_2 Input Reference Voltage | V | 1.15 | 1.25 | 1.35 |
| V_{IH} | Input High Voltage | V | VREFT +0.18 | | VDDQ +0.30 |
| V_{IL} | Input Low Voltage | V | -0.30 | | VREFT -0.18 |
| VREFR | SSTL_2 Output Reference Voltage | V | 1.15 | 1.25 | 1.35 |
| V_{OH} | Output High Voltage | V | VREFR +0.38 | | VDDQ |
| V_{OL} | Output Low Voltage | V | GND | | VREFR -0.38 |

HDMP-1685A AC Electrical Specifications (TRx)

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Min. | Typ. | Max. |
|------------------------|--|-------|------|------|------|
| $t_{r,RFCT}$ | RFCT LVTTTL Input Rise Time, 0.8 to 2.0 Volts | ns | 0 | | 2.4 |
| $t_{f,RFCT}$ | RFCT LVTTTL Input Fall Time, 2.0 to 0.8 Volts | ns | 0 | | 2.4 |
| $t_{r,SSTLo}$ | SSTL Output Rise Time, 1.0 V to 1.6 V | ns | | 0.4 | 1.5 |
| $t_{f,SSTLo}$ | SSTL Output Fall Time, 1.6 V to 1.0 V | ns | | 0.28 | 1.5 |
| t_{rs,HS_OUT} | HS_OUT Single-Ended (SO[0:3] \pm) Rise Time (20% - 80%) | ps | 85 | 205 | 300 |
| t_{fs,HS_OUT} | HS_OUT Single-Ended (SO[0:3] \pm) Fall Time (20% - 80%) | ps | 85 | 180 | 300 |
| t_{rd,HS_OUT} | HS_OUT Differential Rise Time | ps | 85 | | 300 |
| t_{fd,HS_OUT} | HS_OUT Differential Fall Time | ps | 85 | | 300 |
| V_{IP,HS_IN} | HS_IN (SI[0:3] \pm) Input Peak-To-Peak Differential Voltage | mV | 200 | 1200 | 2000 |
| $V_{OP,HS_OUT}^{[1]}$ | HS_OUT Output Pk-Pk Diff. Voltage ($Z_0=50\text{ Ohms}$, Fig.10) | mV | 1000 | 1300 | 1800 |

Note:

- Output Peak-to-Peak Differential Voltage specified as SO[0:3]+ minus SO[0:3]-. The amplitude will be 25% higher when terminating into 75 Ω loads.

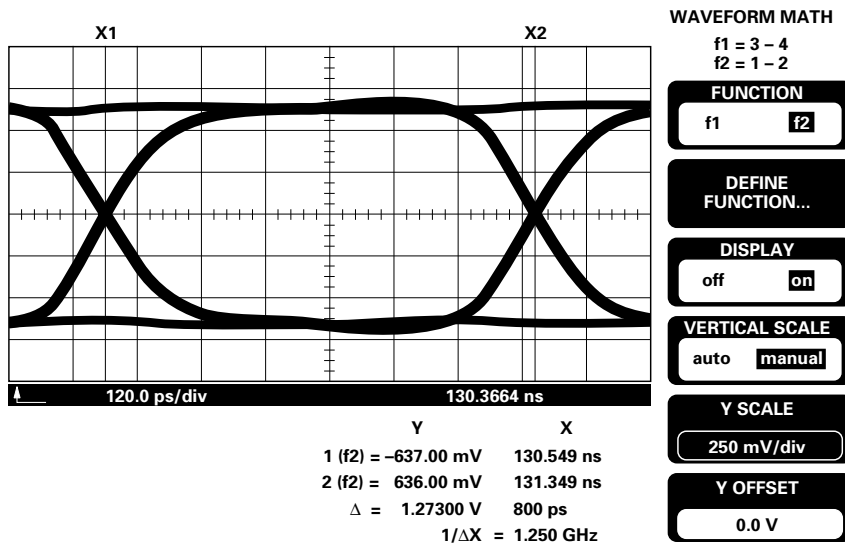


Figure 7. Eye diagram of a high speed differential output.

HDMP-1685A Output Jitter Characteristics – Transmitter Section

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Typ. |
|-------------------|--|-------|------|
| RJ ^[1] | Random Jitter at DOUT, the High Speed Electrical Data Port, specified as 1 sigma deviation of the 50% crossing point (RMS) | ps | 11 |
| DJ ^[1] | Deterministic Jitter at DOUT, the High Speed Electrical Data Port (pk-pk) | ps | 26 |

Note:

1. Defined by Fibre Channel Specification X3.230-1994 FC-PH Standard, Annex A, Section A.4 and tested using measurement method shown in Figure 8.

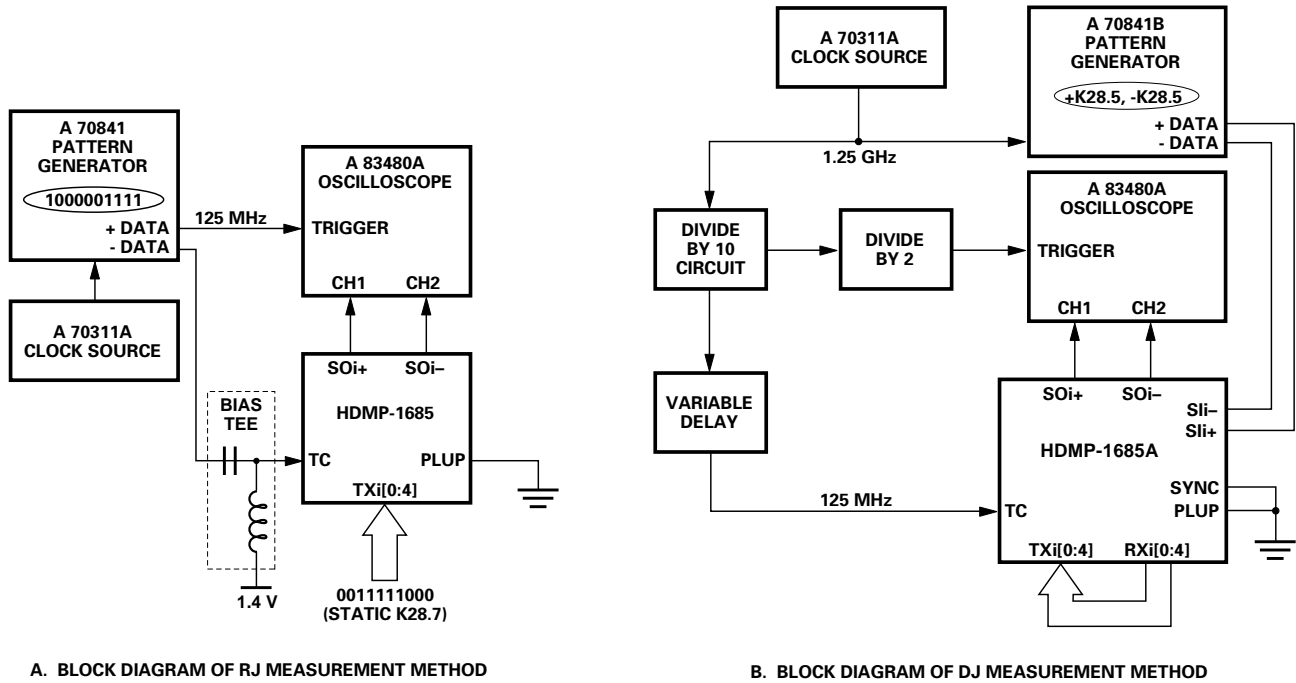


Figure 8. Transmitter jitter measurement method.

HDMP-1685A Thermal and Power Temperature Characteristics (TRx)

$T_A = 0^\circ\text{C}$ to $T_C = 85^\circ\text{C}$, $V_{CC} = 3.15\text{ V}$ to 3.45 V

| Symbol | Parameter | Units | Typ. | Max. |
|------------------------------|--|---------------------------|------|------|
| $I_{CC,TRx}$ | Transceiver V_{CC} Supply Current, $T_A = 25^\circ\text{C}$ | mA | 900 | |
| $P_{D,TRx}$ ^[1] | Transceiver Power Dissipation, Outputs Connected per Recommended Bias Terminations with 2 ⁷ -1 PRBS Pattern | W | 2.97 | 3.5 |
| Θ_{jC} ^[1] | Thermal Resistance, Junction to Case | $^\circ\text{C}/\text{W}$ | 7.8 | |
| T_j | Junction Temperature (absolute maximum) | $^\circ\text{C}$ | 0 | +125 |
| T_C | Case Temperature (absolute maximum) | $^\circ\text{C}$ | 0 | +95 |

Note:

1. Based on independent package testing by Agilent. Θ_{ja} for these devices is $36^\circ\text{C}/\text{W}$ for the HDMP-1685A. Θ_{ja} is measured on a standard 3x3" FR4 PCB in a still air environment. To determine the actual junction temperature in a given application, use the following: $T_j = T_c + (\Theta_{jC} \times P_D)$, where T_c is the case temperature measured on the top center of the package and P_D is the power being dissipated.

HDMP-1685A I/O Type Definitions

| I/O Type | Definition |
|----------|--|
| I-LVTTL | Input LVTTTL, floats high when left open |
| I-SSTL2 | Input SSTL_2, floats low when left open |
| O-SSTL2 | Output SSTL_2 |
| HS_OUT | 50 Ω matched Output Driver. Will drive AC coupled 50 Ω loads. PECL level compatible (Figure 10). |
| HS_IN | PECL level compatible. Must be AC coupled (Figure 10). |
| C | External Circuit Node |
| S | Power Supply or Ground |

HDMP-1685A Pin Input Capacitance (TRx)

| Symbol | Parameter | Units | Typ. | Max. |
|--------------------|--------------------------------------|-------|------|------|
| C _{INPUT} | Input Capacitance on SSTL input pins | pF | 1.6 | |

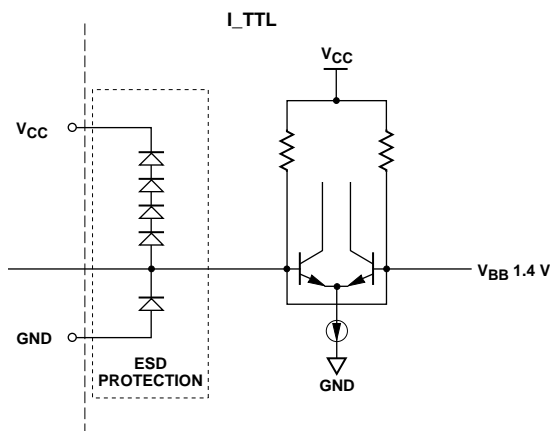
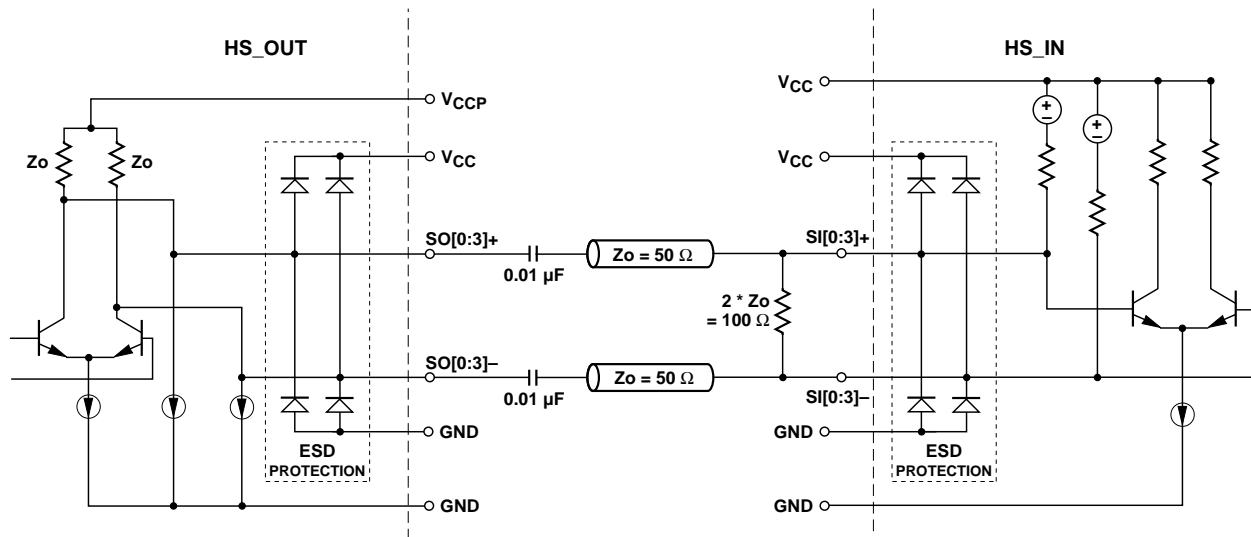


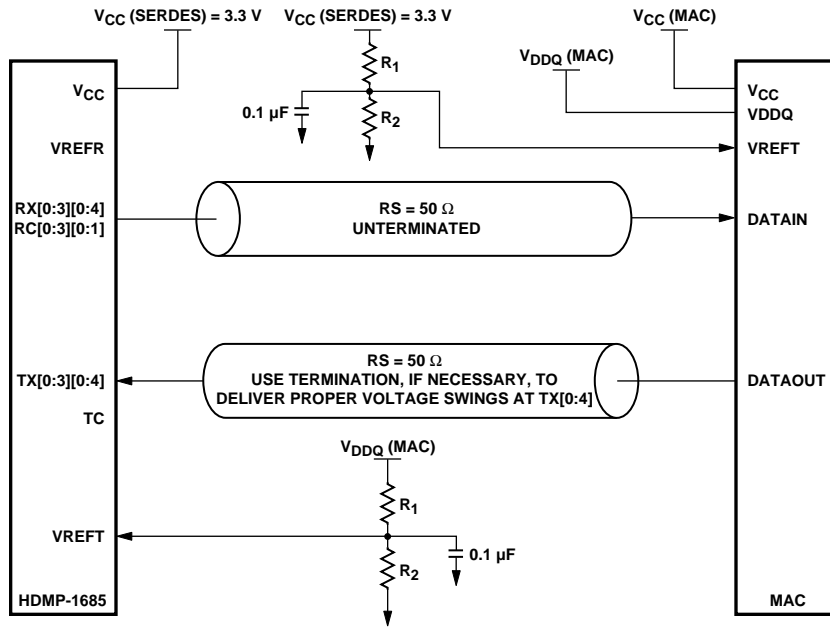
Figure 9. LVTTL input simplified circuit schematic (for RFCT).



NOTES:

1. HS_IN INPUTS SHOULD NEVER BE CONNECTED TO GROUND AS PERMANENT DAMAGE TO THE DEVICE MAY RESULT.
2. CAPACITORS MAY BE PLACED AT THE SENDING END OR THE RECEIVING END.

Figure 10. HS_OUT and HS_IN simplified circuit schematic.



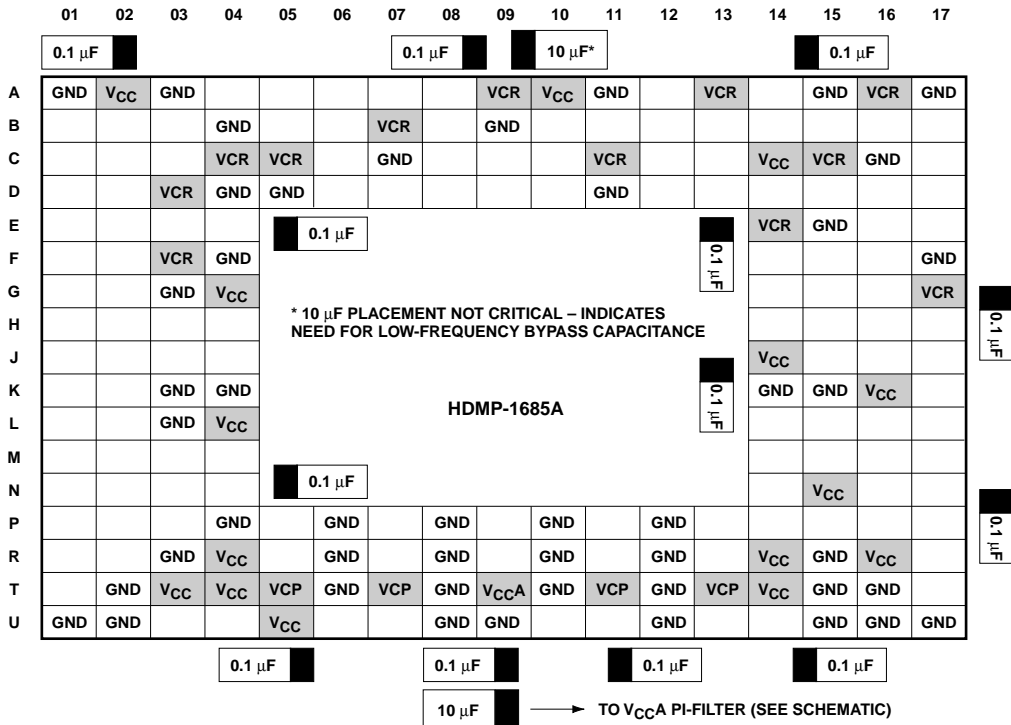
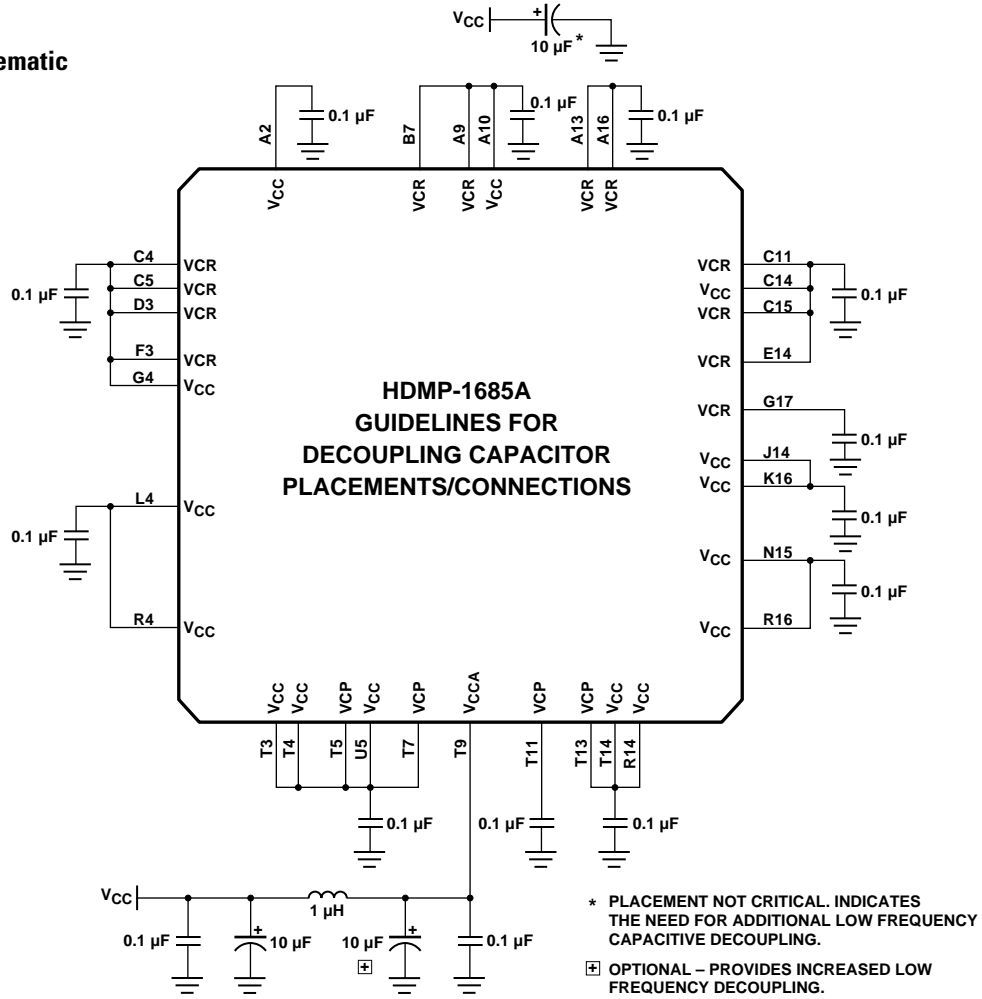
NOTE: VREFR ON EACH DEVICE MAY BE USED TO DRIVE VREFT ON THE OTHER DEVICE INSTEAD OF USING THE CONFIGURATION ABOVE. VREFR SHOULD BE BYPASSED WITH 0.1 μF IN THIS CASE. IF USED, R₁ AND R₂ SHOULD BE 500-1000 Ω. 1% RESISTORS SHOULD BE USED FOR R₁ AND R₂. WHEN USING THE CONFIGURATION ABOVE, VREFT TO THE MAC SHOULD BE SET TO 1.25 V NOMINAL. USING THIS VALUE CENTERS VREFR RELATIVE TO THE RX[0:3][0:4] OUTPUT SWINGS PROVIDED BY THE HDMP-1685A.

Figure 11. 0-SSTL_2 and 1-SSTL_2 simplified circuit schematic.

| | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|------|-----------------|-----------------|-----------------|-----------------|------|------|------------------|------------------|-----------------|------|------|------|-----------------|------|-----------------|------|------|
| A | GND | V _{CC} | GND | SYN1 | RC10 | RX10 | RX14 | | VCR1 | V _{CC} | GND | RX21 | VCR2 | | GND | VCR2 | GND | |
| B | | | | GND | RC11 | RX11 | VCR1 | | GND | SYN2 | RX20 | RX22 | | | SYN3 | RC30 | RC31 | |
| C | RX04 | | | VCR0 | VCR1 | RX12 | GND | | | RC20 | VCR2 | RX23 | | V _{CC} | VCR3 | GND | RX30 | |
| D | RX00 | RX01 | VCR0 | GND | GND | RX13 | VRFR | | | RC21 | GND | RX24 | | RX31 | RX32 | RX33 | RX34 | |
| E | RC00 | RC01 | RX02 | RX03 | | | | | | | | | | VCR3 | GND | | | |
| F | | SYN0 | VCR0 | GND | | | | | | | | | | | | | GND | |
| G | | | GND | V _{CC} | | | | GND | | | | | | | TX22 | TX21 | TX20 | VCR3 |
| H | TX14 | | | | | | | GNDA | | | | | | | | | TX24 | TX23 |
| J | TX10 | TX11 | TX12 | TX13 | | | | V _{CCP} | | | | | | V _{CC} | | | | |
| K | | | GND | GND | | | | V _{CC} | | | | | | GND | GND | V _{CC} | TC | |
| L | | | GND | V _{CC} | | | | V _{CCA} | | | | | | TX33 | TX32 | TX31 | TX30 | |
| M | TX04 | | | | | | | VCR | | | | | | | | | | TX34 |
| N | TX00 | TX01 | TX02 | TX03 | | | | | | | | | | | PLUP | V _{CC} | | |
| P | VRFT | | | GND | SO0- | GND | SO1- | GND | CAP0 | GND | SO2+ | GND | SO3+ | | | | | |
| R | RFCT | | GND | V _{CC} | SO0+ | GND | SO1+ | GNDA | CAP1 | GND | SO2- | GND | SO3- | V _{CC} | GND | V _{CC} | SYNC | |
| T | | GND | V _{CC} | V _{CC} | VCP0 | GND | VCP1 | GND | V _{CCA} | GND | VCP2 | GND | VCP3 | V _{CC} | GND | GND | | |
| U | GND | GND | SIO- | SIO+ | V _{CC} | S11- | S11+ | GND | GND | S12- | S12+ | GND | S13- | S13+ | GND | GND | GND | |

Figure 12. Pinout of HDMP-1685A (top view).

Filtering Schematic



HDMP-1685A TRx I/O Definition

| Name | Pin | Type | Signal |
|------|-----|---------|--|
| CAP0 | P09 | C | Loop Filter Capacitor: A loop filter capacitor for the internal PLLs must be connected across the CAP0 and CAP1 pins. (typical value = 0.1 μ F) |
| CAP1 | R09 | | |
| PLUP | N14 | I-SSTL2 | Parallel Loopback Enable Input: When set high, a high-speed serial signal from the transmitter section's serial output select block, reflecting TX data, is driven to the receiver section's serial input select block. RX data reflects this serial signal. Also when in parallel loopback mode, the SO [0:3]+/- outputs are held static at logic 1. |
| RFCT | R01 | I-LVTTL | LVTTTL Reference Clock: RFCT is a 125 MHz clock signal supplied to the IC. |
| RC00 | E01 | O-SSTL2 | Receiver Byte Clocks: The receiver sections drive 125 MHz receive byte clocks RC [0:3] [0:1]. |
| RC01 | E02 | | |
| RC10 | A05 | | |
| RC11 | B05 | | |
| RC20 | C10 | | |
| RC21 | D10 | | |
| RC30 | B16 | | |
| RC31 | B17 | | |
| RX00 | D01 | | |
| RX01 | D02 | | |
| RX02 | E03 | | |
| RX03 | E04 | | |
| RX04 | C01 | | |
| RX10 | A06 | | |
| RX11 | B06 | | |
| RX12 | C06 | | |
| RX13 | D06 | | |
| RX14 | A07 | | |
| RX20 | B11 | | |
| RX21 | A12 | | |
| RX22 | B12 | | |
| RX23 | C12 | | |
| RX24 | D12 | | |
| RX30 | C17 | | |
| RX31 | D14 | | |
| RX32 | D15 | | |
| RX33 | D16 | | |
| RX34 | D17 | | |
| SI0+ | U04 | HS_IN | Serial Data Inputs: High-speed inputs. Serial data are accepted from the SI [0:3]+/- inputs except when PLUP is high. |
| SI0- | U03 | | |
| SI1+ | U07 | | |
| SI1- | U06 | | |
| SI2+ | U11 | | |
| SI2- | U10 | | |
| SI3+ | U14 | | |
| SI3- | U13 | | |

HDMP-1685A TRx I/O Definition, continued

| Name | Pin | Type | Signal |
|-------|-----|---------|--|
| S00+ | R05 | HS_OUT | Serial Data Outputs: High-speed outputs. These lines are active except when PLUP is high, in which case these outputs are held static at logic 1. |
| S00- | P05 | | |
| S01+ | R07 | | |
| S01- | P07 | | |
| S02+ | P11 | | |
| S02- | R11 | | |
| S03+ | P13 | | |
| S03- | R13 | | |
| SYNC | R17 | I-SSTL2 | Enable Byte Sync Input: When high, turns on the internal byte sync functions to allow clock synchronization to a comma character of positive disparity (0011111XXX). When the line is low, the function is disabled and will not reset registers and clocks, or strobe the SYN [0:3] lines. |
| SYN0 | F02 | O-SSTL2 | Byte Sync Outputs: Active high outputs. Used to indicate detection of a comma character of positive disparity (0011111XXX) when SYNC is enabled. |
| SYN1 | A04 | | |
| SYN2 | B10 | | |
| SYN3 | B15 | | |
| TC | K17 | I-SSTL2 | Transmit Byte Clock: This signal is used to latch transmit data for all channels into the IC. |
| TX00 | N01 | I-SSTL2 | Data Inputs: Four 5-pin data busses. TX [0:3] [0] are the first bits transmitted. |
| TX01 | N02 | | |
| TX02 | N03 | | |
| TX03 | N04 | | |
| TX04 | M01 | | |
| TX10 | J01 | | |
| TX11 | J02 | | |
| TX12 | J03 | | |
| TX13 | J04 | | |
| TX14 | H01 | | |
| TX20 | G16 | | |
| TX21 | G15 | | |
| TX22 | G14 | | |
| TX23 | H17 | | |
| TX24 | H16 | | |
| TX30 | L17 | | |
| TX31 | L16 | | |
| TX32 | L15 | | |
| TX33 | L14 | | |
| TX34 | M17 | | |
| VREFT | P01 | I-S | TX Parallel Interface SSTL_2 Reference Voltage: Voltage reference derived from 2 resistor network with V _{DDQ} (ASIC) as supply, as recommended in Figure 11. |
| VREFR | D07 | O-S | RX Parallel Interface SSTL_2 Reference Voltage: Provided by HDMP-1685A. Drives the VREF input of the ASIC. |

HDMP-1685A TRx I/O Definition, continued

| Name | Pin | Type | Signal |
|------------------------------|---|-------------|---|
| V _{CC} | A02 A10 C14 G04 J14 K16 L04 N15 R04 R14 R16 T03 T04 T14 U05 | S | Power Supply: Normally 3.3 volts. Used for logic, SSTL inputs, and LVTTTL I/O. |
| VCCA | T09 | S | Analog Power Supply: Normally 3.3 volts. Used to provide a clean supply line for the PLLs and high-speed analog cells. |
| VCR0 | C04 D03 F03 | S | Rx SSTL2 Output Power Supply: Normally 3.3 volts. Used for all SSTL2 receiver output buffer cells. |
| VCR1 | A09 B07 C05 | | |
| VCR2 | A13 A16 C11 | | |
| VCR3 | C15 E14 G17 | | |
| VCP0 VCP1 VCP2 VCP3 | T05 T07 T11 T13 | S | High-Speed Output Supply: Normally 3.3 volts. Used only for the last stage of the high-speed transmitter output cells (HS_OUT) as shown in Figure 10. Due to high current transitions, this V _{CC} should be well bypassed to a ground plane. |
| GNDA | R08 | S | Analog Ground: Normally 0 volts. All GND pads on the chip are connected to one ground slug in the package, which then distributes these to GND balls. |

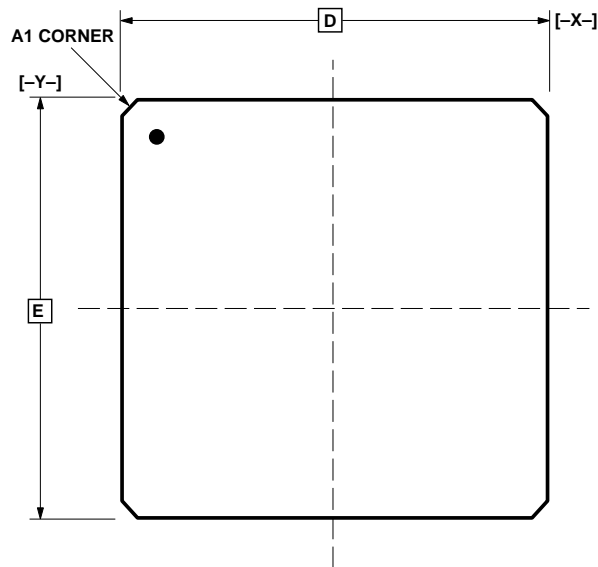
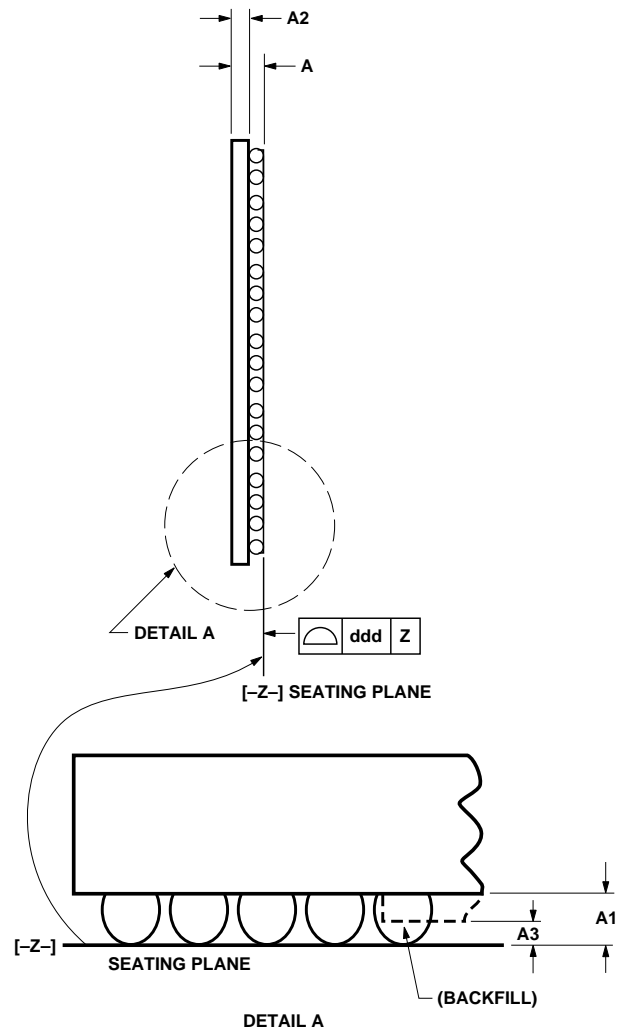
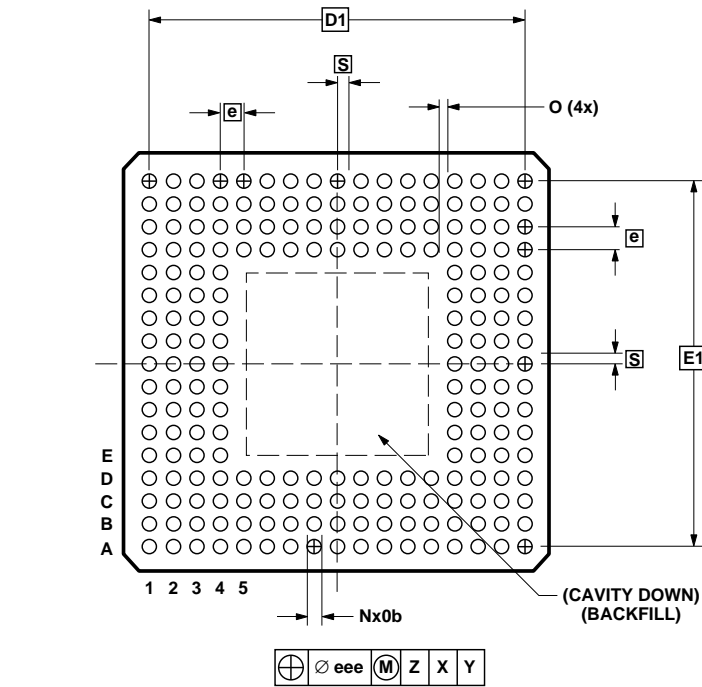
HDMP-1685A TRx I/O Definition, continued

| Name | Pin | Type | Signal |
|-------------|--|-------------|---|
| GND | A01 A03 A11 A15 A17 B04 B09 C07 C16 D04 D05 D11 E15 F04 F17 G03 K03 K04 K14 K15 L03 P04 P06 P08 P10 P12 R03 R06 R10 R12 R15 T02 T06 T08 T10 T12 T15 T16 U01 U02 U08 U09 U12 U15 U16 U17 | S | Logic Ground: Normally 0 volts. All GND pads on the chip are connected to one ground slug in the package, which then distributes these to GND balls. |

HDMP-1685A TRx I/O Definition, continued

| Name | Pin | Type | Signal |
|-------------|------------|-------------|--|
| NC | A08 | | These pins are connected to an isolated pad and have no functionality. They may be left open, or LVTTTL levels may be applied. |
| | A14 | | |
| | B01 | | |
| | B02 | | |
| | B03 | | |
| | B08 | | |
| | B13 | | |
| | B14 | | |
| | C02 | | |
| | C03 | | |
| | C08 | | |
| | C09 | | |
| | C13 | | |
| | D08 | | |
| | D09 | | |
| | D13 | | |
| | E16 | | |
| | E17 | | |
| | F01 | | |
| | F14 | | |
| | F15 | | |
| | F16 | | |
| | G01 | | |
| | G02 | | |
| | H02 | | |
| | H03 | | |
| | H04 | | |
| | H14 | | |
| | H15 | | |
| | J15 | | |
| | J16 | | |
| | J17 | | |
| | K01 | | |
| | K02 | | |
| | L01 | | |
| | L02 | | |
| | M02 | | |
| | M03 | | |
| | M04 | | |
| | M14 | | |
| | M15 | | |
| | M16 | | |
| | N16 | | |
| | N17 | | |
| | P02 | | |
| | P03 | | |
| | P14 | | |
| | P15 | | |
| | P16 | | |
| | P17 | | |
| | R02 | | |
| | T01 | | |
| | T17 | | |

Package Drawing



TOLERANCE OF FORM AND POSITION

| SYMBOL | MIN. | NOM. | MAX. |
|--------|------|------|------|
| ddd | | | 0.15 |
| eee | | | 0.30 |

DIMENSIONS IN MILLIMETERS

| SYMBOL | MIN. | NOM. | MAX. |
|--------|--------------|------|------|
| A | 1.35 | 1.50 | 1.65 |
| A1 | 0.60 | 0.65 | 0.70 |
| A2 | 0.85 | 0.90 | 0.95 |
| A3 | 0.15 | | |
| D | 23.00 ± 0.20 | | |
| D1 | 20.32 BSC | | |
| E | 23.00 ± 0.20 | | |
| E1 | 20.32 BSC | | |
| MD/ME | 17 | | |
| N | 208 | | |
| N1 | 4 | | |
| O | 0.60 | | |
| b | 0.60 | 0.75 | 0.90 |
| e | 1.27 ± 0.10 | | |

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