

# Si4542DY

## 30V Complementary PowerTrench® MOSFET

### General Description

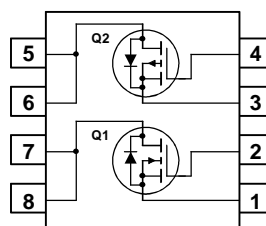
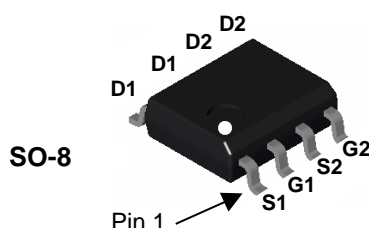
This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

### Applications

- DC/DC converter
- Power management

### Features

- **Q1: N-Channel**  
6 A, 30 V  $R_{DS(on)} = 28\text{ m}\Omega @ V_{GS} = 10\text{V}$   
 $R_{DS(on)} = 35\text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- **Q2: P-Channel**  
-6 A, -30 V  $R_{DS(on)} = 32\text{ m}\Omega @ V_{GS} = -10\text{V}$   
 $R_{DS(on)} = 45\text{ m}\Omega @ V_{GS} = -4.5\text{V}$



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DSS}$	Drain-Source Voltage	30	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	6	-6	A
	- Pulsed	20	-20	
$P_D$	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1.2		
	(Note 1c)	1		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
4542	Si4542DY	13"	12mm	2500 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Off Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	Q1 Q2	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		23 -21		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	Q1 Q2	1 -1	1.5 -1.7	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		-4 4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -6\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -6\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	Q1  Q2		19 32 25 21 29 30	28 48 35 32 51 45	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	Q1 Q2	20 -20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 6\text{ A}$ $V_{DS} = -10\text{ V}, I_D = -6\text{ A}$	Q1 Q2		18 16		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2		830 1540		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$ Q2	Q1 Q2		185 400		pF
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	Q1 Q2		80 170		pF

**Electrical Characteristics (continued)** $T_A = 25^\circ\text{C}$  unless otherwise noted

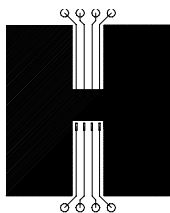
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Switching Characteristics</b> (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DS} = 15\text{ V}, I_D = 1\text{ A}$	Q1 Q2		6 13	12 24	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		10 22	18 35	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DS} = -15\text{ V}, I_D = -1\text{ A}$	Q1 Q2		18 47	29 75	ns
$t_f$	Turn-Off Fall Time	$V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		5 18	12 30	ns
$Q_g$	Total Gate Charge	Q1 $V_{DS} = 15\text{ V}, I_D = 7.5\text{ A}, V_{GS} = 5\text{ V}$	Q1 Q2		9 15	13 20	nC
$Q_{gs}$	Gate-Source Charge	Q2	Q1 Q2		2.8 4		nC
$Q_{gd}$	Gate-Drain Charge	$V_{DS} = -10\text{ V}, I_D = -6\text{ A}, V_{GS} = -5\text{ V}$	Q1 Q2		3.1 5		nC

### Drain-Source Diode Characteristics and Maximum Ratings

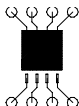
$I_S$	Maximum Continuous Drain-Source Diode Forward Current	Q1			1.3	A
		Q2			-1.3	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q1		0.7	V
		$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q2		-0.7	-1.2

#### Notes:

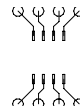
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in<sup>2</sup> pad of 2 oz copper



b) 125°C/W when mounted on a .02 in<sup>2</sup> pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

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