



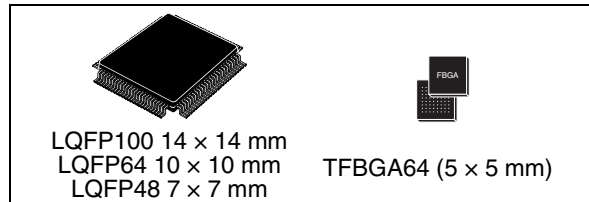
# STM32F100x4 STM32F100x6 STM32F100x8 STM32F100xB

Low & medium-density value line, advanced ARM-based 32-bit MCU with 16 to 128 KB Flash, 12 timers, ADC, DAC & 8 comm interfaces

Preliminary data

## Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 24 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance
  - Single-cycle multiplication and hardware division
- Memories
  - 16 to 128 Kbytes of Flash memory
  - 4 to 8 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR and programmable voltage detector (PVD)
  - 4-to-24 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V<sub>BAT</sub> supply for RTC and backup registers
- Debug mode
  - Serial wire debug (SWD) and JTAG interfaces
- DMA
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I<sup>2</sup>Cs, USARTs and DACs
- 1 × 12-bit, 1.2 μs A/D converter (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- 2 × 12-bit D/A converters
- Up to 80 fast I/O ports
  - 37/51/80 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant



- Up to 12 timers
  - Up to three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 16-bit, 6-channel advanced-control timer: up to 6 channels for PWM output, dead time generation and emergency stop
  - One 16-bit timer, with 2 IC/OC, 1 OCN/PWM, dead-time generation and emergency stop
  - Two 16-bit timers, each with IC/OC/OCN/PWM, dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: 24-bit downcounter
  - Two 16-bit basic timers to drive the DAC
- Up to 8 communication interfaces
  - Up to two I<sup>2</sup>C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 SPIs (12 Mbit/s)
  - Consumer electronics control (CEC) interface
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

Table 1. Device summary

Reference	Part number
STM32F100x4	STM32F100C4, STM32F100R4
STM32F100x6	STM32F100C6, STM32F100R6
STM32F100x8	STM32F100C8, STM32F100R8, STM32F100V8
STM32F100xB	STM32F100CB, STM32F100RB, STM32F100VB

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB value line microcontrollers. In the rest of the document, the STM32F100x4 and STM32F100x6 are referred to as low-density devices while the STM32F100x8 and STM32F100xB are identified as medium-density devices.

The STM32F100xx datasheet should be read in conjunction with the low- and medium-density STM32F100xx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website at the following address: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/>.



## 2 Description

The STM32F100xx value line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 24 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 8 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (up to two I<sup>2</sup>Cs, two SPIs, one HDMI CEC, and up to three USARTs), one 12-bit ADC, two 12-bit DACs, up to six general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F100xx low- and medium-density value line family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F100xx value line family includes devices in three different packages ranging from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F100xx value line microcontroller family suitable for a wide range of applications:

- Application control and user interface
- Medical and handheld equipment
- PC peripherals, gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

*Figure 1* shows the general block diagram of the device family.

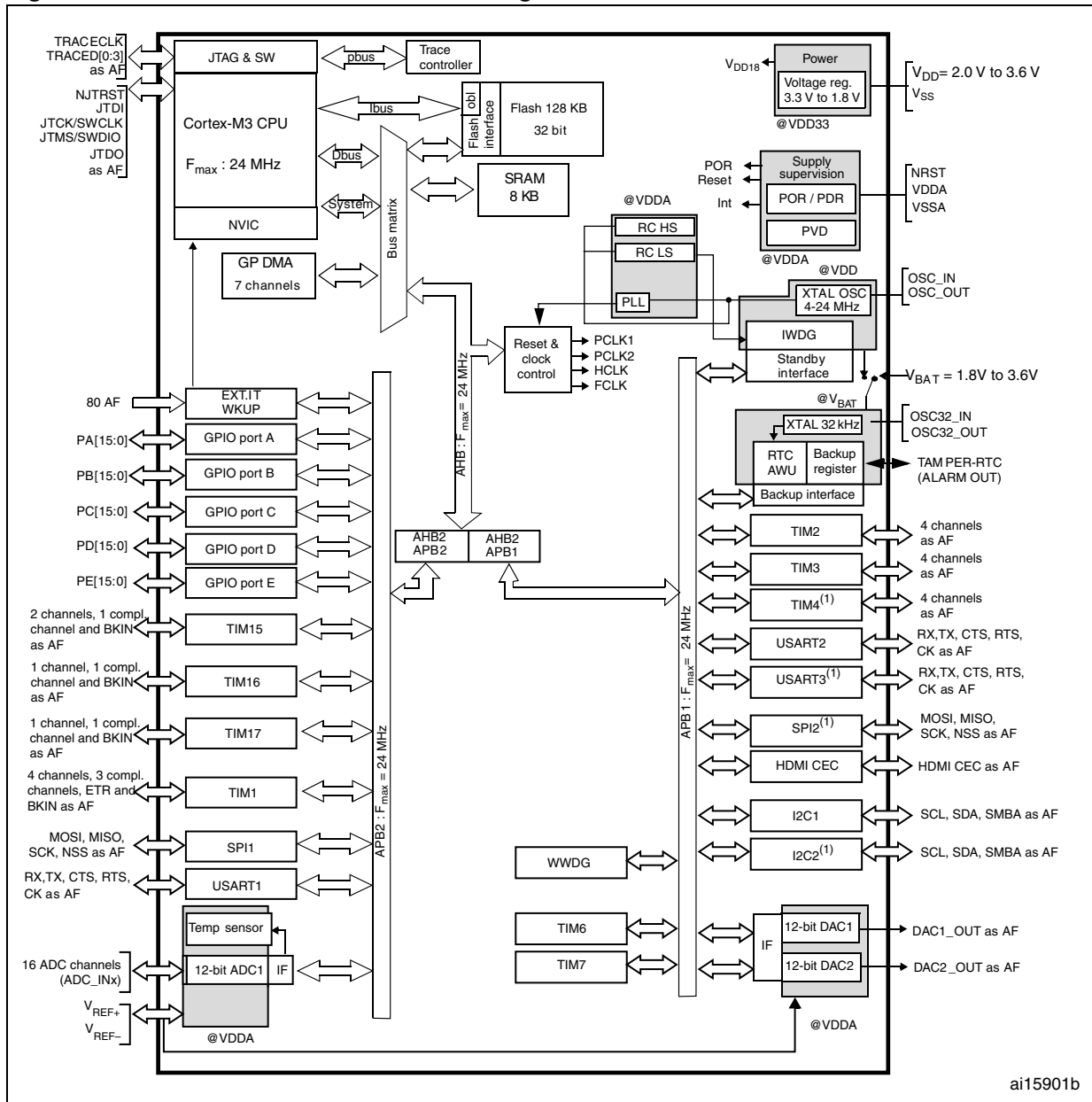
## 2.1 Device overview

Table 2. STM32F100xx features and peripheral counts

Peripheral		STM32F100Cx				STM32F100Rx				STM32F100Vx	
Flash - Kbytes		16	32	64	128	16	32	64	128	64	128
SRAM - Kbytes		4	4	8	8	4	4	8	8	8	8
Timers	Advanced-control	1		1		1		1		1	
	General-purpose	5 <sup>(1)</sup>		6		5 <sup>(1)</sup>		6		6	
Communication interfaces	SPI	1 <sup>(2)</sup>		2		1 <sup>(2)</sup>		2		2	
	I <sup>2</sup> C	1 <sup>(3)</sup>		2		1 <sup>(3)</sup>		2		2	
	USART	2 <sup>(4)</sup>		3		2 <sup>(4)</sup>		3		3	
	CEC	1									
12-bit synchronized ADC number of channels		1 10 channels				1 16 channels				1 16 channels	
GPIOs		37				51				80	
12-bit DAC Number of channels		2 2									
CPU frequency		24 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperatures		Ambient operating temperature: -40 to +85 °C / -40 to +105 °C (see <a href="#">Table 8</a> ) Junction temperature: -40 to +125 °C (see <a href="#">Table 8</a> )									
Packages		LQFP48				LQFP64, TFBGA64				LQFP100	

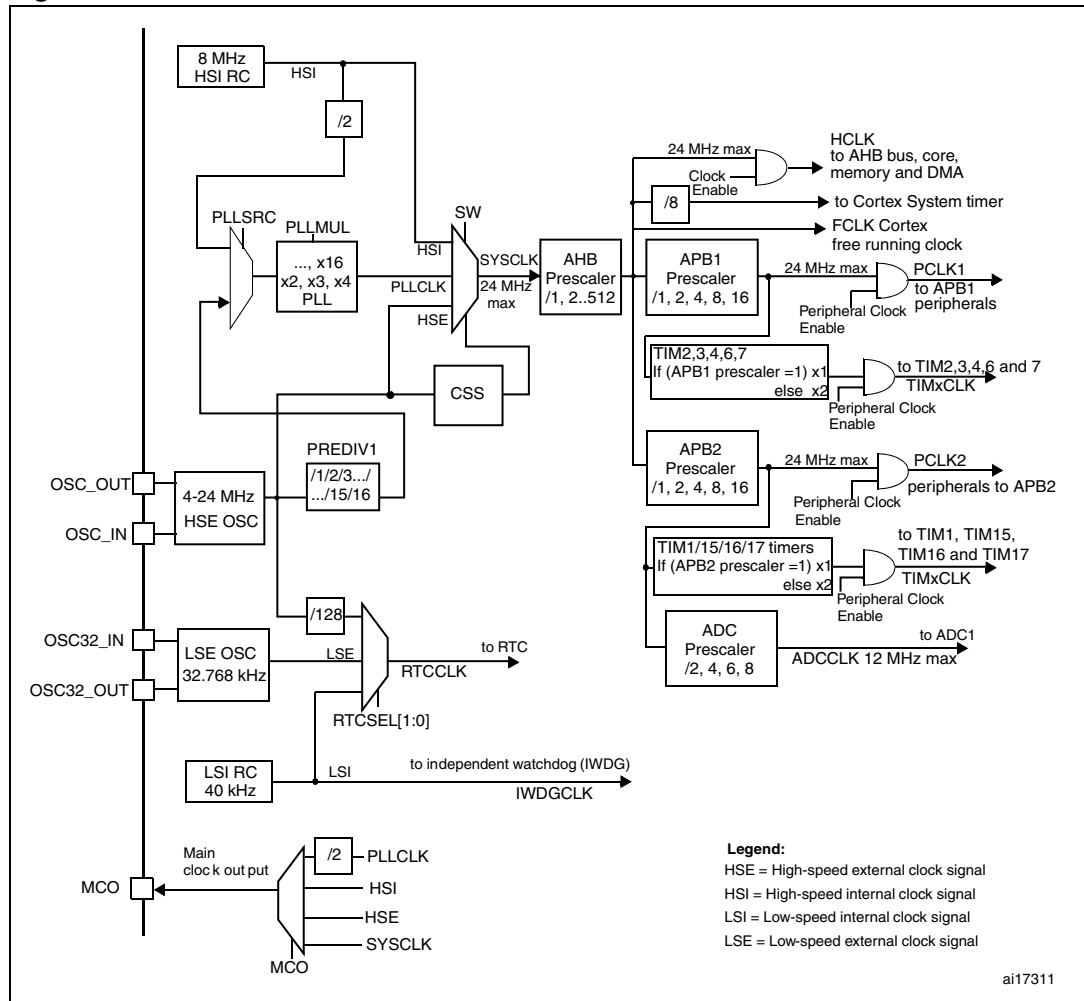
1. TIM4 not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART3 is not present.

Figure 1. STM32F100xx value line block diagram



1. Peripherals not present in low-density value line devices.
2. AF = alternate function on I/O port pin.
3.  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  (junction temperature up to  $105\text{ }^\circ\text{C}$ ) or  $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$  (junction temperature up to  $125\text{ }^\circ\text{C}$ ).

Figure 2. Clock tree



4. To have an ADC conversion time of 1.2  $\mu$ s, APB2 must be at 24 MHz.

## 2.2 Overview

### 2.2.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F100xx value line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

## 2.3 Embedded Flash memory

Up to 128 Kbytes of embedded Flash memory is available for storing programs and data.

## 2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 2.5 Embedded SRAM

Up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

## 2.6 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 41 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

## 2.7 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

## 2.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

## 2.9 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

## 2.10 Power supply schemes

- $V_{DD} = 2.0$  to  $3.6$  V: External power supply for I/Os and the internal regulator. Provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 2.0$  to  $3.6$  V: External analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to  $V_{DDA}$  is  $2.4$  V when the ADC is used).  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.
- $V_{BAT} = 1.8$  to  $3.6$  V: Power supply for RTC, external clock  $32$  kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

## 2.11 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to  $2$  V. The device remains in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

## 2.12 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

## 2.13 Low-power modes

The STM32F100xx value line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**  
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**  
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the  $1.8$  V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.



The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note:* The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

## 2.14 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I<sup>2</sup>C, USART, all timers and ADC.

## 2.15 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V<sub>DD</sub> supply when present or through the V<sub>BAT</sub> pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V<sub>DD</sub> power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

## 2.16 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, six general-purpose timers, two basic timers and two watchdog timers.

[Table 3](#) compares the features of the advanced-control, general-purpose and basic timers.

**Table 3. Timer feature comparison**

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

### 2.16.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### 2.16.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16 & TIM17)

There are six synchronizable general-purpose timers embedded in the STM32F100xx devices (see [Table 3](#) for differences). Each general-purpose timers can be used to generate PWM outputs, or as simple time base.

#### TIM2, TIM3, TIM4

STM32F100xx devices feature three synchronizable 4-channels general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-

pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

### **TIM15, TIM16 and TIM17**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

### **2.16.3 Basic timers TIM6 and TIM7**

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### **2.16.4 Independent watchdog**

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### **2.16.5 Window watchdog**

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 2.16.6 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

### 2.17 I<sup>2</sup>C bus

The I<sup>2</sup>C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

### 2.18 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

### 2.19 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

Both SPIs can be served by the DMA controller.

### 2.20 HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The STM32F100xx value line embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

## 2.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

## 2.22 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to [Table 4: STM32F100xx pin definitions](#); it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the STM32F10xxx reference manual for software considerations.

## 2.23 ADC (analog-to-digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

## 2.24 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference  $V_{REF+}$

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

## 2.25 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between  $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$ . The temperature sensor is internally connected to the ADC1\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

## 2.26 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 3 Pinouts and pin description

Figure 3. STM32F100xx value line LQFP100 pinout

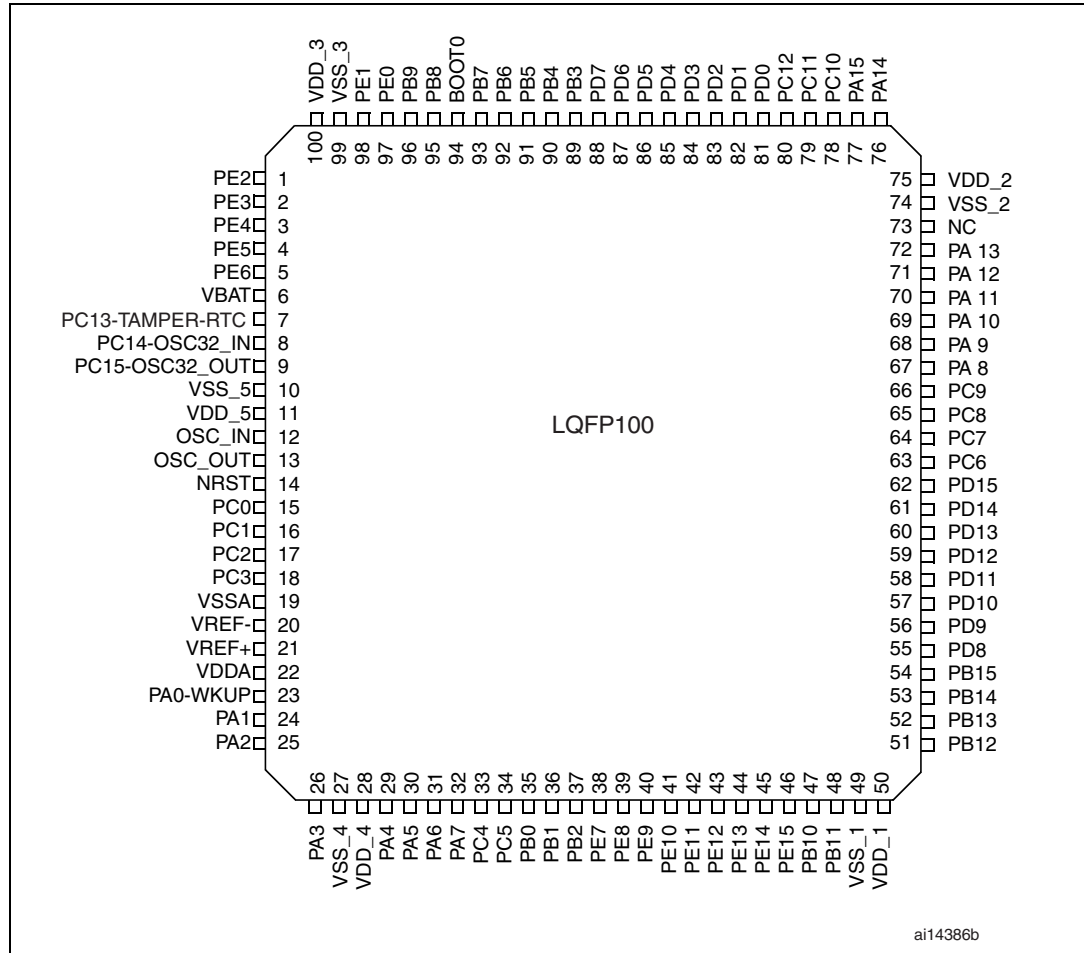


Figure 4. STM32F100xx value line LQFP64 pinout

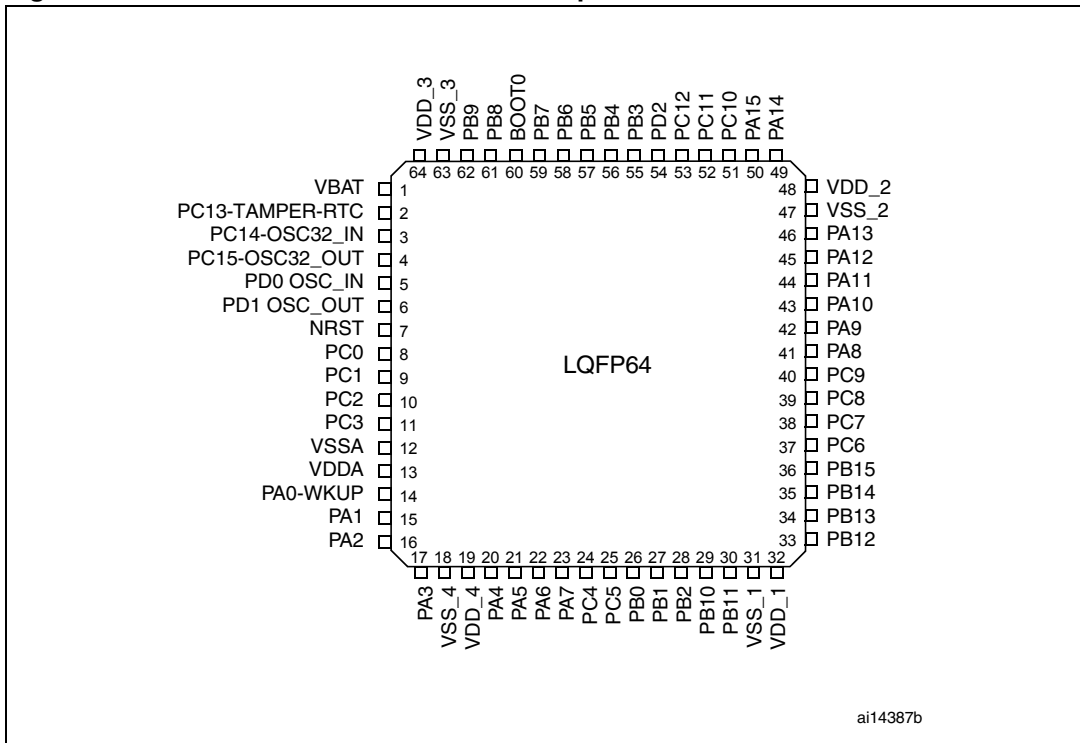


Figure 5. STM32F100xx value line LQFP48 pinout

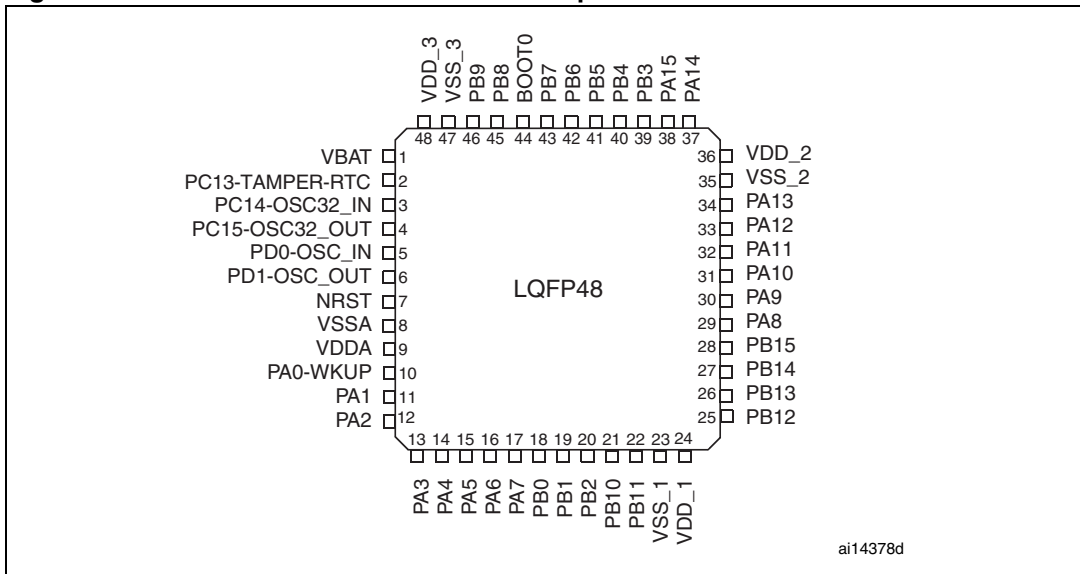
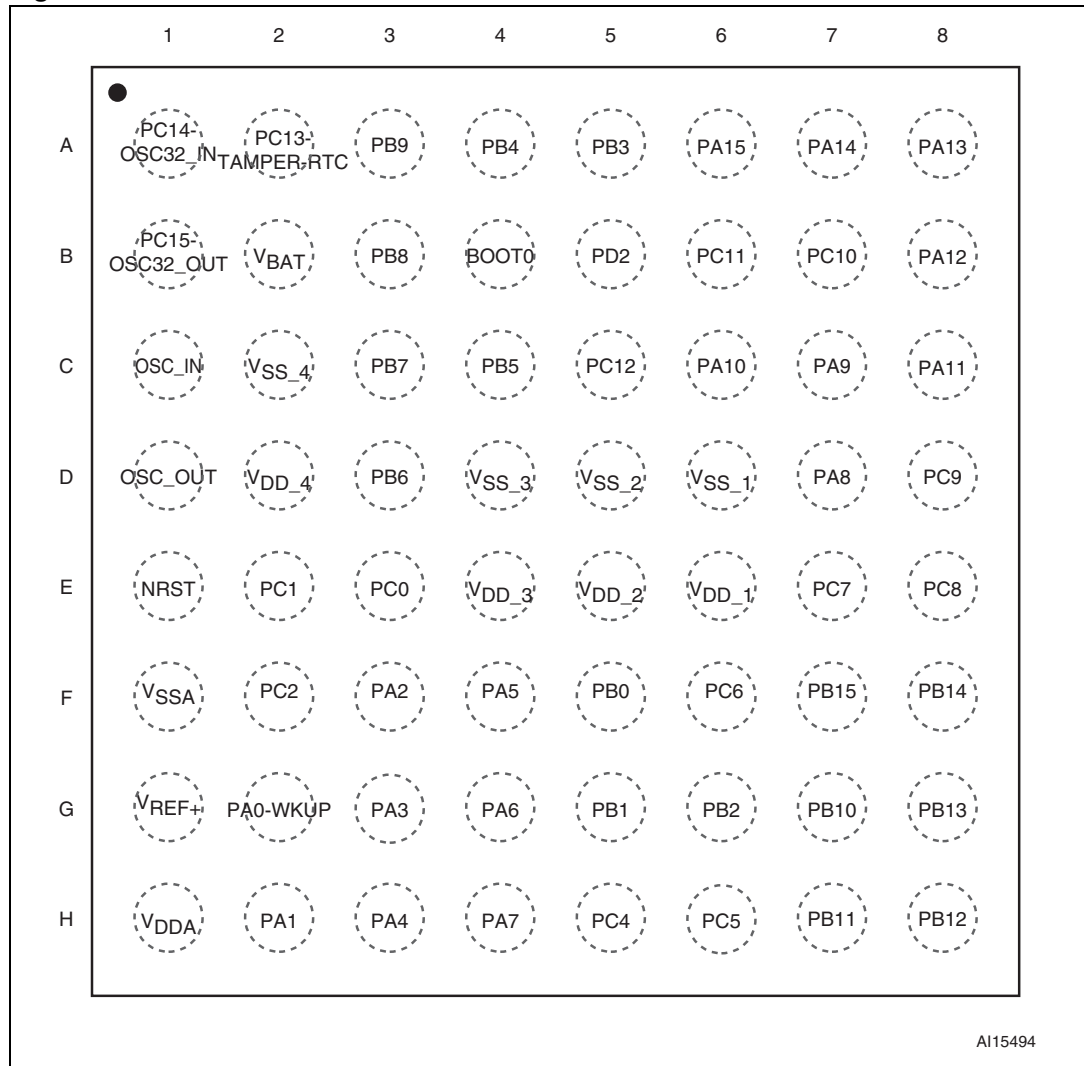




Figure 6. STM32F100xx value line TFBGA64 ballout



AI15494

Table 4. STM32F100xx pin definitions

Pins				Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)(4)</sup>	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
1	-	-	-	PE2	I/O	FT	PE2	TRACECLK	
2	-	-	-	PE3	I/O	FT	PE3	TRACED0	
3	-	-	-	PE4	I/O	FT	PE4	TRACED1	
4	-	-	-	PE5	I/O	FT	PE5	TRACED2	
5	-	-	-	PE6	I/O	FT	PE6	TRACED3	
6	1	B2	1	V <sub>BAT</sub>	S		V <sub>BAT</sub>		
7	2	A2	2	PC13-TAMPER-RTC <sup>(5)</sup>	I/O		PC13 <sup>(6)</sup>	TAMPER-RTC	

Table 4. STM32F100xx pin definitions (continued)

Pins				Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)(4)</sup>	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
8	3	A1	3	PC14- OSC32_IN <sup>(5)</sup>	I/O		PC14 <sup>(6)</sup>	OSC32_IN	
9	4	B1	4	PC15- OSC32_OUT <sup>(5)</sup>	I/O		PC15 <sup>(6)</sup>	OSC32_OUT	
10	-	-	-	V <sub>SS_5</sub>	S		V <sub>SS_5</sub>		
11	-	-	-	V <sub>DD_5</sub>	S		V <sub>DD_5</sub>		
12	5	C1	5	OSC_IN	I		OSC_IN		
13	6	D1	6	OSC_OUT	O		OSC_OUT		
14	7	E1	7	NRST	I/O		NRST		
15	8	E3	-	PC0	I/O		PC0	ADC1_IN10	
16	9	E2	-	PC1	I/O		PC1	ADC1_IN11	
17	10	F2	-	PC2	I/O		PC2	ADC1_IN12	
18	11	- <sup>(7)</sup>	-	PC3	I/O		PC3	ADC1_IN13	
19	12	F1	8	V <sub>SSA</sub>	S		V <sub>SSA</sub>		
20	-	-	-	V <sub>REF-</sub>	S		V <sub>REF-</sub>		
21	-	G1	-	V <sub>REF+</sub>	S		V <sub>REF+</sub>		
22	13	H1	9	V <sub>DDA</sub>	S		V <sub>DDA</sub>		
23	14	G2	10	PA0-WKUP	I/O		PA0	WKUP / USART2_CTS <sup>(12)</sup> / ADC1_IN0 / TIM2_CH1_ETR <sup>(12)</sup>	
24	15	H2	11	PA1	I/O		PA1	USART2_RTS <sup>(12)</sup> / ADC1_IN1 / TIM2_CH2 <sup>(12)</sup>	
25	16	F3	12	PA2	I/O		PA2	USART2_TX <sup>(12)</sup> / ADC1_IN2 / TIM2_CH3 <sup>(12)</sup> / TIM15_CH1 <sup>(12)</sup>	
26	17	G3	13	PA3	I/O		PA3	USART2_RX <sup>(12)</sup> / ADC1_IN3 / TIM2_CH4 <sup>(12)</sup> / TIM15_CH2 <sup>(12)</sup>	
27	18	C2	-	V <sub>SS_4</sub>	S		V <sub>SS_4</sub>		
28	19	D2	-	V <sub>DD_4</sub>	S		V <sub>DD_4</sub>		
29	20	H3	14	PA4	I/O		PA4	SPI1_NSS <sup>(12)</sup> / ADC1_IN4 USART2_CK <sup>(12)</sup> / DAC1_OUT	
30	21	F4	15	PA5	I/O		PA5	SPI1_SCK <sup>(12)</sup> / ADC1_IN5 / DAC2_OUT	
31	22	G4	16	PA6	I/O		PA6	SPI1_MISO <sup>(12)</sup> / ADC1_IN6 / TIM3_CH1 <sup>(12)</sup>	TIM1_BKIN / TIM16_CH1
32	23	H4	17	PA7	I/O		PA7	SPI1_MOSI <sup>(12)</sup> / ADC1_IN7 / TIM3_CH2 <sup>(12)</sup>	TIM1_CH1N / TIM17_CH1
33	24	H5	-	PC4	I/O		PC4	ADC1_IN14	

Table 4. STM32F100xx pin definitions (continued)

Pins				Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)(4)</sup>	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
34	25	H6	-	PC5	I/O		PC5	ADC1_IN15	
35	26	F5	18	PB0	I/O		PB0	ADC1_IN8/TIM3_CH3 <sup>(12)</sup>	TIM1_CH2N
36	27	G5	19	PB1	I/O		PB1	ADC1_IN9/TIM3_CH4 <sup>(12)</sup>	TIM1_CH3N
37	28	G6	20	PB2	I/O	FT	PB2/BOOT1		
38	-	-	-	PE7	I/O	FT	PE7		TIM1_ETR
39	-	-	-	PE8	I/O	FT	PE8		TIM1_CH1N
40	-	-	-	PE9	I/O	FT	PE9		TIM1_CH1
41	-	-	-	PE10	I/O	FT	PE10		TIM1_CH2N
42	-	-	-	PE11	I/O	FT	PE11		TIM1_CH2
43	-	-	-	PE12	I/O	FT	PE12		TIM1_CH3N
44	-	-	-	PE13	I/O	FT	PE13		TIM1_CH3
45	-	-	-	PE14	I/O	FT	PE14		TIM1_CH4
46	-	-	-	PE15	I/O	FT	PE15		TIM1_BKIN
47	29	G7	21	PB10	I/O	FT	PB10	I2C2_SCL <sup>(8)</sup> /USART3_TX <sup>(12)</sup>	TIM2_CH3 / CEC
48	30	H7	22	PB11	I/O	FT	PB11	I2C2_SDA <sup>(8)</sup> /USART3_RX <sup>(12)</sup>	TIM2_CH4
49	31	D6	23	V <sub>SS_1</sub>	S		V <sub>SS_1</sub>		
50	32	E6	24	V <sub>DD_1</sub>	S		V <sub>DD_1</sub>		
51	33	H8	25	PB12	I/O	FT	PB12	SPI2_NSS <sup>(9)</sup> / I2C2_SMBA <sup>(8)</sup> / TIM1_BKIN <sup>(12)</sup> /USART3_CK <sup>(12)</sup>	
52	34	G8	26	PB13	I/O	FT	PB13	SPI2_SCK <sup>(9)</sup> /TIM1_CH1N <sup>(12)</sup> USART3_CTS <sup>(12)</sup>	
53	35	F8	27	PB14	I/O	FT	PB14	SPI2_MISO <sup>(9)</sup> /TIM1_CH2N <sup>(12)</sup> / USART3_RTS <sup>(12)</sup>	TIM15_CH1
54	36	F7	28	PB15	I/O	FT	PB15	SPI2_MOSI <sup>(9)</sup> / TIM1_CH3N / TIM15_CH1N <sup>(12)</sup>	TIM15_CH2
55	-	-	-	PD8	I/O	FT	PD8		USART3_TX
56	-	-	-	PD9	I/O	FT	PD9		USART3_RX
57	-	-	-	PD10	I/O	FT	PD10		USART3_CK
58	-	-	-	PD11	I/O	FT	PD11		USART3_CTS
59	-	-	-	PD12	I/O	FT	PD12		TIM4_CH1 <sup>(10)</sup> / USART3_RTS
60	-	-	-	PD13	I/O	FT	PD13		TIM4_CH2 <sup>(10)</sup>
61	-	-	-	PD14	I/O	FT	PD14		TIM4_CH3 <sup>(10)</sup>

Table 4. STM32F100xx pin definitions (continued)

Pins				Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)(4)</sup>		
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap	
62	-	-	-	PD15	I/O	FT	PD15		TIM4_CH4 <sup>(10)</sup>	
63	37	F6	-	PC6	I/O	FT	PC6		TIM3_CH1	
64	38	E7		PC7	I/O	FT	PC7		TIM3_CH2	
65	39	E8		PC8	I/O	FT	PC8		TIM3_CH3	
66	40	D8	-	PC9	I/O	FT	PC9		TIM3_CH4	
67	41	D7	29	PA8	I/O	FT	PA8	USART1_CK / MCO / TIM1_CH1		
68	42	C7	30	PA9	I/O	FT	PA9	USART1_TX <sup>(12)</sup> / TIM1_CH2	TIM15_BKIN	
69	43	C6	31	PA10	I/O	FT	PA10	USART1_RX <sup>(12)</sup> / TIM1_CH3	TIM17_BKIN	
70	44	C8	32	PA11	I/O	FT	PA11	USART1_CTS / TIM1_CH4		
71	45	B8	33	PA12	I/O	FT	PA12	USART1_RTS / TIM1_ETR		
72	46	A8	34	PA13	I/O	FT	JTMS- SWDIO		PA13	
73	-	-	-	Not connected						
74	47	D5	35	V <sub>SS_2</sub>	S		V <sub>SS_2</sub>			
75	48	E5	36	V <sub>DD_2</sub>	S		V <sub>DD_2</sub>			
76	49	A7	37	PA14	I/O	FT	JTCK/SWCLK		PA14	
77	50	A6	38	PA15	I/O	FT	JTDI		TIM2_CH1_ETR / PA15/ SPI1_NSS	
78	51	B7	-	PC10	I/O	FT	PC10		USART3_TX	
79	52	B6	-	PC11	I/O	FT	PC11		USART3_RX	
80	53	C5	-	PC12	I/O	FT	PC12		USART3_CK	
81	5	C1	5	PD0	I/O	FT	OSC_IN <sup>(11)</sup>			
82	6	D1	6	PD1	I/O	FT	OSC_OUT <sup>(11)</sup>			
83	54	B5		PD2	I/O	FT	PD2	TIM3_ETR		
84	-	-	-	PD3	I/O	FT	PD3		USART2_CTS	
85	-	-	-	PD4	I/O	FT	PD4		USART2_RTS	
86	-	-	-	PD5	I/O	FT	PD5		USART2_TX	
87	-	-	-	PD6	I/O	FT	PD6		USART2_RX	
88	-	-	-	PD7	I/O	FT	PD7		USART2_CK	
89	55	A5	39	PB3	I/O	FT	JTDO		TIM2_CH2 / PB3 TRACESWO SPI1_SCK	

Table 4. STM32F100xx pin definitions (continued)

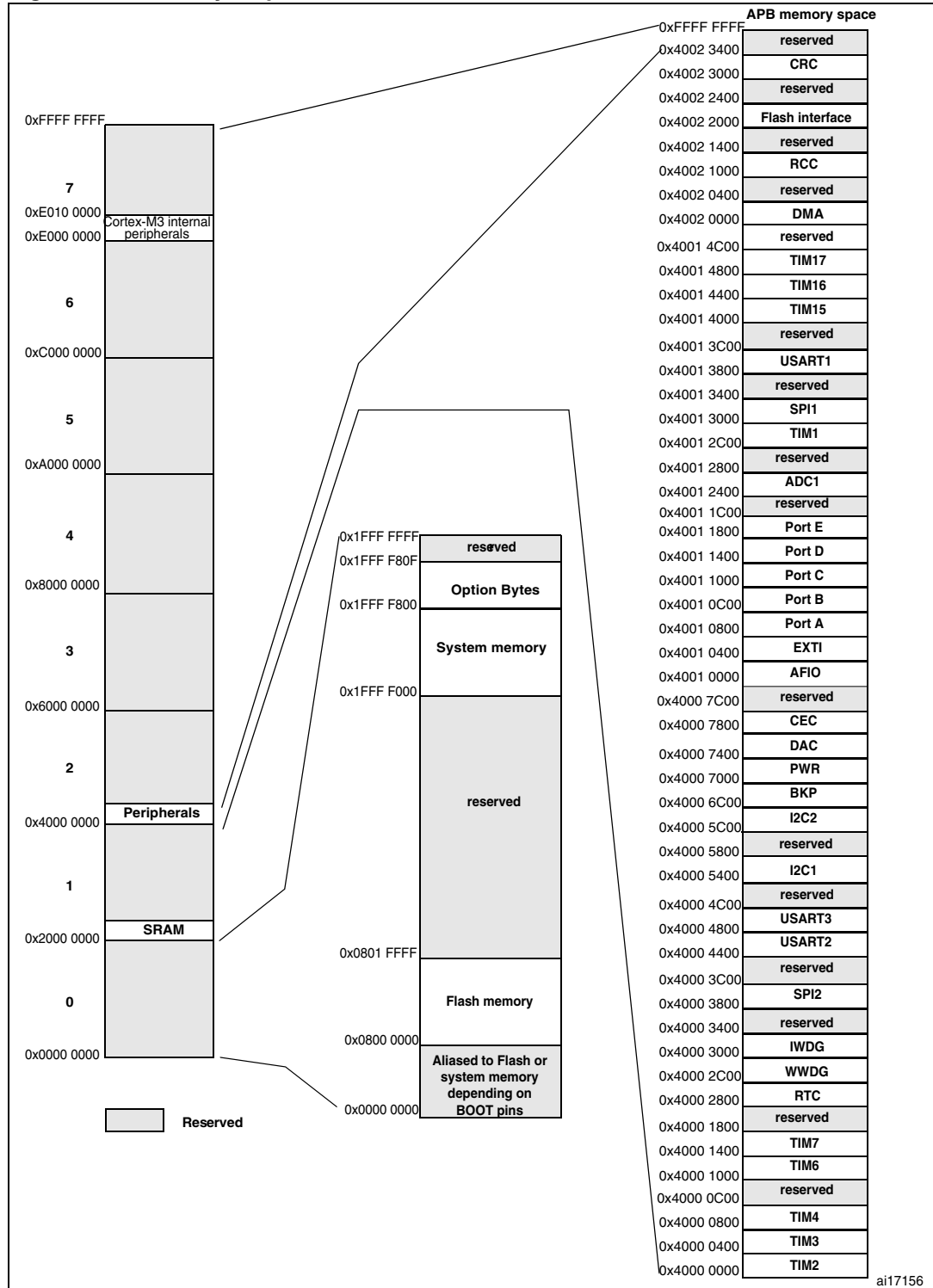
Pins				Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)(4)</sup>	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
90	56	A4	40	PB4	I/O	FT	NJTRST		PB4 / TIM3_CH1 SPI1_MISO
91	57	C4	41	PB5	I/O		PB5	I2C1_SMBA / TIM16_BKIN	TIM3_CH2 / SPI1_MOSI
92	58	D3	42	PB6	I/O	FT	PB6	I2C1_SCL <sup>(12)</sup> / TIM4_CH1 <sup>(10)(12)</sup> TIM16_CH1N	USART1_TX
93	59	C3	43	PB7	I/O	FT	PB7	I2C1_SDA <sup>(12)</sup> / TIM17_CH1N TIM4_CH2 <sup>(10)(12)</sup>	USART1_RX
94	60	B4	44	BOOT0	I		BOOT0		
95	61	B3	45	PB8	I/O	FT	PB8	TIM4_CH3 <sup>(10)(12)</sup> / TIM16_CH1 <sup>(12)</sup> / CEC <sup>(12)</sup>	I2C1_SCL
96	62	A3	46	PB9	I/O	FT	PB9	TIM4_CH4 <sup>(10)(12)</sup> / TIM17_CH1 <sup>(12)</sup>	I2C1_SDA
97	-	-	-	PE0	I/O	FT	PE0	TIM4_ETR <sup>(10)</sup>	
98	-	-	-	PE1	I/O	FT	PE1		
99	63	D4	47	V <sub>SS_3</sub>	S		V <sub>SS_3</sub>		
100	64	E4	48	V <sub>DD_3</sub>	S		V <sub>DD_3</sub>		

1. I = input, O = output, S = supply, HiZ= high impedance.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to [Table 2 on page 11](#).
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is restricted: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must *not* be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).
7. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V<sub>REF+</sub> functionality is provided instead.
8. I2C2 is not present on low-density value line devices.
9. SPI2 is not present on low-density value line devices.
10. TIM4 is not present on low-density value line devices.
11. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages and C1 and C2 in the TFBGA64 package are configured as OSC\_IN/OSC\_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
12. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).

# 4 Memory mapping

The memory map is shown in *Figure 7*.

**Figure 7. Memory map**



## 5 Electrical characteristics

### 5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ °C}$  and  $T_A = T_{A\text{max}}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\Sigma$ ).

#### 5.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ °C}$ ,  $V_{DD} = 3.3\text{ V}$  (for the  $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean} \pm 2\Sigma$ ).

#### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 8](#).

#### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 9](#).

Figure 8. Pin loading conditions

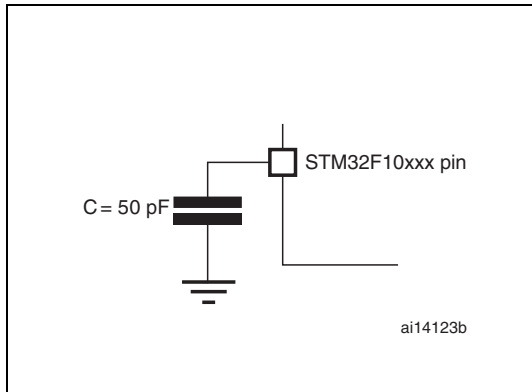
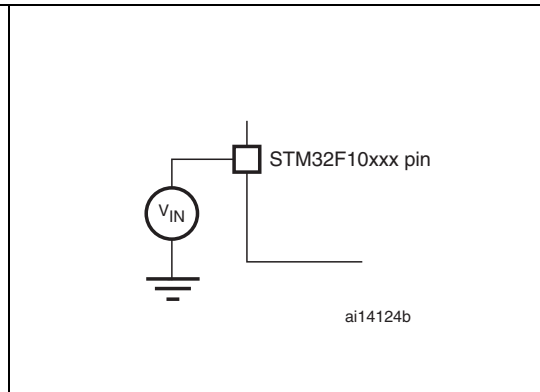
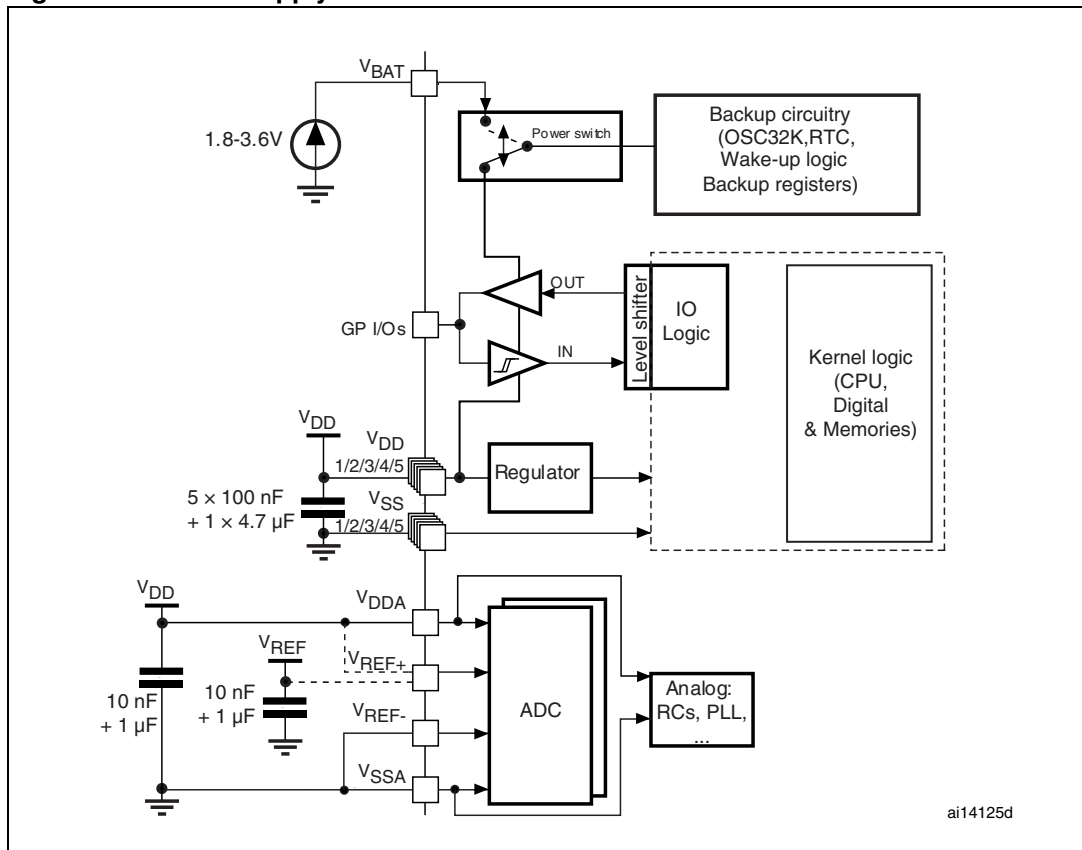


Figure 9. Pin input voltage



### 5.1.6 Power supply scheme

Figure 10. Power supply scheme

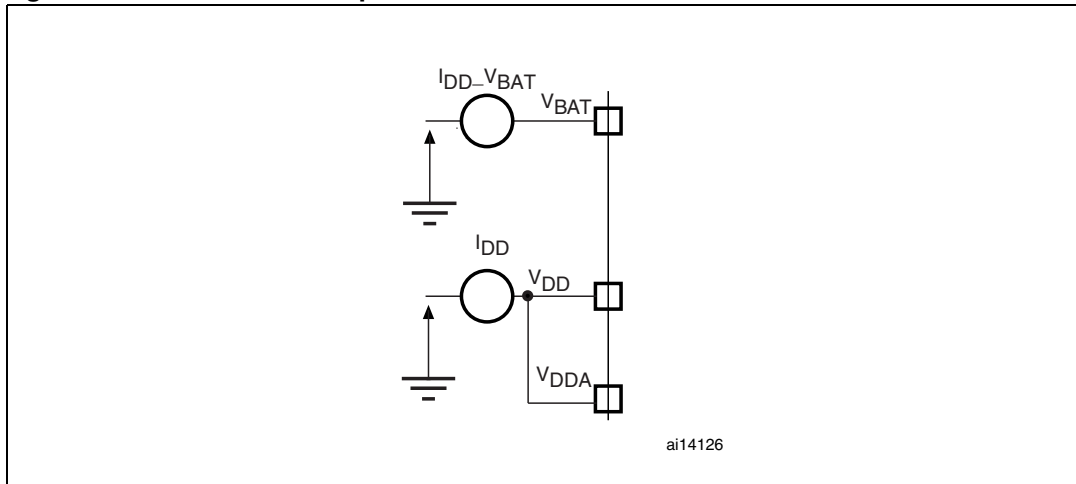


**Caution:** In [Figure 10](#), the 4.7 μF capacitor must be connected to V<sub>DD3</sub>.



### 5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 5: Voltage characteristics](#), [Table 6: Current characteristics](#), and [Table 7: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including $V_{DDA}$ and $V_{DD}$ ) <sup>(1)</sup>	-0.3	4.0	V
$V_{IN}$	Input voltage on five volt tolerant pin <sup>(2)</sup>	$V_{SS} - 0.3$	+5.5	
	Input voltage on any other pin <sup>(2)</sup>	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins		50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 5.3.11: Absolute maximum ratings (electrical sensitivity)</a>		

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2.  $I_{INJ(PIN)}$  must never be exceeded (see [Table 6: Current characteristics](#)). This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{INmax}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .

**Table 6. Current characteristics**

Symbol	Ratings	Max.	Unit
$I_{VDD}$	Total current into $V_{DD}/V_{DDA}$ power lines (source) <sup>(1)</sup>	150	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>	150	
$I_{IO}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ <sup>(2)(3)</sup>	Injected current on NRST pin	± 5	
	Injected current on High-speed external OSC_IN and Low-speed external OSC_IN pins	± 5	
	Injected current on the PA5 and PA6 pins <sup>(4)</sup>	+5 / -0	
	Injected current on any other pin <sup>(4)</sup>	± 5	
$\Sigma I_{INJ(PIN)}$ <sup>(2)</sup>	Total injected current (sum of all I/O and control pins) <sup>(4)</sup>	± 25	

- All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
- $I_{INJ(PIN)}$  must never be exceeded. This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .
- Negative injection disturbs the analog performance of the device. See note in [Section 5.3.16: 12-bit ADC characteristics](#).
- When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with  $\Sigma I_{INJ(PIN)}$  maximum current injection on four I/O port pins of the device.

**Table 7. Thermal characteristics**

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature	150	°C

## 5.3 Operating conditions

### 5.3.1 General operating conditions

**Table 8. General operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{HCLK}$	Internal AHB clock frequency		0	24	MHz
$f_{PCLK1}$	Internal APB1 clock frequency		0	24	
$f_{PCLK2}$	Internal APB2 clock frequency		0	24	
$V_{DD}$	Standard operating voltage		2	3.6	V
$V_{DDA}$ <sup>(1)</sup>	Analog operating voltage (ADC not used)	Must be the same potential as $V_{DD}$	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	

**Table 8. General operating conditions (continued)**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{BAT}$	Backup operating voltage		1.8	3.6	V
$P_D$	Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 <sup>(2)</sup>	LQFP100		434	mW
		LQFP64		444	
		TFBGA64		308	
		LQFP48		363	
$T_A$	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation <sup>(3)</sup>	-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation <sup>(3)</sup>	-40	125	
$T_J$	Junction temperature range	6 suffix version	-40	105	°C
		7 suffix version	-40	125	

1. When the ADC is used, refer to [Table 41: ADC characteristics](#).
2. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Table 6.2: Thermal characteristics on page 79](#)).
3. In low power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Table 6.2: Thermal characteristics on page 79](#)).

### 5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for  $T_A$ .

**Table 9. Operating conditions at power-up / power-down**

Symbol	Parameter	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate	0	$\infty$	$\mu\text{s/V}$
	$V_{DD}$ fall time rate	20	$\infty$	

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 10](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}^{(2)}$	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 <sup>(1)</sup>	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}^{(2)}$	PDR hysteresis			40		mV
$t_{RSTTEMPO}^{(2)}$	Reset temporization		1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.

2. Guaranteed by design, not tested in production.

### 5.3.4 Embedded reference voltage

The parameters given in [Table 11](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 11. Embedded internal reference voltage**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT}$	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.16	1.20	1.26	V
		$-40\text{ }^{\circ}\text{C} < T_A < +85\text{ }^{\circ}\text{C}$	1.16	1.20	1.24	V
$T_{S\_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage			5.1	17.1 <sup>(2)</sup>	$\mu\text{s}$
$V_{RERINT}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V} \pm 10\text{ mV}$			10	mV
$T_{Ccoeff}^{(2)}$	Temperature coefficient				100	ppm/ $^{\circ}\text{C}$

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

### 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 11: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- All peripherals are disabled except if it is explicitly mentioned
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled  $f_{PCLK1} = f_{HCLK}$ ,  $f_{PCLK2} = f_{HCLK}$

The parameters given in [Table 12](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 12. Maximum current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Max <sup>(1)</sup>		Unit
				T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD</sub>	Supply current in Run mode	External clock <sup>(2)</sup> , all peripherals enabled	24 MHz	15.4	15.7	mA
			16 MHz	11	11.5	
			8 MHz	6.7	6.9	
		External clock <sup>(2)</sup> , all peripherals disabled	24 MHz	10.3	10.5	
			16 MHz	7.8	8.1	
			8 MHz	5.1	5.3	

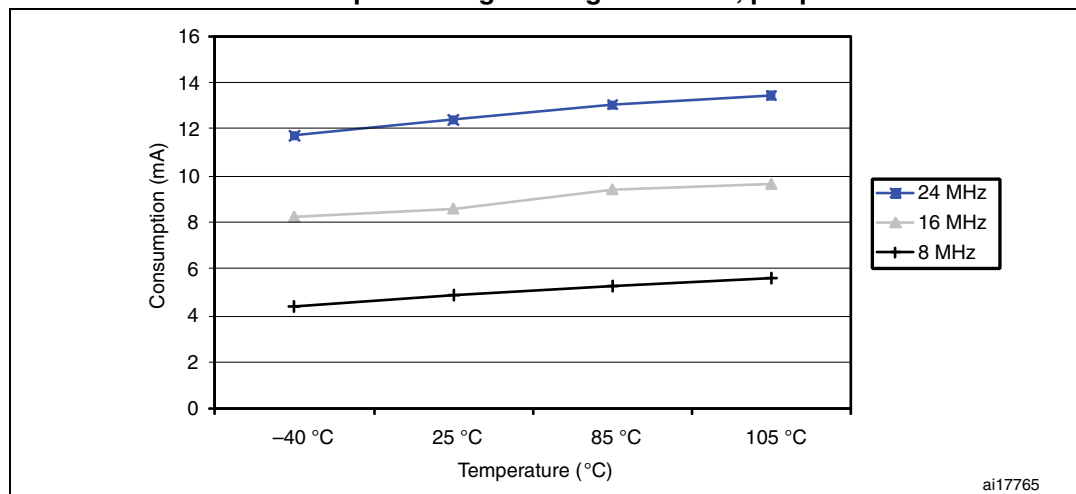
1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f<sub>HCLK</sub> > 8 MHz.

**Table 13. Maximum current consumption in Run mode, code with data processing running from RAM**

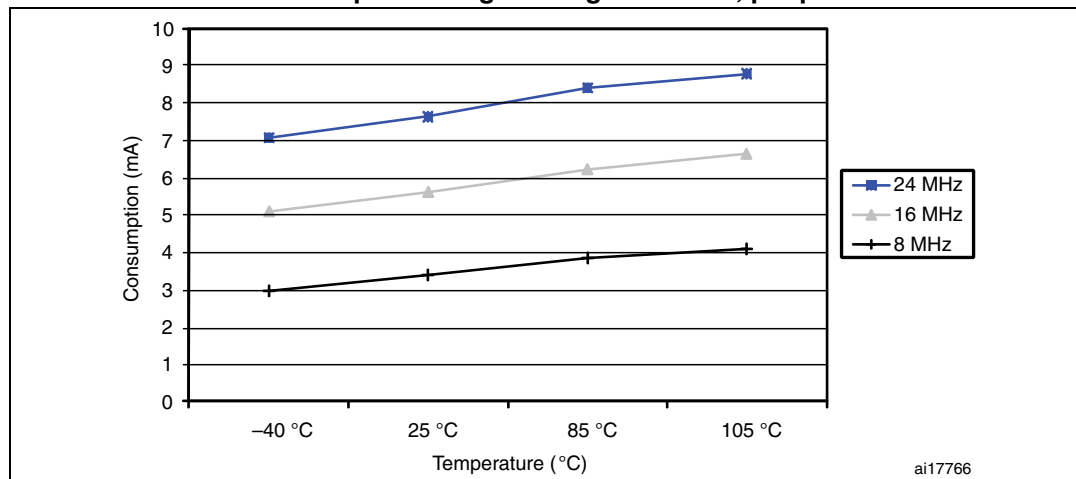
Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Max <sup>(1)</sup>		Unit
				T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD</sub>	Supply current in Run mode	External clock <sup>(2)</sup> , all peripherals enabled	24 MHz	14.5	15	mA
			16 MHz	10	10.5	
			8 MHz	6	6.3	
		External clock <sup>(2)</sup> all peripherals disabled	24MHz	9.3	9.7	
			16 MHz	6.8	7.2	
			8 MHz	4.4	4.7	

1. Based on characterization, tested in production at V<sub>DD</sub> max, f<sub>HCLK</sub> max.
2. External clock is 8 MHz and PLL is on when f<sub>HCLK</sub> > 8 MHz.

**Figure 12. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled**



**Figure 13. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled**



**Table 14. STM32F100xxB maximum current consumption in Sleep mode, code running from Flash or RAM**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Max <sup>(1)</sup>		Unit
				T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD</sub>	Supply current in Sleep mode	External clock <sup>(2)</sup> all peripherals enabled	24 MHz	9.6	10	mA
			16 MHz	7.1	7.5	
			8 MHz	4.5	4.8	
		External clock <sup>(2)</sup> all peripherals disabled	24 MHz	3.8	4	
			16 MHz	3.3	3.5	
			8 MHz	2.7	3	

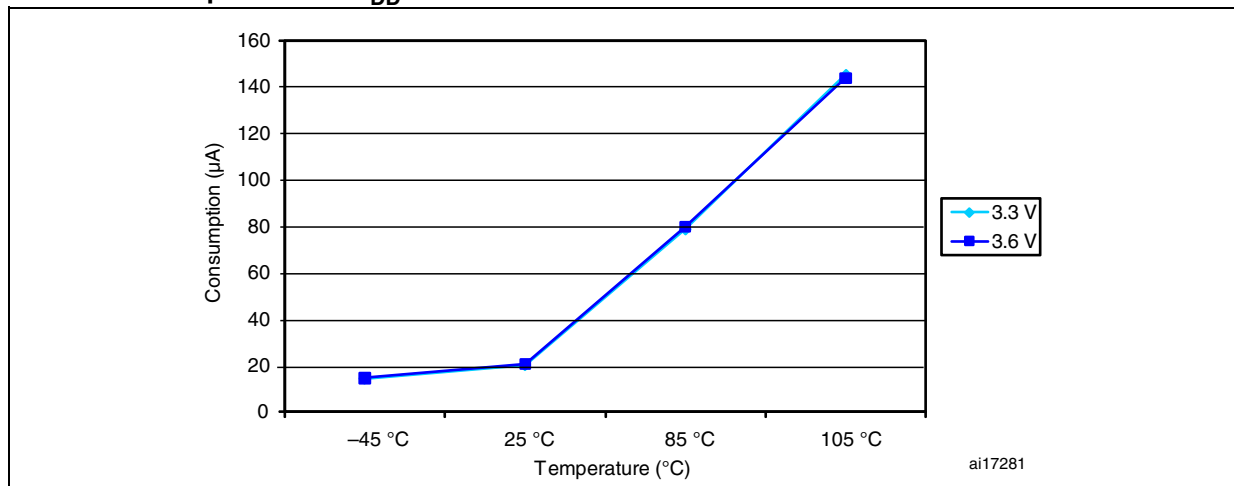
1. Based on characterization, tested in production at V<sub>DD</sub> max and f<sub>HCLK</sub> max with peripherals enabled.  
 2. External clock is 8 MHz and PLL is on when f<sub>HCLK</sub> > 8 MHz.

**Table 15. Typical and maximum current consumptions in Stop and Standby modes<sup>(1)</sup>**

Symbol	Parameter	Conditions	Typ <sup>(2)</sup>			Max		Unit
			V <sub>DD</sub> /V <sub>BAT</sub> = 2.0 V	V <sub>DD</sub> /V <sub>BAT</sub> = 2.4 V	V <sub>DD</sub> /V <sub>BAT</sub> = 3.3 V	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD</sub>	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)		23.5	24	190	350	μA
		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)		13.5	14	170	330	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON		2.6	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF		2.4	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF		1.7	2	4	5	
I <sub>DD_VBAT</sub>	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	2.0	2.3	

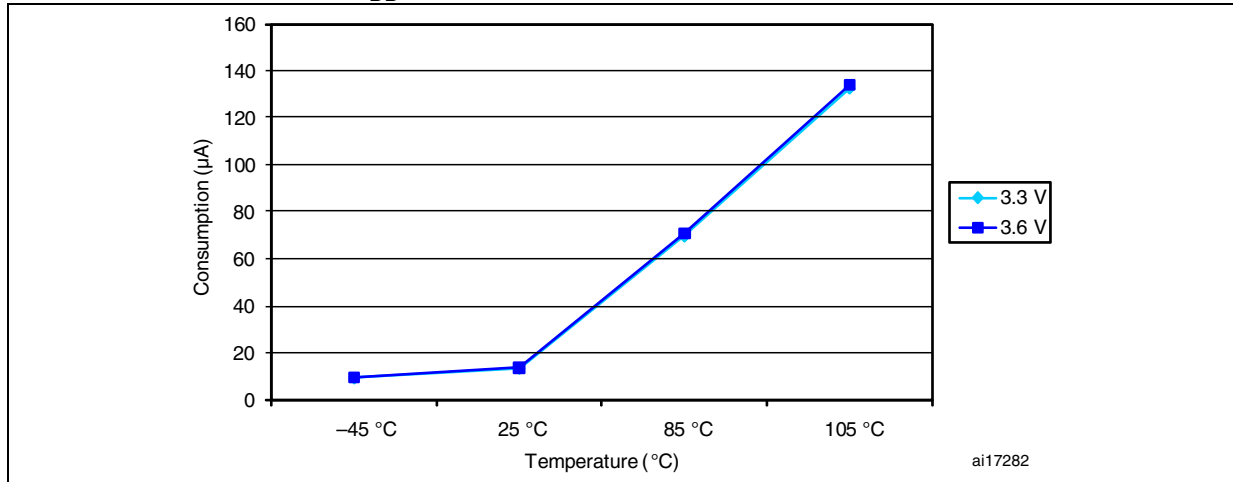
1. TBD stands for to be determined.
2. Typical values are measured at T<sub>A</sub> = 25 °C.

**Figure 14. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V<sub>DD</sub> = 3.3 V and 3.6 V**

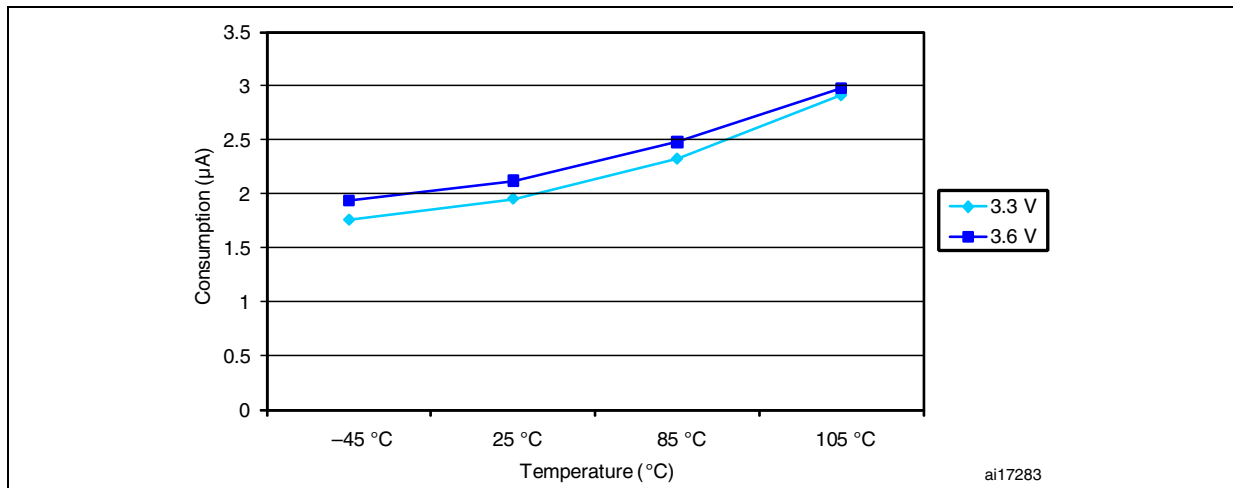




**Figure 15. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at  $V_{DD} = 3.3\text{ V}$  and  $3.6\text{ V}$**



**Figure 16. Typical current consumption in Standby mode versus temperature at  $V_{DD} = 3.3\text{ V}$  and  $3.6\text{ V}$**



### Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- All peripherals are disabled except if it is explicitly mentioned
- When the peripherals are enabled  $f_{PCLK1} = f_{HCLK}$ ,  $f_{PCLK2} = f_{HCLK}$ ,  $f_{ADCCLK} = f_{PCLK2}/2$

The parameters given in [Table 16](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 16. Typical current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typical values <sup>(1)</sup>		Unit
				All peripherals enabled <sup>(2)</sup>	All peripherals disabled	
I <sub>DD</sub>	Supply current in Run mode	Running on high-speed external clock with an 8 MHz crystal <sup>(3)</sup>	24 MHz	15.4	9	mA
			16 MHz	11.2	6.50	
			8 MHz	6.2	3.9	
			4 MHz	3.75	2.5	
			2 MHz	2.3	1.8	
			1 MHz	1.65	1.35	
			500 kHz	1.3	1.2	
		125 kHz	1.1	1		
		Running on high-speed internal RC (HSI)	24 MHz	15	8.4	
			16 MHz	10.3	6.1	
			8 MHz	5.5	3.4	
			4 MHz	3.1	1.9	
			2 MHz	1.7	1.15	
			1 MHz	1	0.8	
500 kHz	0.75		0.6			
125 kHz	0.5	0.43				

1. Typical values are measures at T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC\_CR2 register).
3. AHB prescaler used to reduce the frequency (when f<sub>HCLK</sub> > 8 MHz).

**Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typical values <sup>(1)</sup>		Unit
				All peripherals enabled <sup>(2)</sup>	All peripherals disabled	
I <sub>DD</sub>	Supply current in Sleep mode	Running on high-speed external clock with an 8 MHz crystal <sup>(3)</sup>	24 MHz	9.8	2.6	mA
			16 MHz	7	2	
			8 MHz	3.8	1.3	
			4 MHz	2.5	1.2	
			2 MHz	1.7	1.1	
			1 MHz	1.35	1	
			500 kHz	1.1	1	
			125 kHz	1	0.95	
		Running on high-speed internal RC (HSI)	24 MHz	9.6	2	
			16 MHz	6.8	1.4	
			8 MHz	3.2	0.7	
			4 MHz	1.9	0.55	
			2 MHz	1.1	0.46	
			1 MHz	0.75	0.41	
			500 kHz	0.56	0.39	
			125 kHz	0.43	0.37	

1. Typical values are measures at T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC\_CR2 register).
3. AHB prescaler used to reduce the frequency (when f<sub>HCLK</sub> > 8 MHz).

**On-chip peripheral current consumption**

The current consumption of the on-chip peripherals is given in [Table 18](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 5](#).

Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C <sup>(1)</sup>	Unit
APB1	TIM2	0.52	mA
	TIM3	0.46	
	TIM4	0.5	
	TIM6	0.125	
	TIM7	0.19	
	DAC	0.5 <sup>(2)</sup>	
	WWDG	0.13	
	SPI2	0.2	
	USART2	0.38	
	USART3	0.32	
	I2C1	0.27	
	I2C2	0.28	
	HDMI CEC	0.16	
APB2	GPIO A	0.25	
	GPIO B	0.12	
	GPIO C	0.18	
	GPIO D	0.15	
	GPIO E	0.15	
	ADC1 <sup>(3)</sup>	0.15	
	SPI1	0.12	
	USART1	0.27	
	TIM1	0.63	
	TIM15	0.33	
	TIM16	0.26	
	TIM17	0.25	

1.  $f_{HCLK} = f_{APB1} = f_{APB2} = 24$  MHz, default prescaler value for each peripheral.

2. Specific conditions for DAC: EN1 bit in DAC\_CR register set to 1.

3. Specific conditions for ADC:  $f_{HCLK} = 24$  MHz,  $f_{APB1} = f_{APB2} = f_{HCLK}$ ,  $f_{ADCCLK} = f_{APB2}/2$ , ADON bit in the ADC\_CR2 register is set to 1.

### 5.3.6 External clock source characteristics

#### High-speed external user clock generated from an external source

The characteristics given in [Table 19](#) result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in [Table 8](#).

**Table 19. High-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>HSE_ext</sub>	User external clock source frequency <sup>(1)</sup>		1	8	24	MHz
V <sub>HSEH</sub>	OSC_IN input pin high level voltage		0.7V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>HSEL</sub>	OSC_IN input pin low level voltage		V <sub>SS</sub>		0.3V <sub>DD</sub>	
t <sub>w(HSE)</sub> t <sub>w(HSE)</sub>	OSC_IN high or low time <sup>(1)</sup>		16			ns
t <sub>r(HSE)</sub> t <sub>f(HSE)</sub>	OSC_IN rise or fall time <sup>(1)</sup>				20	
C <sub>in(HSE)</sub>	OSC_IN input capacitance <sup>(1)</sup>			5		pF
DuCy <sub>(HSE)</sub>	Duty cycle		45		55	%
I <sub>L</sub>	OSC_IN Input leakage current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>			±1	μA

1. Guaranteed by design, not tested in production.

**Low-speed external user clock generated from an external source**

The characteristics given in [Table 20](#) result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in [Table 8](#).

**Table 20. Low-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>LSE_ext</sub>	User external clock source frequency <sup>(1)</sup>			32.768	1000	kHz
V <sub>LSEH</sub>	OSC32_IN input pin high level voltage		0.7V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>LSEL</sub>	OSC32_IN input pin low level voltage		V <sub>SS</sub>		0.3V <sub>DD</sub>	
t <sub>w(LSE)</sub> t <sub>w(LSE)</sub>	OSC32_IN high or low time <sup>(1)</sup>		450			ns
t <sub>r(LSE)</sub> t <sub>f(LSE)</sub>	OSC32_IN rise or fall time <sup>(1)</sup>				50	
C <sub>in(LSE)</sub>	OSC32_IN input capacitance <sup>(1)</sup>			5		pF
DuCy <sub>(LSE)</sub>	Duty cycle		30		70	%
I <sub>L</sub>	OSC32_IN Input leakage current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>			±1	μA

1. Guaranteed by design, not tested in production.

Figure 17. High-speed external clock source AC timing diagram

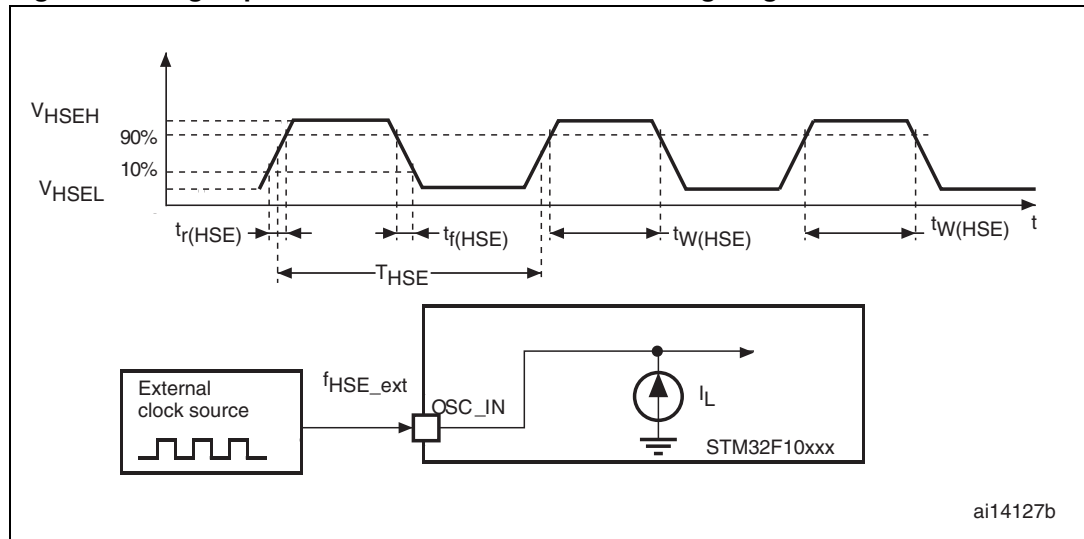
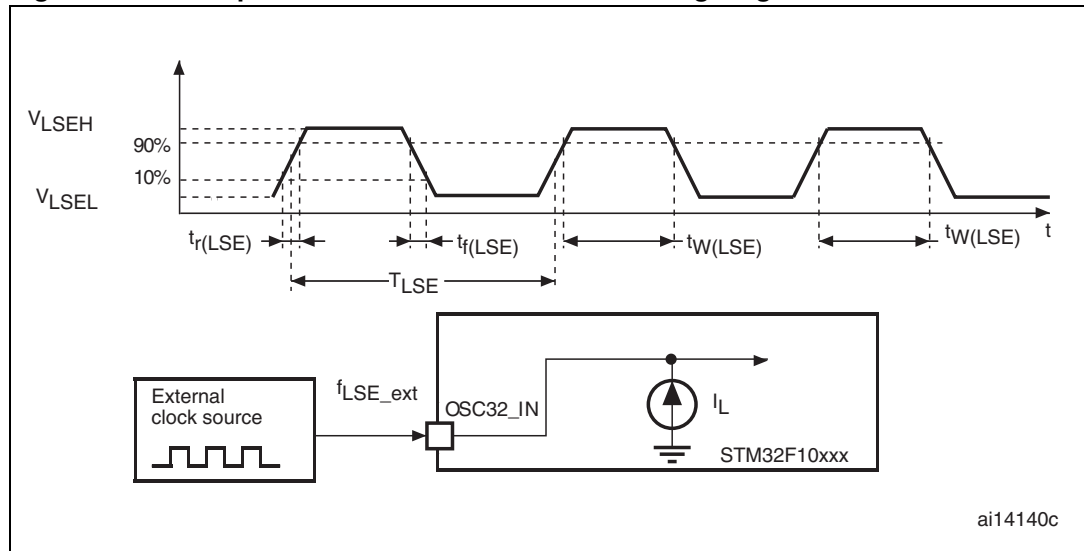


Figure 18. Low-speed external clock source AC timing diagram



**High-speed external clock generated from a crystal/ceramic resonator**

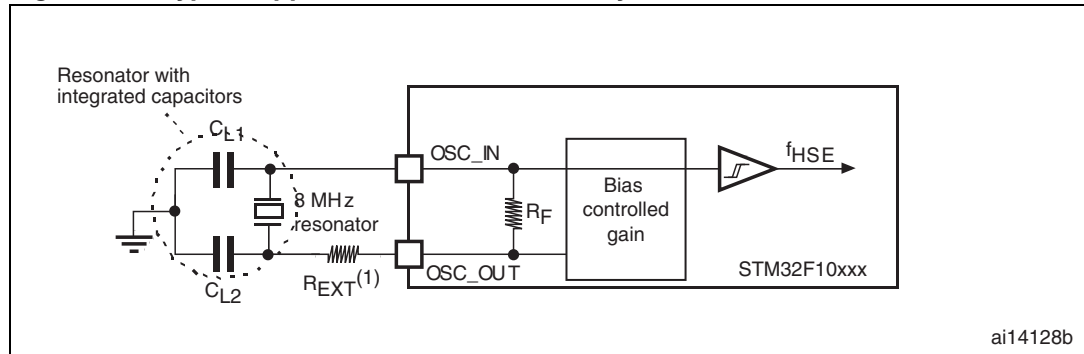
The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 21](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 21. HSE 4-24 MHz oscillator characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OSC\_IN}$	Oscillator frequency		4	8	24	MHz
$R_F$	Feedback resistor			200		k $\Omega$
$C_{L1}$ $C_{L2}^{(3)}$	Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ ) <sup>(4)</sup>	$R_S = 30 \Omega$		30		pF
$i_2$	HSE driving current	$V_{DD} = 3.3 V$ $V_{IN} = V_{SS}$ with 30 pF load			1	mA
$g_m$	Oscillator transconductance	Startup	25			mA/V
$t_{SU(HSE)}^{(5)}$	Startup time	$V_{DD}$ is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator.  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing  $C_{L1}$  and  $C_{L2}$ .
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

**Figure 19. Typical application with an 8 MHz crystal**



1.  $R_{EXT}$  value depends on the crystal characteristics.

**Low-speed external clock generated from a crystal/ceramic resonator**

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 22](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Note:** For  $C_{L1}$  and  $C_{L2}$  it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator.  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ .

Load capacitance  $C_L$  has the following formula:  $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$  where  $C_{stray}$  is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

**Caution:** To avoid exceeding the maximum value of  $C_{L1}$  and  $C_{L2}$  (15 pF) it is strongly recommended to use a resonator with a load capacitance  $C_L \leq 7$  pF. Never use a resonator with a load capacitance of 12.5 pF.

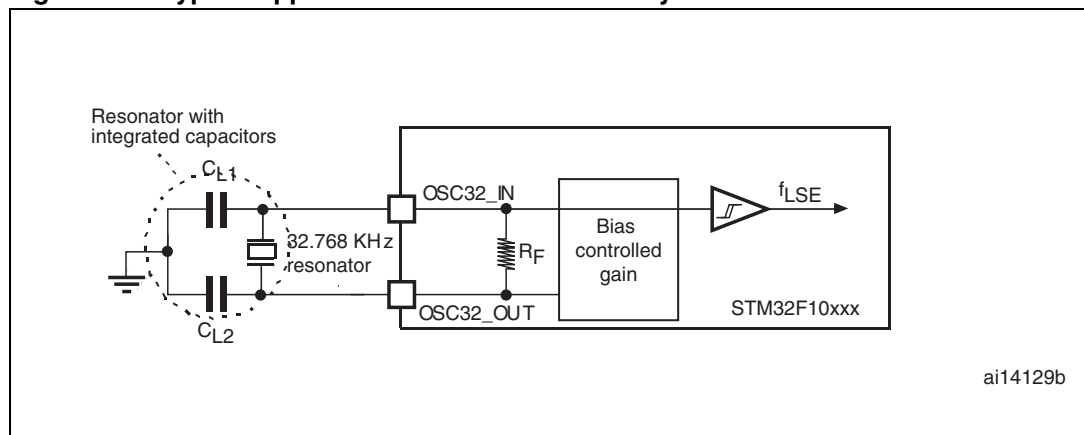
**Example:** if you choose a resonator with a load capacitance of  $C_L = 6$  pF, and  $C_{stray} = 2$  pF, then  $C_{L1} = C_{L2} = 8$  pF.

**Table 22. LSE oscillator characteristics ( $f_{LSE} = 32.768$  kHz)<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_F$	Feedback resistor			5		M $\Omega$
$C_{L1}$ $C_{L2}$ <sup>(2)</sup>	Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ ) <sup>(3)</sup>	$R_S = 30$ K $\Omega$			15	pF
$I_2$	LSE driving current	$V_{DD} = 3.3$ V $V_{IN} = V_{SS}$			1.4	$\mu$ A
$g_m$	Oscillator transconductance		5			$\mu$ A/V
$t_{SU(LSE)}$ <sup>(4)</sup>	Startup time	$V_{DD}$ is stabilized		3		s

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs above the table.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small  $R_S$  value for example MSIV-TIN32.768 kHz. Refer to crystal manufacturer for more details
4.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

**Figure 20. Typical application with a 32.768 kHz crystal**



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### 5.3.7 Internal clock source characteristics

The parameters given in [Table 23](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

#### High-speed internal (HSI) RC oscillator

**Table 23. HSI oscillator characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSI}$	Frequency			8		MHz
$ACC_{HSI}$	Accuracy of HSI oscillator	$T_A = -40$ to $105$ °C	-2.7		3	%
		$T_A = -10$ to $85$ °C	-2		2.5	%
		$T_A = 0$ to $70$ °C	-2		2.5	%
		$T_A = 25$ °C	-0.7		1	%
$t_{su(HSI)}$	HSI oscillator startup time		1		2	μs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	μA

1. Guaranteed by design, not tested in production.
2.  $V_{DD} = 3.3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.

#### Low-speed internal (LSI) RC oscillator

**Table 24. LSI oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}$	Frequency	30	40	60	kHz
$t_{su(LSI)}^{(2)}$	LSI oscillator startup time			85	μs
$I_{DD(LSI)}^{(2)}$	LSI oscillator power consumption		0.65	1.2	μA

1.  $V_{DD} = 3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

#### Wakeup time from low-power mode

The wakeup times given in [Table 25](#) are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 25. Low-power mode wakeup timings**

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}^{(1)}$	Wakeup from Sleep mode	1.8	μs

**Table 25. Low-power mode wakeup timings (continued)**

Symbol	Parameter	Typ	Unit
$t_{WUSTOP}^{(1)}$	Wakeup from Stop mode (regulator in run mode)	3.6	$\mu\text{s}$
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}^{(1)}$	Wakeup from Standby mode	50	$\mu\text{s}$

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

### 5.3.8 PLL characteristics

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 26. PLL characteristics**

Symbol	Parameter	Value			Unit
		Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	
$f_{PLL\_IN}$	PLL input clock <sup>(2)</sup>	1	8.0	24	MHz
	PLL input clock duty cycle	40		60	%
$f_{PLL\_OUT}$	PLL multiplier output clock	16		24	MHz
$t_{LOCK}$	PLL lock time			200	$\mu\text{s}$
Jitter	Cycle-to-cycle jitter			300	ps

1. Based on device characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by  $f_{PLL\_OUT}$ .

### 5.3.9 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $105$  °C unless otherwise specified.

**Table 27. Flash memory characteristics**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
$t_{\text{prog}}$	16-bit programming time	$T_A = -40$ to $+105$ °C	40	52.5	70	μs
$t_{\text{ERASE}}$	Page (1 KB) erase time	$T_A = -40$ to $+105$ °C	20		40	ms
$t_{\text{ME}}$	Mass erase time	$T_A = -40$ to $+105$ °C	20		40	ms
$I_{\text{DD}}$	Supply current	Read mode $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V			20	mA
		Write / Erase modes $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V			5	mA
		Power-down mode / Halt, $V_{\text{DD}} = 3.0$ to $3.6$ V			50	μA
$V_{\text{prog}}$	Programming voltage		2		3.6	V

1. Guaranteed by design, not tested in production.

**Table 28. Flash memory endurance and data retention**

Symbol	Parameter	Conditions	Value			Unit
			Min <sup>(1)</sup>	Typ	Max	
$N_{\text{END}}$	Endurance	$T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions)	10			kcycles
$t_{\text{RET}}$	Data retention	1 kcycle <sup>(2)</sup> at $T_A = 85$ °C	30			Years
		1 kcycle <sup>(2)</sup> at $T_A = 105$ °C	10			
		10 kcycles <sup>(2)</sup> at $T_A = 55$ °C	20			

1. Based on characterization not tested in production.

2. Cycling performed over the whole temperature range.

### 5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 29](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 29. EMS characteristics**

Symbol	Parameter	Conditions	Level/Class
$V_{FESD}$	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 24\text{ MHz}$ , LQFP100 package, conforms to IEC 61000-4-2	2B
$V_{EFTB}$	Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 24\text{ MHz}$ , LQFP100 package, conforms to IEC 61000-4-4	4A

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 30. EMI characteristics**

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f <sub>HSE</sub> /f <sub>HCLK</sub> ]	Unit
				8/24 MHz	
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25°C, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	9	dBµV
			30 MHz to 130 MHz	17	
			130 MHz to 1GHz	16	
			SAE EMI Level	4	-

**5.3.11 Absolute maximum ratings (electrical sensitivity)**

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 31. ESD absolute maximum ratings**

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (human body model)	T <sub>A</sub> = +25 °C conforming to JESD22-A114	2	TBD	V
V <sub>ESD(CDM)</sub>	Electrostatic discharge voltage (charge device model)	T <sub>A</sub> = +25 °C conforming to JESD22-C101	II	TBD	

1. Based on characterization results, not tested in production.

**Static latch-up**

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78 IC latch-up standard.

**Table 32. Electrical sensitivities**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T <sub>A</sub> = +105 °C conforming to JESD78	TBD

### 5.3.12 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 33](#) are derived from tests performed under the conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

**Table 33. I/O static characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Standard I/O input low level voltage		-0.5		$0.28 (V_{DD}-2) + 0.8$	V
	I/O FT <sup>(1)</sup> input low level voltage		-0.5		$0.32 (V_{DD}-2) + 0.75$	
$V_{IH}$	Standard I/O input high level voltage		$0.41 (V_{DD}-2) + 1.3$		$V_{DD} + 0.5$	
	I/O FT <sup>(1)</sup> input high level voltage		$0.42 (V_{DD}-2) + 1$		5.5	
$V_{hys}$	Standard I/O Schmitt trigger voltage hysteresis <sup>(2)</sup>		200			mV
	I/O FT Schmitt trigger voltage hysteresis <sup>(2)</sup>		$5\% V_{DD}$ <sup>(3)</sup>			mV
$I_{lkg}$	Input leakage current <sup>(4)</sup>	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			$\pm 1$	$\mu A$
		$V_{IN} = 5 V$ I/O FT			3	
$R_{PU}$	Weak pull-up equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
$R_{PD}$	Weak pull-down equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{DD}$	30	40	50	$k\Omega$
$C_{IO}$	I/O pin capacitance			5		pF

1. FT = 5V tolerant. To sustain a voltage higher than  $V_{DD} + 0.5$  the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 21](#) and [Figure 22](#) for standard I/Os, and in [Figure 23](#) and [Figure 24](#) for 5 V tolerant I/Os.

Figure 21. Standard I/O input characteristics - CMOS port

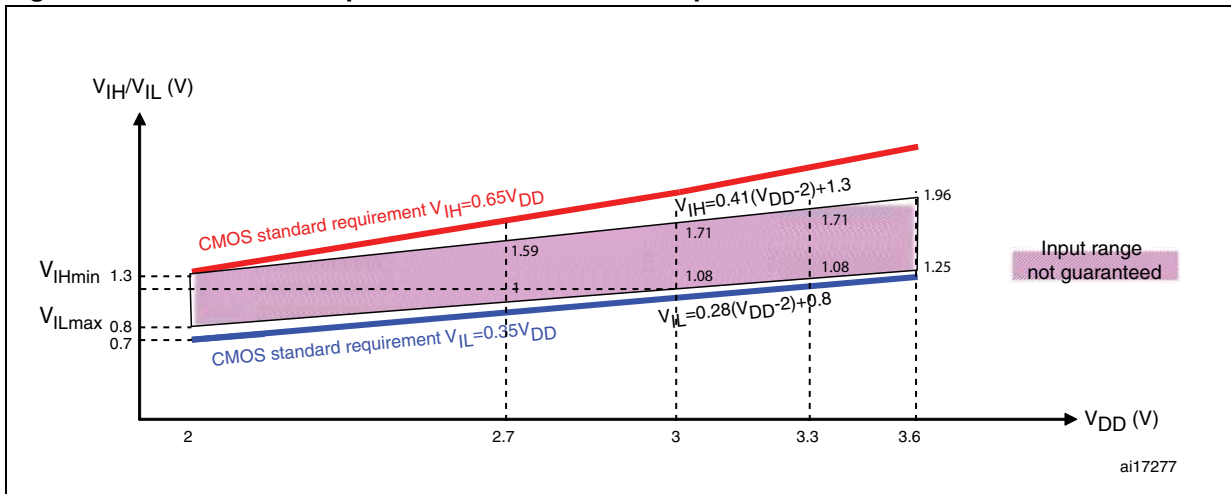


Figure 22. Standard I/O input characteristics - TTL port

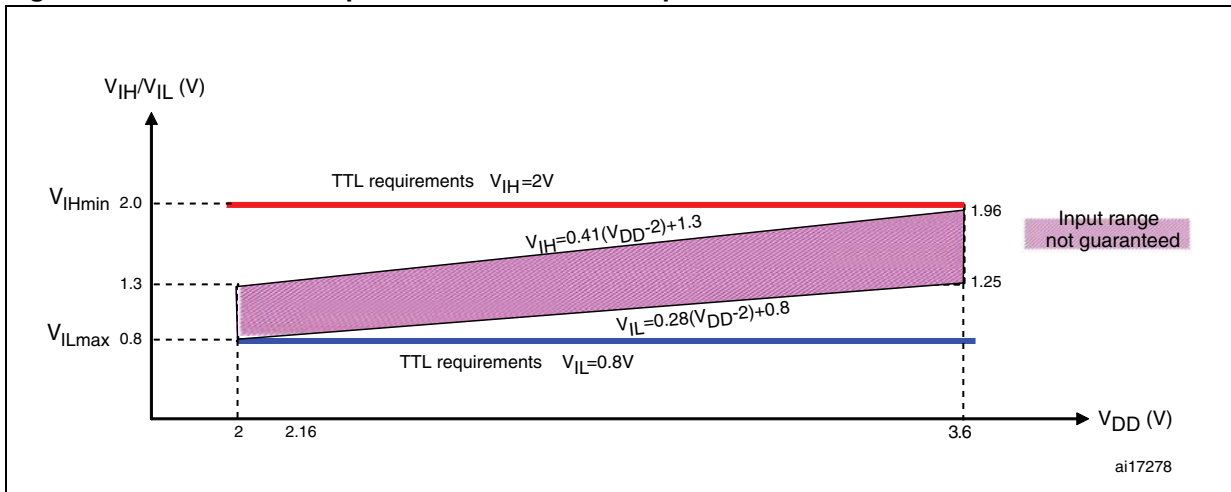


Figure 23. 5 V tolerant I/O input characteristics - CMOS port

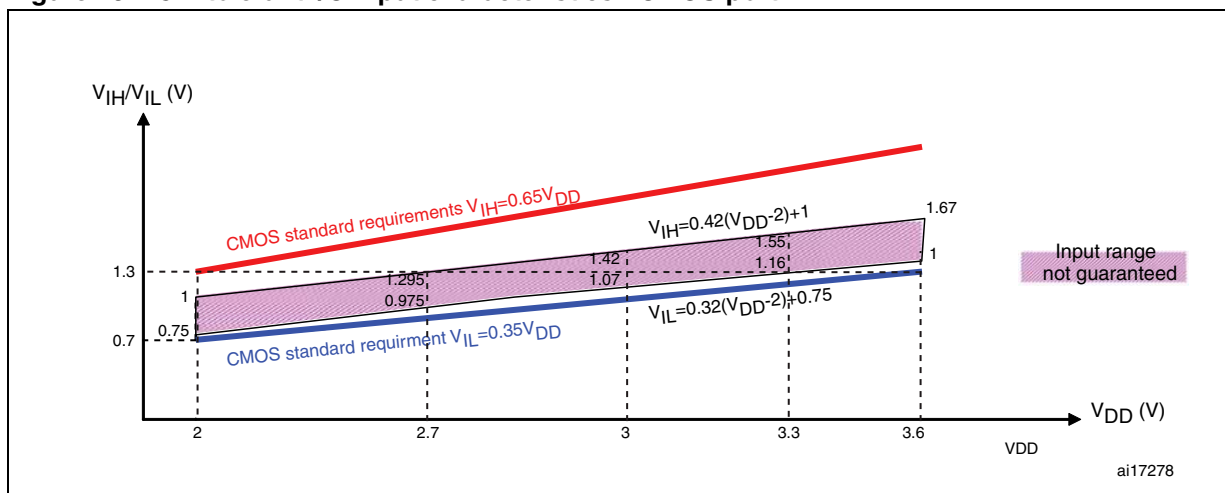
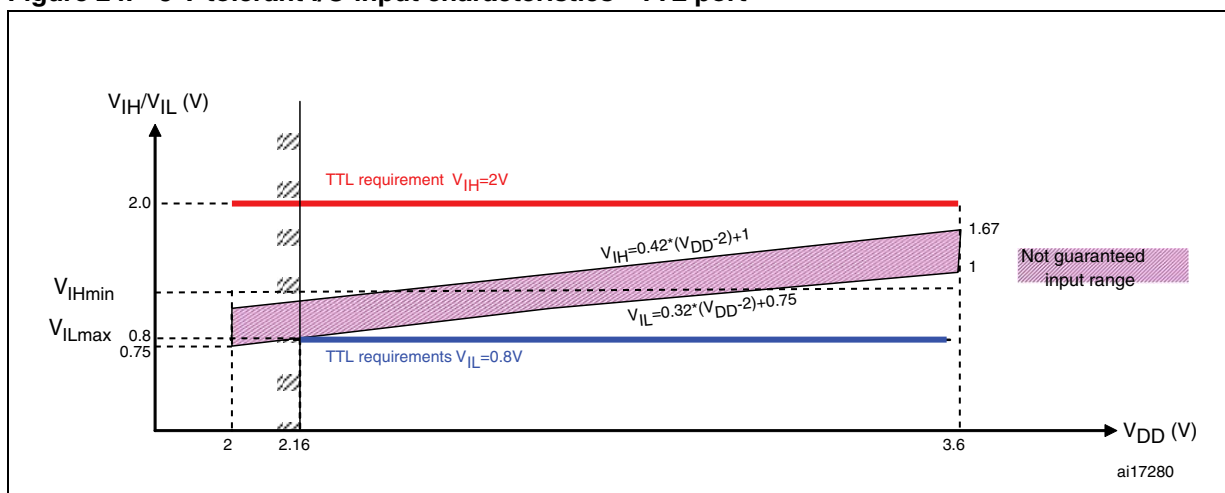


Figure 24. 5 V tolerant I/O input characteristics - TTL port



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed  $V_{OL}$ ).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $I_{VDD}$  (see [Table 6](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $I_{VSS}$  (see [Table 6](#)).



### Output voltage levels

Unless otherwise specified, the parameters given in [Table 34](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

**Table 34. Output voltage characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port, $I_{IO} = +8 \text{ mA}$ , $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +20 \text{ mA}^{(3)}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		1.3	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-1.3$		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +6 \text{ mA}^{(3)}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$		

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
2. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD}$ .
3. Based on characterization data, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 25](#) and [Table 35](#), respectively.

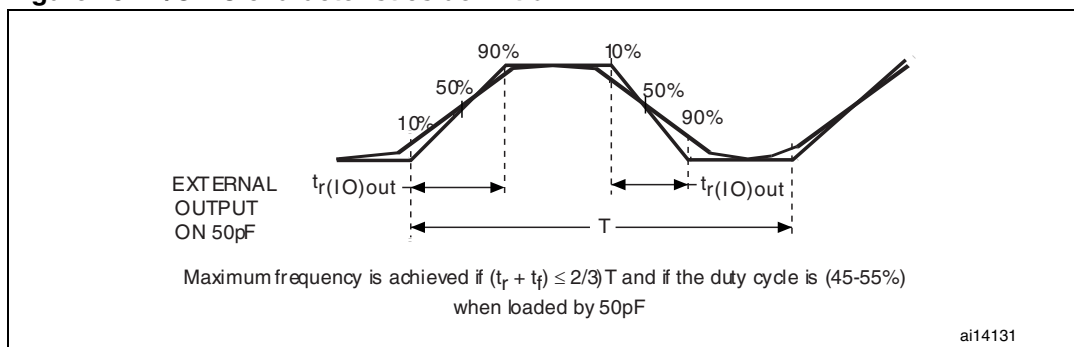
Unless otherwise specified, the parameters given in [Table 35](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 35. I/O AC characteristics<sup>(1)</sup>**

MODEx [1:0] bit value <sup>(1)</sup>	Symbol	Parameter	Conditions	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	125 <sup>(3)</sup>	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		125 <sup>(3)</sup>	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	10	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	25 <sup>(3)</sup>	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		25 <sup>(3)</sup>	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	24	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 <sup>(3)</sup>	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 <sup>(3)</sup>	
			$C_L = 50 \text{ pF}$ , $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 <sup>(3)</sup>	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 <sup>(3)</sup>	
			$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 <sup>(3)</sup>	
$C_L = 50 \text{ pF}$ , $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$			12 <sup>(3)</sup>		
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller		10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 25](#).
3. Guaranteed by design, not tested in production.

Figure 25. I/O AC characteristics definition



### 5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see Table 33).

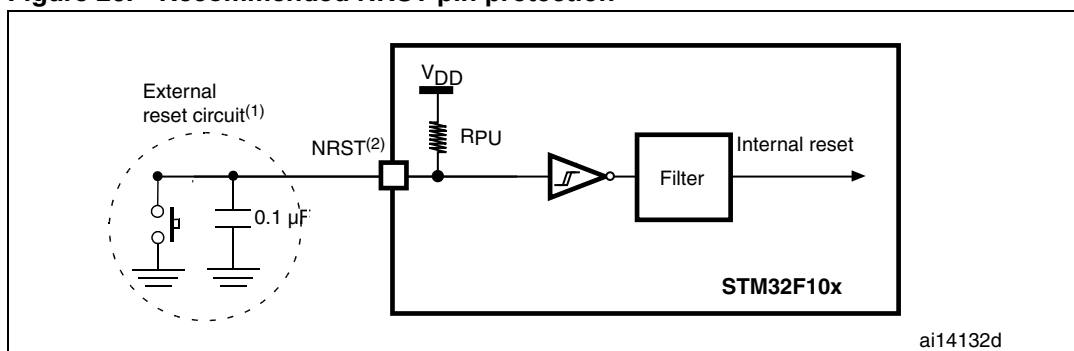
Unless otherwise specified, the parameters given in Table 36 are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in Table 8.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage		-0.5		0.8	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage		2		$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
$R_{PU}$	Weak pull-up equivalent resistor <sup>(2)</sup>	$V_{IN} = V_{SS}$	30	40	50	k $\Omega$
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 26. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in Table 36. Otherwise the reset will not be taken into account by the device.

### 5.3.14 TIMx characteristics

The parameters given in [Table 37](#) are guaranteed by design.

Refer to [Section 5.3.12: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 37. TIMx characteristics**

Symbol	Parameter	Conditions <sup>(1)</sup>	Min	Max	Unit
$t_{\text{res(TIM)}}$	Timer resolution time		1		$t_{\text{TIMxCLK}}$
		$f_{\text{TIMxCLK}} = 24 \text{ MHz}$	41.7		ns
$f_{\text{EXT}}$	Timer external clock frequency on CHx <sup>(2)</sup>		0	$f_{\text{TIMxCLK}}/2$	MHz
		$f_{\text{TIMxCLK}} = 24 \text{ MHz}$	0	12	MHz
$\text{Res}_{\text{TIM}}$	Timer resolution			16	bit
$t_{\text{COUNTER}}$	16-bit counter clock period when the internal clock is selected		1	65536	$t_{\text{TIMxCLK}}$
		$f_{\text{TIMxCLK}} = 24 \text{ MHz}$		2730	$\mu\text{s}$
$t_{\text{MAX\_COUNT}}$	Maximum possible count			$65536 \times 65536$	$t_{\text{TIMxCLK}}$
		$f_{\text{TIMxCLK}} = 24 \text{ MHz}$		178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3 and TIM4, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

### 5.3.15 Communications interfaces

#### I<sup>2</sup>C interface characteristics

Unless otherwise specified, the parameters given in [Table 38](#) are derived from tests performed under the ambient temperature,  $f_{\text{PCLK1}}$  frequency and  $V_{\text{DD}}$  supply voltage conditions summarized in [Table 8](#).

The STM32F100xx value line I<sup>2</sup>C interface meets the requirements of the standard I<sup>2</sup>C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and  $V_{\text{DD}}$  is disabled, but is still present.

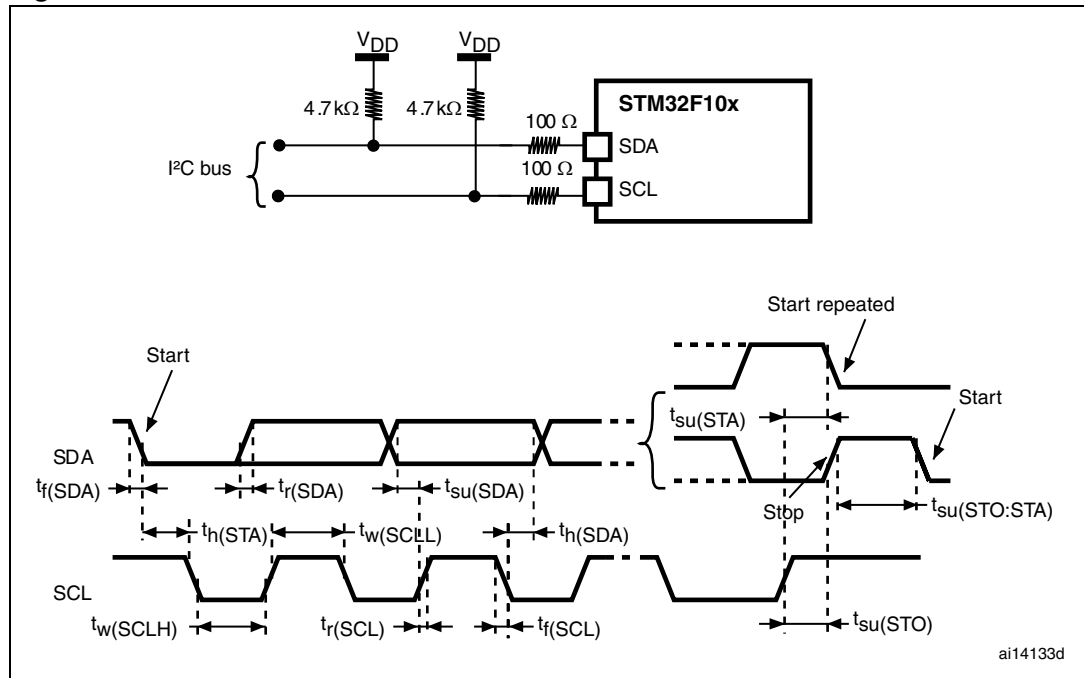
The I<sup>2</sup>C characteristics are described in [Table 38](#). Refer also to [Section 5.3.12: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 38. I<sup>2</sup>C characteristics

Symbol	Parameter	Standard mode I <sup>2</sup> C <sup>(1)</sup>		Fast mode I <sup>2</sup> C <sup>(1)(2)</sup>		Unit
		Min	Max	Min	Max	
t <sub>w(SCLL)</sub>	SCL clock low time	4.7		1.3		μs
t <sub>w(SCLH)</sub>	SCL clock high time	4.0		0.6		
t <sub>su(SDA)</sub>	SDA setup time	250		100		ns
t <sub>h(SDA)</sub>	SDA data hold time	0 <sup>(3)</sup>		0 <sup>(4)</sup>	900 <sup>(3)</sup>	
t <sub>r(SDA)</sub> t <sub>r(SCL)</sub>	SDA and SCL rise time		1000		300	
t <sub>f(SDA)</sub> t <sub>f(SCL)</sub>	SDA and SCL fall time		300		300	
t <sub>h(STA)</sub>	Start condition hold time	4.0		0.6		μs
t <sub>su(STA)</sub>	Repeated Start condition setup time	4.7		0.6		
t <sub>su(STO)</sub>	Stop condition setup time	4.0		0.6		μs
t <sub>w(STO:STA)</sub>	Stop to Start condition time (bus free)	4.7		1.3		μs
C <sub>b</sub>	Capacitive load for each bus line		400		400	pF

1. Guaranteed by design, not tested in production.
2. f<sub>PCLK1</sub> must be higher than 2 MHz to achieve standard mode I<sup>2</sup>C frequencies. It must be higher than 4 MHz to achieve fast mode I<sup>2</sup>C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I<sup>2</sup>C fast mode clock.
3. The maximum hold time of the Start condition only has to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 27. I<sup>2</sup>C bus AC waveforms and measurement circuit<sup>(1)</sup>



1. Measurement points are done at CMOS levels: 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>.

Table 39. SCL frequency (f<sub>PCLK1</sub>= 24 MHz, V<sub>DD</sub> = 3.3 V)<sup>(1)(2)</sup>

f <sub>SCL</sub> (kHz)	I2C_CCR value
	R <sub>P</sub> = 4.7 kΩ
400	0x8011
300	0x8016
200	0x8021
100	0x0064
50	0x00C8
20	0x01F4

1. R<sub>P</sub> = External pull-up resistance, f<sub>SCL</sub> = I<sup>2</sup>C speed,
2. For speeds around 400 kHz, the tolerance on the achieved speed is of ±2%. For other speed ranges, the tolerance on the achieved speed ±1%. These variations depend on the accuracy of the external components used to design the application.

### SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 40](#) are derived from tests performed under the ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

Refer to [Section 5.3.12: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 40. SPI characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}$ $1/t_{c(SCK)}$	SPI clock frequency	Master mode		12	MHz
		Slave mode		12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}^{(2)}$	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}^{(2)}$	NSS hold time	Slave mode	$2t_{PCLK}$		
$t_{w(SCKH)}^{(2)}$ $t_{w(SCKL)}^{(2)}$	SCK high and low time	Master mode, $f_{PCLK} = 24$ MHz, presc = 4	50	60	
$t_{su(MI)}^{(2)}$ $t_{su(SI)}^{(2)}$	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}^{(2)}$ $t_{h(SI)}^{(2)}$	Data input hold time	Master mode	5		
		Slave mode	4		
$t_{a(SO)}^{(2)(3)}$	Data output access time	Slave mode, $f_{PCLK} = 24$ MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}^{(2)(4)}$	Data output disable time	Slave mode	2	10	
$t_{v(SO)}^{(2)(1)}$	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}^{(2)(1)}$	Data output valid time	Master mode (after enable edge)		5	
$t_{h(SO)}^{(2)}$	Data output hold time	Slave mode (after enable edge)	15		
$t_{h(MO)}^{(2)}$		Master mode (after enable edge)	2		

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 28. SPI timing diagram - slave mode and CPHA = 0

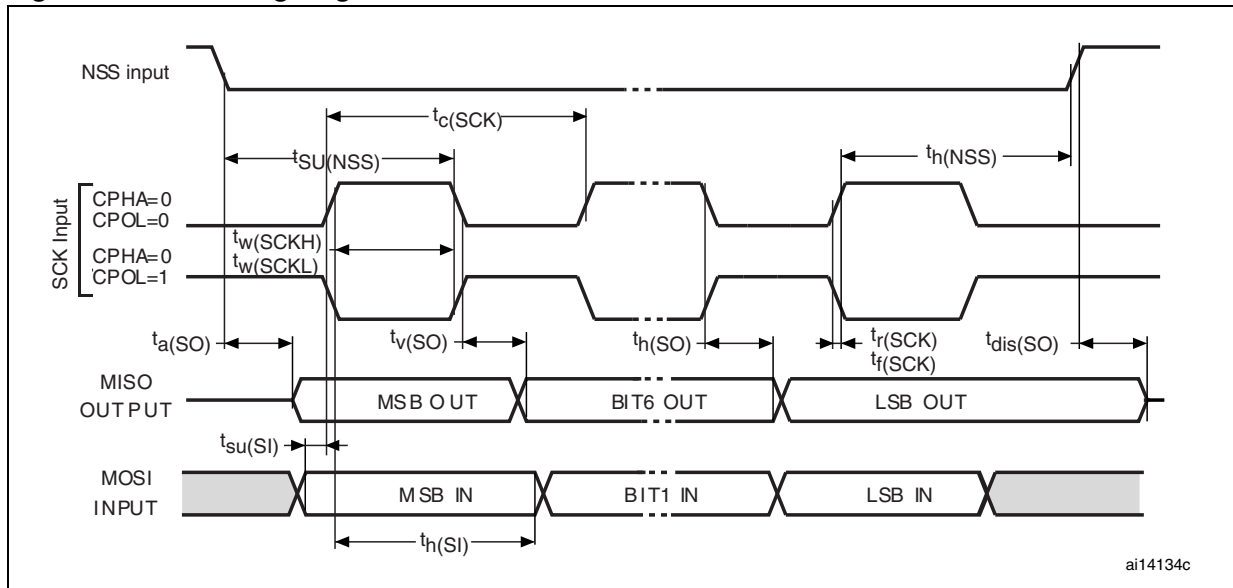
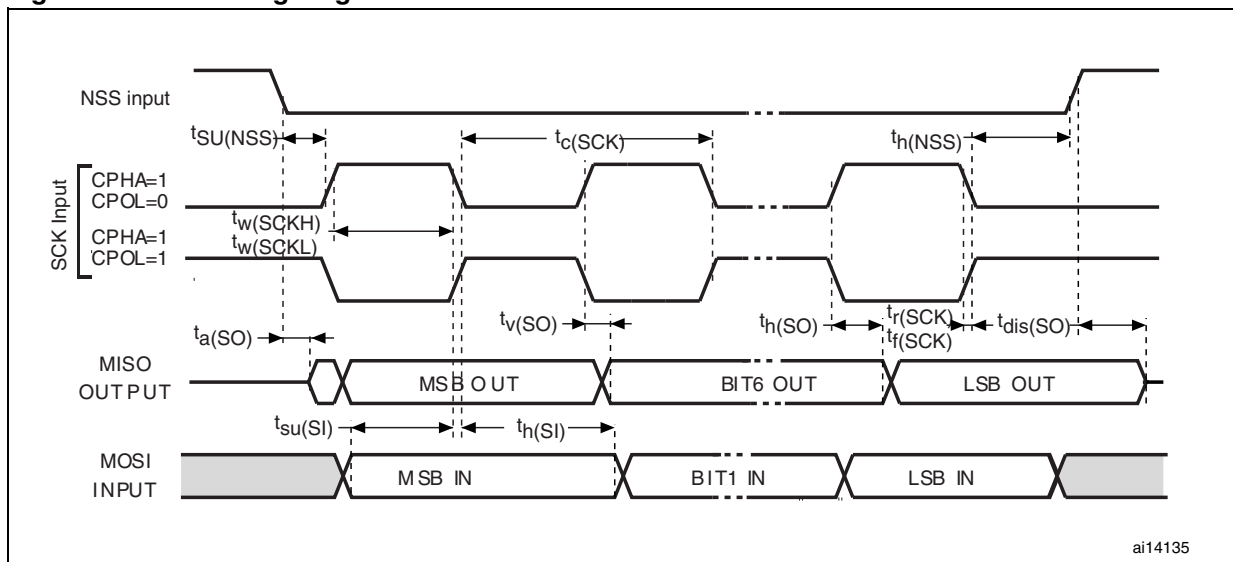


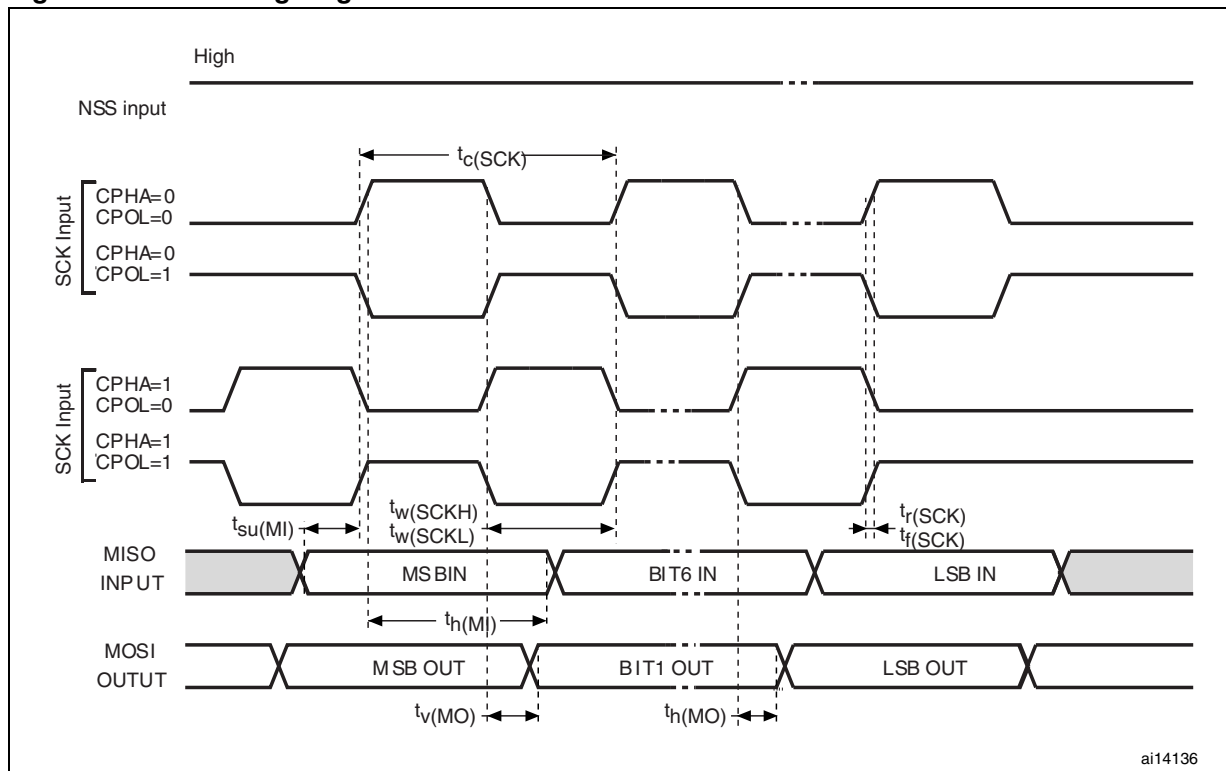
Figure 29. SPI timing diagram - slave mode and CPHA = 1<sup>(1)</sup>



1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .



Figure 30. SPI timing diagram - master mode<sup>(1)</sup>



1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

### HDMI consumer electronics control (CEC)

Refer to [Section 5.3.12: I/O port characteristics](#) for more details on the input/output alternate function characteristics.

### 5.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 41](#) are derived from tests performed under the ambient temperature,  $f_{PCLK2}$  frequency and  $V_{DDA}$  supply voltage conditions summarized in [Table 8](#).

*Note:* It is recommended to perform a calibration after each power-up.

Table 41. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DDA</sub>	Power supply		2.4		3.6	V
V <sub>REF+</sub>	Positive reference voltage		2.4		V <sub>DDA</sub>	V
I <sub>VREF</sub>	Current on the V <sub>REF</sub> input pin			160 <sup>(1)</sup>	220 <sup>(1)</sup>	μA
f <sub>ADC</sub>	ADC clock frequency		0.6		10	MHz
f <sub>S</sub> <sup>(2)</sup>	Sampling rate		0.05		1	MHz
f <sub>TRIG</sub> <sup>(2)</sup>	External trigger frequency	f <sub>ADC</sub> = 12 MHz			823	kHz
					17	1/f <sub>ADC</sub>
V <sub>AIN</sub> <sup>(3)</sup>	Conversion voltage range		0 (V <sub>SSA</sub> tied to ground)		V <sub>REF+</sub>	V
R <sub>AIN</sub> <sup>(2)</sup>	External input impedance	See <a href="#">Equation 1</a> and <a href="#">Table 42</a> for details			50	kΩ
R <sub>ADC</sub> <sup>(2)</sup>	Sampling switch resistance				1	kΩ
C <sub>ADC</sub> <sup>(2)</sup>	Internal sample and hold capacitor				8	pF
t <sub>CAL</sub> <sup>(2)</sup>	Calibration time	f <sub>ADC</sub> = 12 MHz	5.9			μs
			83			1/f <sub>ADC</sub>
t <sub>lat</sub> <sup>(2)</sup>	Injection trigger conversion latency	f <sub>ADC</sub> = 12 MHz			0.214	μs
					3 <sup>(4)</sup>	1/f <sub>ADC</sub>
t <sub>latr</sub> <sup>(2)</sup>	Regular trigger conversion latency	f <sub>ADC</sub> = 12 MHz			0.143	μs
					2 <sup>(4)</sup>	1/f <sub>ADC</sub>
t <sub>S</sub> <sup>(2)</sup>	Sampling time	f <sub>ADC</sub> = 12 MHz	0.125		17.1	μs
			1.5		239.5	1/f <sub>ADC</sub>
t <sub>STAB</sub> <sup>(2)</sup>	Power-up time		0	0	1	μs
t <sub>CONV</sub> <sup>(2)</sup>	Total conversion time (including sampling time)	f <sub>ADC</sub> = 12 MHz	1.17		21	μs
			14 to 252 (t <sub>S</sub> for sampling + 12.5 for successive approximation)			1/f <sub>ADC</sub>

1. Based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. In devices delivered in LQFP packages, V<sub>REF+</sub> is internally connected to V<sub>DDA</sub> and V<sub>REF-</sub> is internally connected to V<sub>SSA</sub>. Devices that come in the TFBGA64 package have a V<sub>REF+</sub> pin but no V<sub>REF-</sub> pin (V<sub>REF-</sub> is internally connected to V<sub>SSA</sub>), see [Table 4: STM32F100xx pin definitions](#) and [Figure 6](#).
4. For external triggers, a delay of 1/f<sub>PCLK2</sub> must be added to the latency specified in [Table 41](#).

**Equation 1: R<sub>AIN</sub> max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 42.  $R_{AIN}$  max for  $f_{ADC} = 12$  MHz<sup>(1)</sup>**

$T_s$ (cycles)	$t_s$ ( $\mu$ s)	$R_{AIN}$ max (k $\Omega$ )
1.5	0.125	0.4
7.5	0.625	5.9
13.5	1.125	11.4
28.5	2.375	25.2
41.5	3.45	37.2
55.5	4.625	50
71.5	5.96	NA
239.5	20	NA

1. Guaranteed by design, not tested in production.

**Table 43. ADC accuracy - limited test conditions<sup>(1)(2)</sup>**

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	$f_{PCLK2} = 24$ MHz, $f_{ADC} = 12$ MHz, $R_{AIN} < 10$ k $\Omega$ , $V_{DDA} = 3$ V to 3.6 V $T_A = 25$ °C Measurements made after ADC calibration	$\pm 1.3$	$\pm 2$	LSB
EO	Offset error		$\pm 1$	$\pm 1.5$	
EG	Gain error		$\pm 0.5$	$\pm 1.5$	
ED	Differential linearity error		$\pm 0.7$	$\pm 1$	
EL	Integral linearity error		$\pm 0.8$	$\pm 1.5$	

1. ADC DC accuracy values are measured after internal calibration.

2. Based on characterization, not tested in production.

**Table 44. ADC accuracy<sup>(1) (2)</sup>**

Symbol	Parameter	Test conditions	Typ	Max <sup>(3)</sup>	Unit
ET	Total unadjusted error	$f_{PCLK2} = 24$ MHz, $f_{ADC} = 12$ MHz, $R_{AIN} < 10$ k $\Omega$ , $V_{DDA} = 2.4$ V to 3.6 V Measurements made after ADC calibration	$\pm 2$	$\pm 5$	LSB
EO	Offset error		$\pm 1.5$	$\pm 2.5$	
EG	Gain error		$\pm 1.5$	$\pm 3$	
ED	Differential linearity error		$\pm 1$	$\pm 2$	
EL	Integral linearity error		$\pm 1.5$	$\pm 3$	

1. ADC DC accuracy values are measured after internal calibration.

2. Better performance could be achieved in restricted  $V_{DD}$ , frequency,  $V_{REF}$  and temperature ranges.

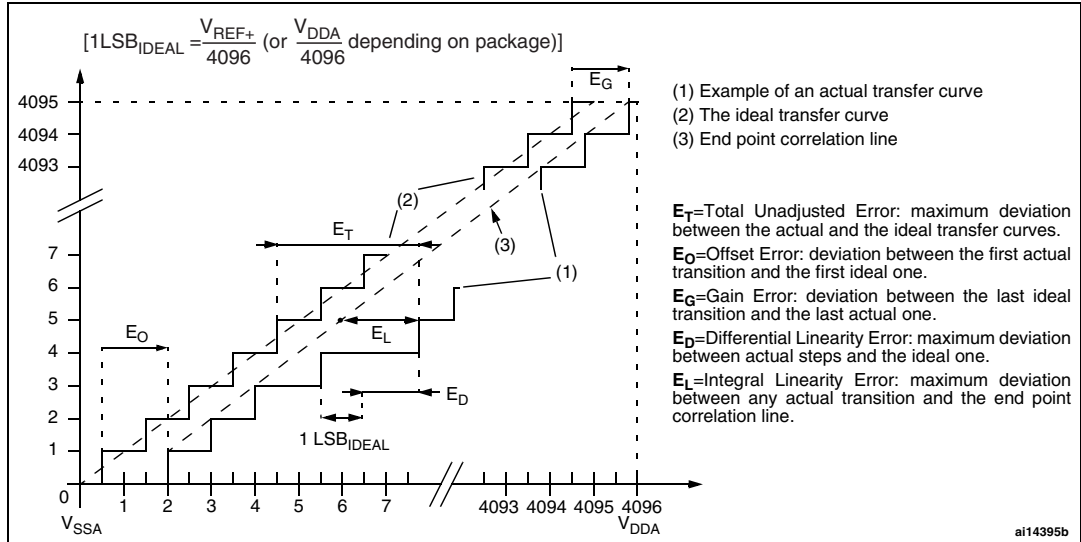
3. Based on characterization, not tested in production.

**Note:** ADC accuracy vs. negative injection current: Injecting a negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject

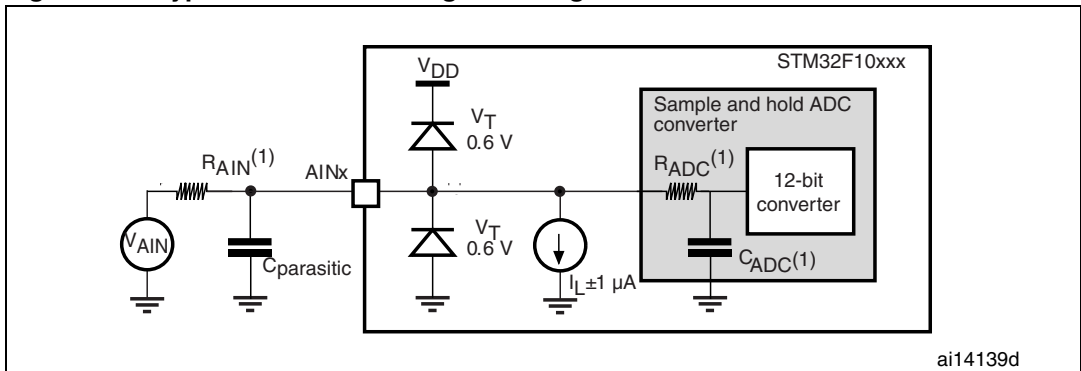
negative currents.

Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 5.3.12](#) does not affect the ADC accuracy.

**Figure 31. ADC accuracy characteristics**



**Figure 32. Typical connection diagram using the ADC**

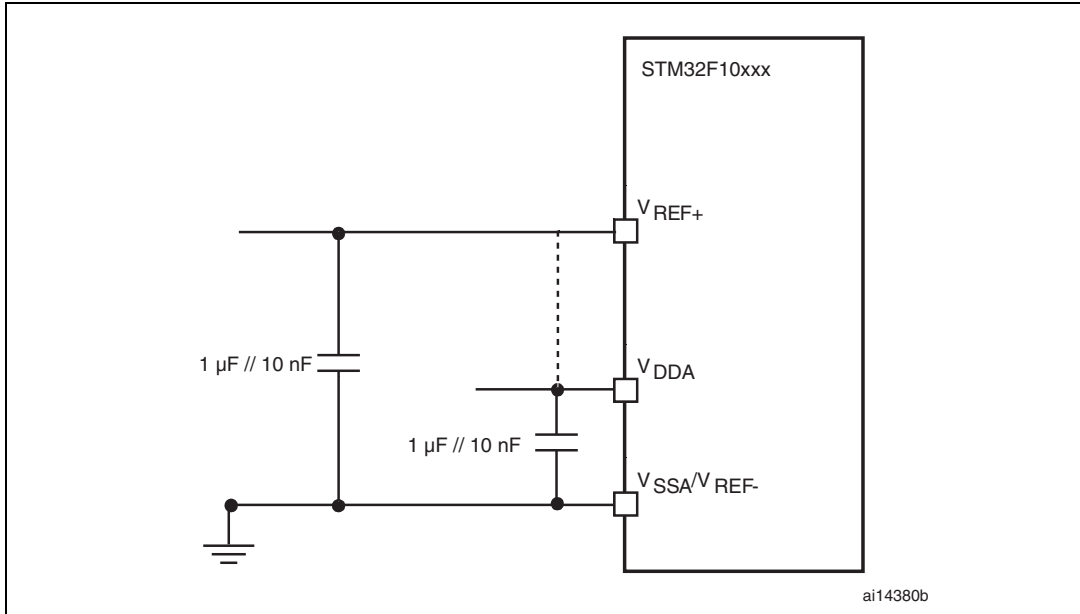


1. Refer to [Table 41](#) for the values of  $R_{\text{AIN}}$ ,  $R_{\text{ADC}}$  and  $C_{\text{ADC}}$ .
2.  $C_{\text{parasitic}}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{\text{parasitic}}$  value will downgrade conversion accuracy. To remedy this,  $f_{\text{ADC}}$  should be reduced.

**General PCB design guidelines**

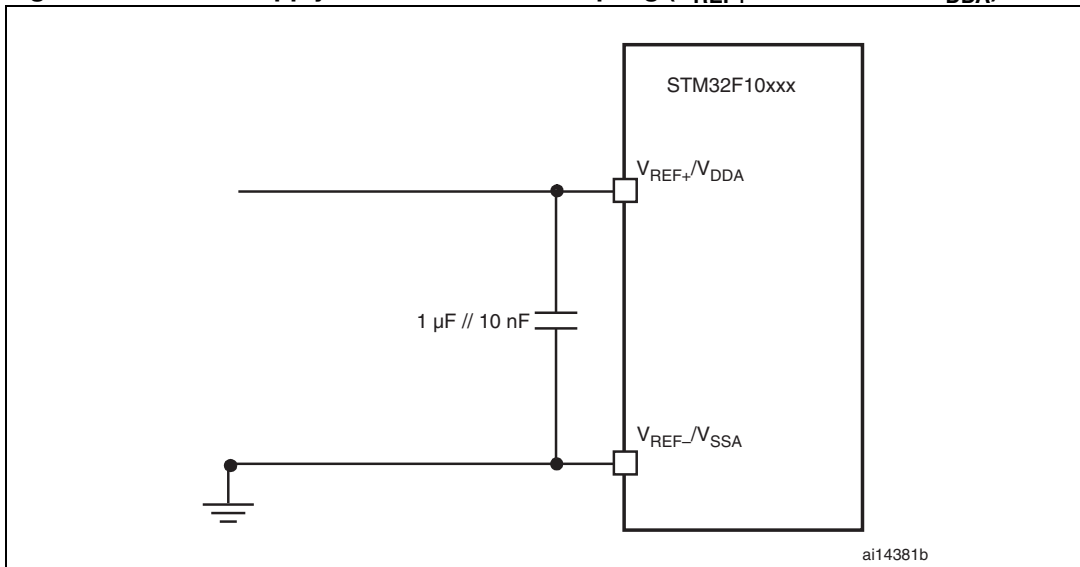
Power supply decoupling should be performed as shown in [Figure 33](#) or [Figure 34](#), depending on whether  $V_{\text{REF+}}$  is connected to  $V_{\text{DDA}}$  or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 33. Power supply and reference decoupling ( $V_{REF+}$  not connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  is available on 100-pin packages and on TFBGA64 packages.  $V_{REF-}$  is available on 100-pin packages only.

**Figure 34. Power supply and reference decoupling ( $V_{REF+}$  connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  and  $V_{REF-}$  inputs are available only on 100-pin packages.

## 5.3.17 DAC electrical specifications

Table 45. DAC characteristics

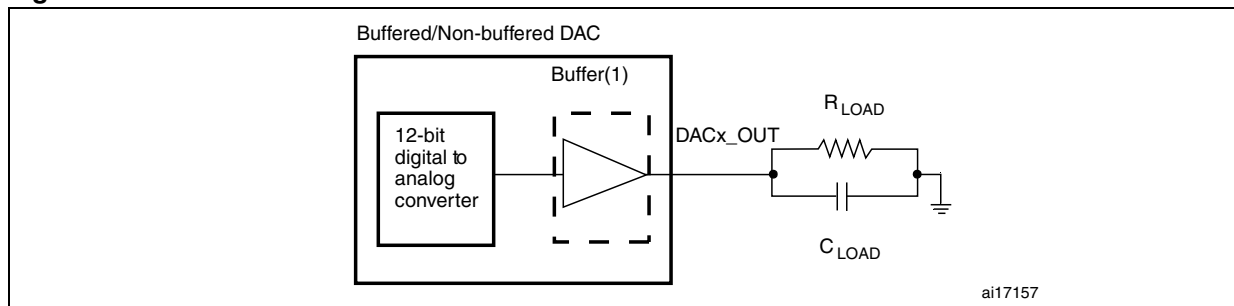
Symbol	Parameter	Min	Typ	Max <sup>(1)</sup>	Unit	Comments
V <sub>DDA</sub>	Analog supply voltage	2.4		3.6	V	
V <sub>REF+</sub>	Reference supply voltage	2.4		3.6	V	V <sub>REF+</sub> must always be below V <sub>DDA</sub>
V <sub>SSA</sub>	Ground	0		0	V	
R <sub>LOAD</sub> <sup>(2)</sup>	Resistive load with buffer ON	5			kΩ	
R <sub>O</sub> <sup>(1)</sup>	Impedance output with buffer OFF			15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V <sub>SS</sub> to have a 1% accuracy is 1.5 MΩ
C <sub>LOAD</sub> <sup>(1)</sup>	Capacitive load			50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min <sup>(1)</sup>	Lower DAC_OUT voltage with buffer ON	0.2			V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V <sub>REF+</sub> = 3.6 V and (0x155) and (0xEAB) at V <sub>REF+</sub> = 2.4 V
DAC_OUT max <sup>(1)</sup>	Higher DAC_OUT voltage with buffer ON			V <sub>DDA</sub> - 0.2	V	
DAC_OUT min <sup>(1)</sup>	Lower DAC_OUT voltage with buffer OFF		0.5		mV	It gives the maximum output excursion of the DAC.
DAC_OUT max <sup>(1)</sup>	Higher DAC_OUT voltage with buffer OFF			V <sub>REF+</sub> - 1LSB	V	
I <sub>DDVREF+</sub>	DAC DC current consumption in quiescent mode (Standby mode)			220	μA	With no load, worst code (0xF1C) at V <sub>REF+</sub> = 3.6 V in terms of DC consumption on the inputs
I <sub>DDA</sub>	DAC DC current consumption in quiescent mode (Standby mode)			380	μA	With no load, middle code (0x800) on the inputs
				480	μA	With no load, worst code (0xF1C) at V <sub>REF+</sub> = 3.6 V in terms of DC consumption on the inputs
DNL <sup>(3)</sup>	Differential non linearity Difference between two consecutive code-1LSB)			±0.5	LSB	Given for the DAC in 10-bit configuration
				±2	LSB	Given for the DAC in 12-bit configuration
INL <sup>(3)</sup>	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)			±1	LSB	Given for the DAC in 10-bit configuration
				±4	LSB	Given for the DAC in 12-bit configuration

**Table 45. DAC characteristics (continued)**

Symbol	Parameter	Min	Typ	Max <sup>(1)</sup>	Unit	Comments
Offset <sup>(3)</sup>	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$ )			±10	mV	Given for the DAC in 12-bit configuration
				±3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6\text{ V}$
				±12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6\text{ V}$
Gain error <sup>(3)</sup>	Gain error			±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}^{(3)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB)		3	4	µs	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$
Update rate <sup>(3)</sup>	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MS/s	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$
$t_{WAKEUP}^{(3)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)		6.5	10	µs	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ <sup>(1)</sup>	Power supply rejection ratio (to $V_{DDA}$ ) (static DC measurement)		-67	-40	dB	No $R_{LOAD}$ , $C_{LOAD} = 50\text{ pF}$

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization, not tested in production.

**Figure 35. 12-bit buffered /non-buffered DAC**



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

### 5.3.18 Temperature sensor characteristics

Table 46. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	$V_{SENSE}$ linearity with temperature		$\pm 1$	$\pm 2$	$^{\circ}\text{C}$
Avg_Slope <sup>(1)</sup>	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	1.32	1.41	1.50	V
$t_{START}^{(2)}$	Startup time	4		10	$\mu\text{s}$
$T_{S\_temp}^{(3)(2)}$	ADC sampling time when reading the temperature			17.1	$\mu\text{s}$

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.



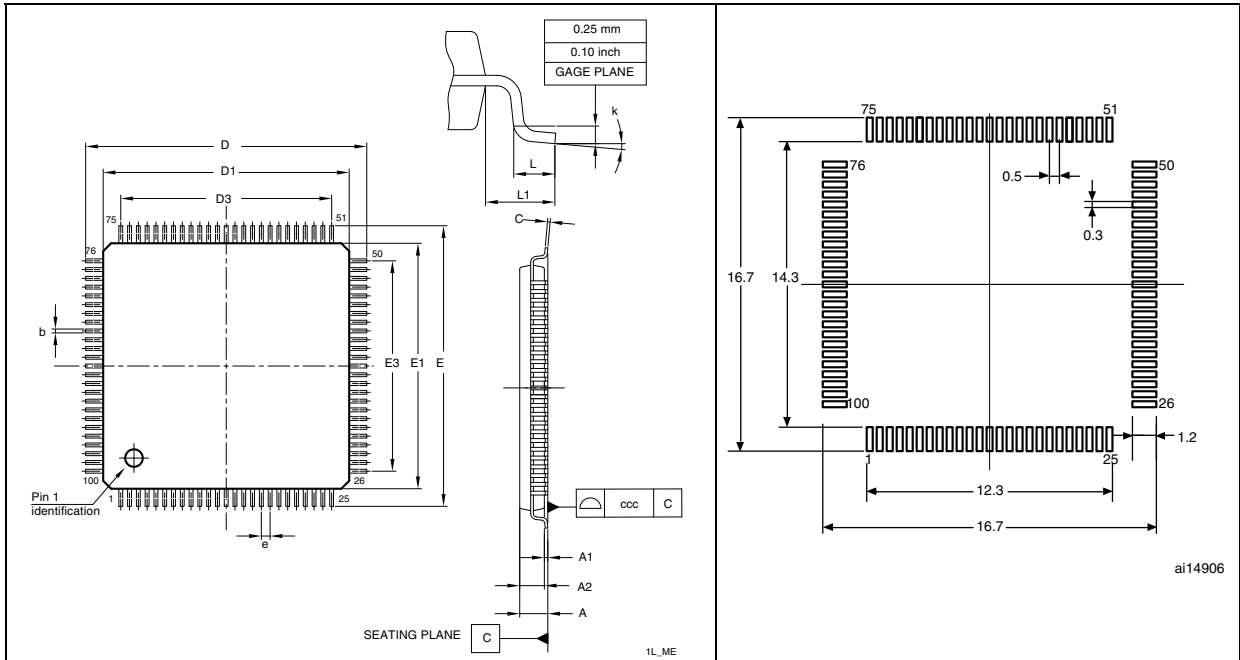
## 6 Package characteristics

### 6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 36. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline<sup>(1)</sup>

Figure 37. Recommended footprint<sup>(1)(2)</sup>



1. Drawing is not to scale.
2. Dimensions are in millimeters.

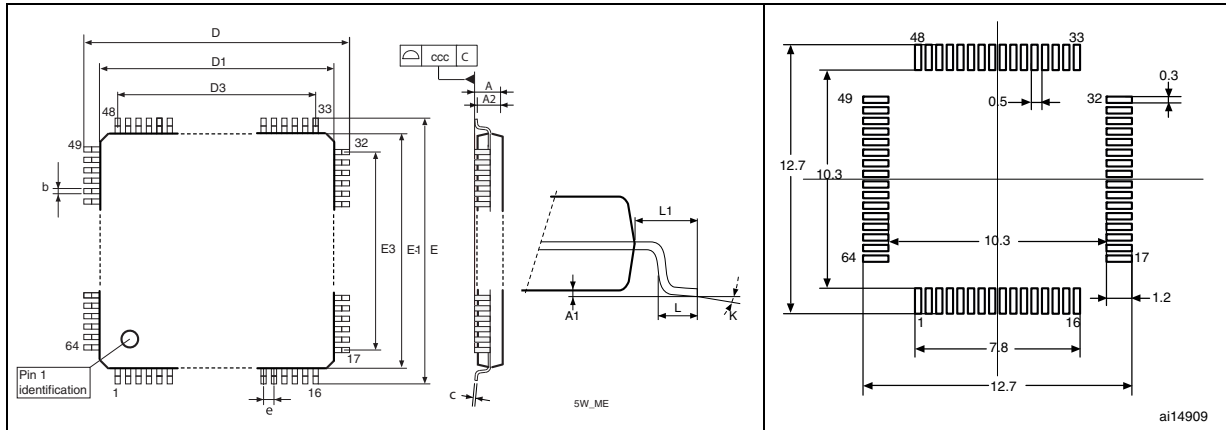
Table 47. LQFP100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.2	0.0035		0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3		12.00			0.4724	
E	15.80	16.00	16.2	0.622	0.6299	0.6378
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3		12.00			0.4724	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
k	0°	3.5°	7°	0.0°	3.5°	7.0°
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline<sup>(1)</sup>

Figure 39. Recommended footprint<sup>(1)(2)</sup>



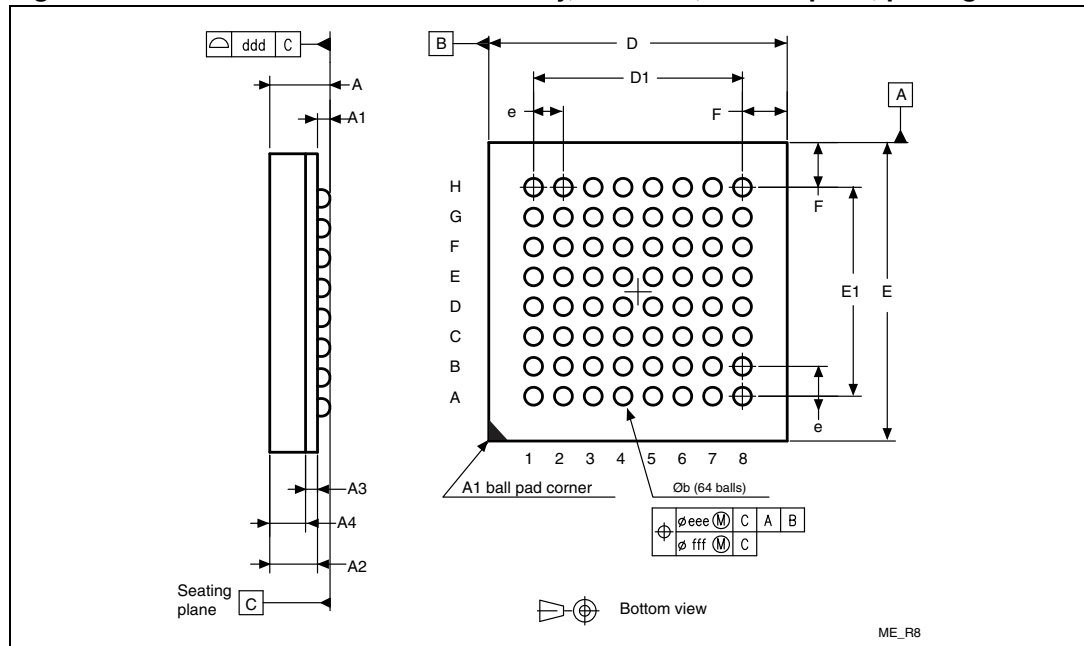
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 48. LQFP64 – 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
<b>Number of pins</b>						
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package outline



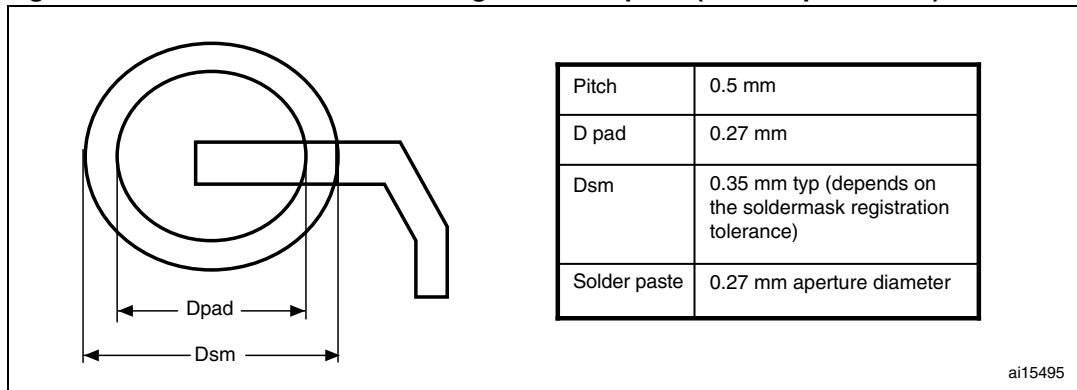
1. Drawing is not to scale.

Table 49. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A			1.200			0.0472
A1	0.150			0.0059		
A2		0.785			0.0309	
A3		0.200			0.0079	
A4			0.600			0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1		3.500			0.1378	
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1		3.500			0.1378	
e		0.500			0.0197	
F		0.750			0.0295	
ddd		0.080			0.0031	
eee		0.150			0.0059	
fff		0.050			0.0020	

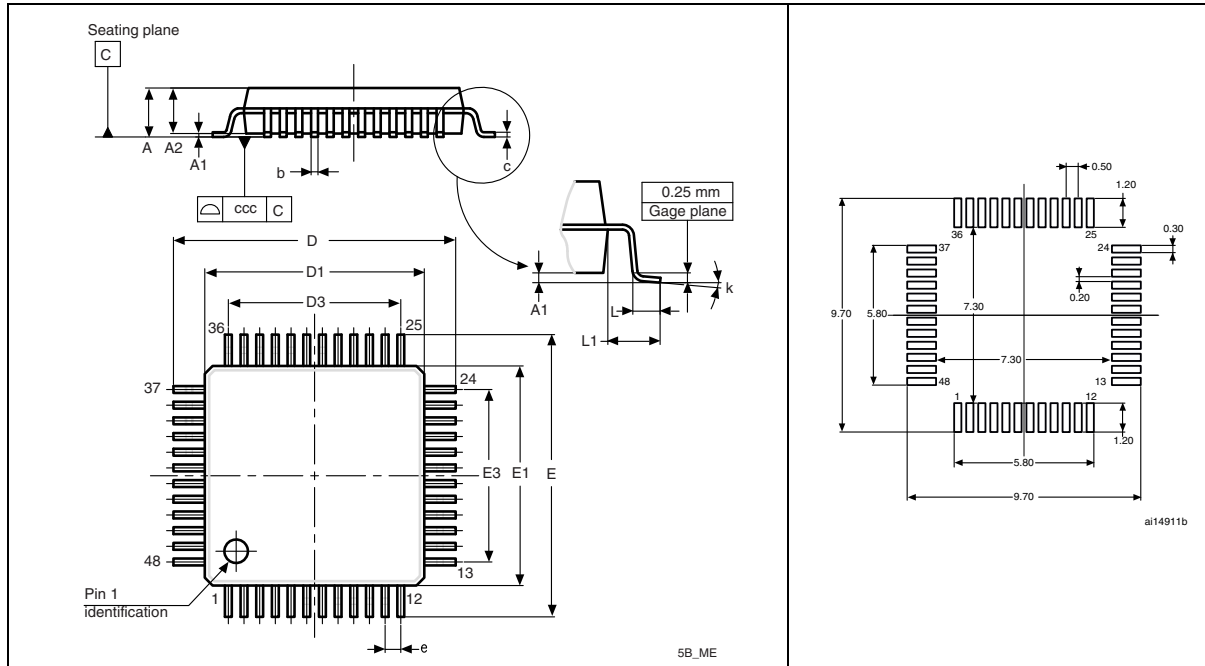
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. Recommended PCB design rules for pads (0.5 mm pitch BGA)



1. Non solder mask defined (NSMD) pads are recommended
2. 4 to 6 mils solder paste screen printing process

Figure 42. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline<sup>(1)</sup>      Figure 43. Recommended footprint<sup>(1)(2)</sup>



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 50. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 6.2 Thermal characteristics

The maximum chip junction temperature ( $T_{Jmax}$ ) must never exceed the values given in [Table 8: General operating conditions on page 34](#).

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D$  max =  $P_{INT}$  max +  $P_{I/O}$  max),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 51. Package thermal characteristics**

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	Thermal resistance junction-ambient LQFP 100 - 14 × 14 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient TFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP 48 - 7 × 7 mm / 0.5 mm pitch	55	

### 6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org).

## 6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 52: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F10xxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 82\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 8 I/Os used at the same time in output mode at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 272\text{ mW}$

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Thus:  $P_{Dmax} = 447\text{ mW}$

Using the values obtained in [Table 51](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64,  $45\text{ °C/W}$

$$T_{Jmax} = 82\text{ °C} + (45\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.1\text{ °C} = 102.1\text{ °C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 52: Ordering information scheme](#)).

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature  $T_J$  remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 115\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 20\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives:  $P_{INTmax} = 70\text{ mW}$  and  $P_{IOmax} = 64\text{ mW}$ :

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus:  $P_{Dmax} = 134\text{ mW}$



Using the values obtained in [Table 51](#)  $T_{Jmax}$  is calculated as follows:

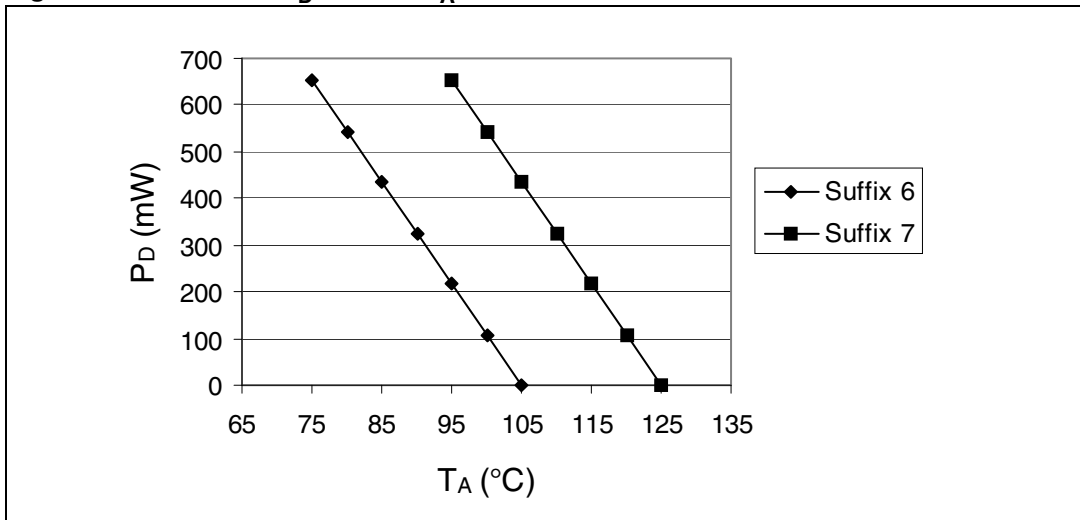
– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ( $-40 < T_J < 125\text{ °C}$ ).

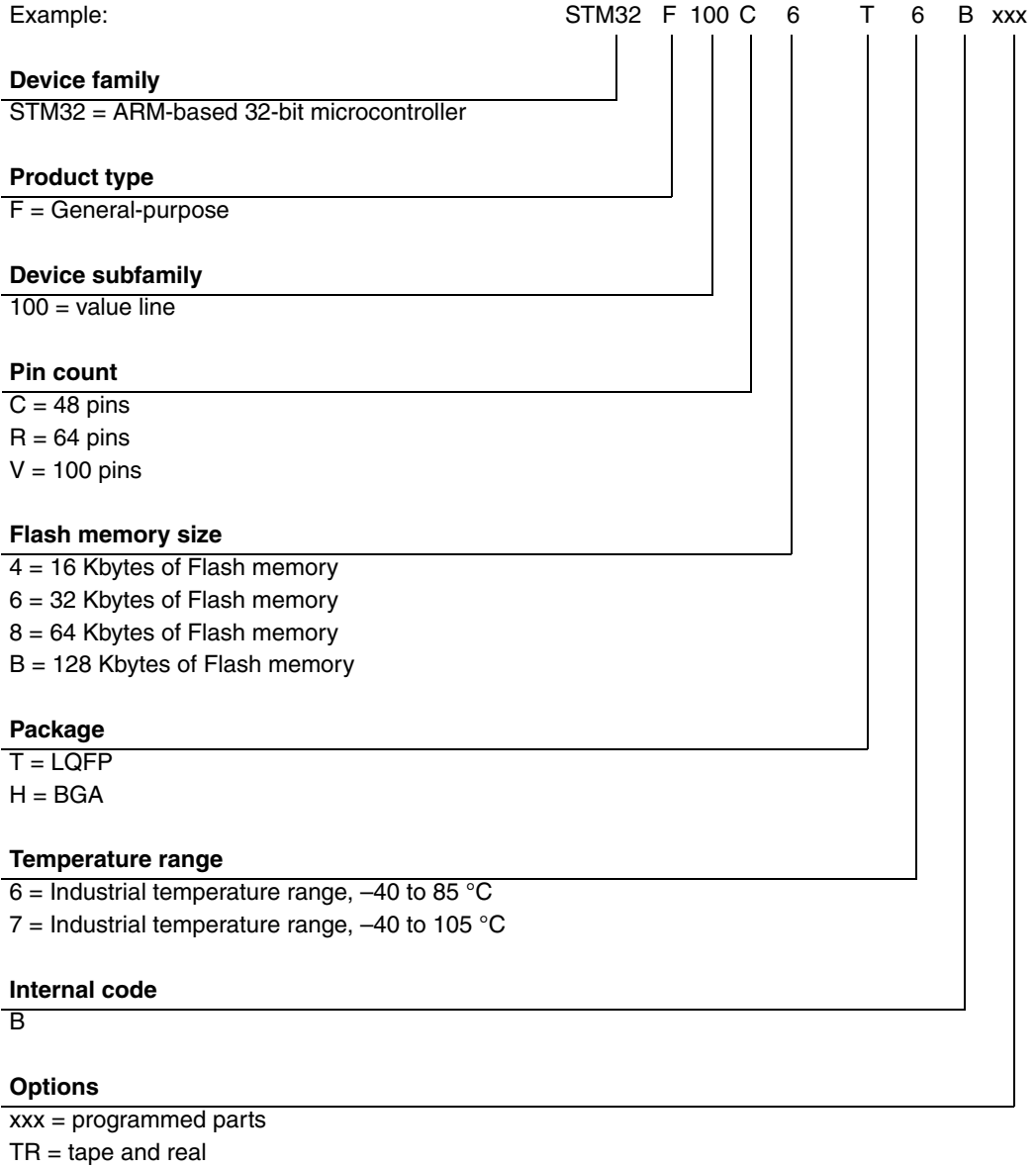
In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 52: Ordering information scheme](#)).

**Figure 44. LQFP100  $P_D$  max vs.  $T_A$**



# 7 Ordering information scheme

**Table 52. Ordering information scheme**



For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

## 8 Revision history

**Table 53. Document revision history**

Date	Revision	Changes
12-Oct-2009	1	Initial release.
19-Jan-2010	2	<p>TFBGA64 package added (see <a href="#">Table 49</a> and <a href="#">Table 40</a>).</p> <p><a href="#">Note 5</a> modified in <a href="#">Table 4: STM32F100xx pin definitions</a>.</p> <p><math>I_{INJ(PIN)}</math> modified in <a href="#">Table 6: Current characteristics</a>. Conditions removed from <a href="#">Table 25: Low-power mode wakeup timings</a>.</p> <p>Notes modified in <a href="#">Table 33: I/O static characteristics</a>.</p> <p><a href="#">Figure 26: Recommended NRST pin protection</a> modified.</p> <p>Note modified in <a href="#">Table 38: I2C characteristics</a>. <a href="#">Figure 27: I2C bus AC waveforms and measurement circuit(1)</a> modified.</p> <p><a href="#">Table 45: DAC characteristics</a> modified. <a href="#">Figure 35: 12-bit buffered /non-buffered DAC</a> added.</p>
26-Feb-2010	3	<p><a href="#">TIM2</a>, <a href="#">TIM3</a>, <a href="#">TIM4</a> and <a href="#">TIM15</a>, <a href="#">TIM16</a> and <a href="#">TIM17</a> updated.</p> <p>HDMI-CEC electrical characteristics added.</p> <p>Values added to:</p> <ul style="list-style-type: none"> <li>– <a href="#">Table 12: Maximum current consumption in Run mode, code with data processing running from Flash</a></li> <li>– <a href="#">Table 13: Maximum current consumption in Run mode, code with data processing running from RAM</a></li> <li>– <a href="#">Table 14: STM32F100xB maximum current consumption in Sleep mode, code running from Flash or RAM</a></li> <li>– <a href="#">Table 15: Typical and maximum current consumptions in Stop and Standby modes</a></li> <li>– <a href="#">Table 18: Peripheral current consumption</a></li> <li>– <a href="#">Table 29: EMS characteristics</a></li> <li>– <a href="#">Table 30: EMI characteristics</a></li> <li>– <a href="#">Table 46: TS characteristics</a></li> </ul> <p><a href="#">Section 5.3.12: I/O port characteristics</a> modified.</p> <p>Added figures:</p> <ul style="list-style-type: none"> <li>– <a href="#">Figure 12: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled</a></li> <li>– <a href="#">Figure 13: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled</a></li> <li>– <a href="#">Figure 14: Typical current consumption in Stop mode with regulator in Run mode versus temperature at VDD = 3.3 V and 3.6 V</a></li> <li>– <a href="#">Figure 15: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V</a></li> <li>– <a href="#">Figure 16: Typical current consumption in Standby mode versus temperature at VDD = 3.3 V and 3.6 V</a></li> </ul>

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