

| STRUCTURE | Silicon Monolithic Integrated Circuit |
|-----------------|---------------------------------------|
| NAME OF PRODUCT | DC-AC Inverter Control IC |
| TYPE | BD9897FS |

FUNCTION

36V High voltage process

• 1ch control with Full-Bridge

- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Mode-selectable the operating or stand-by mode by stand-by pin
- Synchronous operating the other BD9897FS IC's
- BURST mode controlled by PWM and DC input
- Output liner Control by external DC voltage

OAbsolute Maximum Ratings (Ta = 25° C)

| Parameter | Symbol | Limits | Unit |
|------------------------------|--------|----------|------|
| Supply Voltage | Vcc | 36 | ۷ |
| BST pin | BST | 40 | ٧ |
| SW pin | SW | 36 | ٧ |
| BST-SW voltage difference | BST-SW | 7 | ٧ |
| Operating Temperature Range | Topr | -40~+85 | °C |
| Storage Temperature Range | Tstg | -55~+150 | °C |
| Maximum Junction Temperature | Tjmax | +150 | °C |
| Power Dissipation | Pd | 950* | mW |

*Pd derate at 7.6mW/°C for temperature above Ta = 25° C (When mounted on a PCB 70.0mm × 70.0mm × 1.6mm) OOperating condition

| Parameter | Symbol | Limits | Unit |
|---------------------------|--------|------------|------|
| Supply voltage | Vcc | 7.5~30.0 | V |
| BST voltage | BST | 4. 0~36. 0 | V |
| BST-SW voltage difference | BST-SW | 4.0~6.5 | V |
| CT oscillation frequency | fct | 60~180 | kHz |
| BCT oscillation frequency | fBCT | 0.05~1.00 | kHz |

Status of this document

The Japanese version of this document is the official specification.

Please use the translation version of this document as a reference to expedite understanding of the official version.

If these are any uncertainty in translation version of this document, official version takes priority.



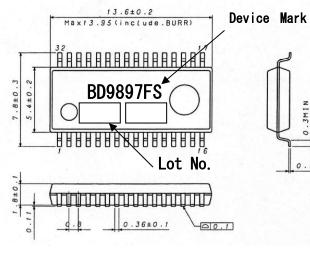
O Electric Characteristics (Ta=25°C, VCC=24V)

| Parameter | | | Limits | | | |
|---------------------------------------------------------------------------------|-----------------------|------------------|-----------------|------------------|------------|--------------------------------------|
| | Symbol | MIN. | TYP. | MAX. | Unit | Conditions |
| ((WHOLE DEVICE)) | | | | | | |
| Operating current | lcc1 | - | 7.2 | 13 | mA | $CT_SYNC_IN = OPEN$ |
| Stand-by current | lcc2 | - | 13.0 | 30.0 | μA | |
| ((STAND BY CONTROL)) | | • | | | | • |
| Stand-by voltage H | VstH | 2.0 | - | VCC | ٧ | System ON |
| Stand-by voltage L | VstL | -0.3 | - | 0.8 | V | System OFF |
| ((UVLO BLOCK))) | | 1 | | | | - |
| Operating voltage (VCC) | VuvloH | 5.7 | 6.0 | 6.3 | ٧ | |
| Hesteresis width (VCC) | ⊿VCC_Vuvlo | 0.26 | 0.35 | 0. 43 | ٧ | |
| Operating voltage (UVLO) | Vuvlo2 | 2. 179 | 2. 25 | 2. 321 | ۷ | - |
| Hesteresis width (UVLO) | ⊿Vuvlo | 0. 074 | 0. 098 | 0. 122 | ۷ | |
| ((REG BLOCK)) | | 5.00 | 5.00 | 5.00 | | 1000 Z 011 |
| REG output voltage | VREG | 5. 68 20. 0 | 5.80 — | 5.92 | V | VCC>7. OV |
| REG source current ((OSC BLOCK)) | IREG | 20.0 | - | — | mA | |
| Active edge setting current | lact | 1.35/(RT*7) | 1.5/(RT*6) | 1.65/(RT*5) | A | |
| Negative edge setting current | Ineg | lact × 29 | lact × 35 | lact × 41 | A | |
| OSC Max voltage | VOSCH | 1.8 | 2.0 | 2.2 | V | fCT=120kHz |
| OSC Min voltage | VOSCL | 0, 35 | 0, 45 | 0, 60 | V | fCT=120kHz |
| Soft start current | 188 | 0.6 | 1.1 | 1.6 | μA | = |
| SRT ON resistance | RSRT | - | 1.1 | 200 | Ω | |
| ((BOSC BLOCK)) | | | | | | 1 |
| BOSC Max voltage | VBCTH | 1, 94 | 2.00 | 2.06 | V | fBCT=0. 3kHz |
| ő | | | | | - | - |
| BOSC Min voltage | VBCTL | 0.40 | 0.50 | 0.60 | V | fBCT=0. 3kHz |
| BOSC constant current | IBCT | 1.35/BRT | 1.5/RT | 1.65/RT | A | VBCT=0. 2V |
| BOSC frequency | fBCT | 291 | 300 | 309 | Hz | (BRT=33k Ω BCT=0.048 μ F) |
| ((FEED BACK BLOCK)) | | | | | | - |
| IS threshold voltage 1 | VISO | 1. 225 | 1.250 | 1.275 | ٧ | |
| IS threshold voltage 2 | VIS(2) | _ | VREFIN | VIST | ٧ | VREF applying voltage |
| - | VVS | 1. 220 | 1. 250 | 1. 280 | v | |
| VS threshold voltage | | - | - | 0.9 | - | |
| IS source current 1 IS source current 2 | \$1 | 32 | 50 | 68 | μ Α μ Α | DUTY=2. 2V DUTY=0V IS=0. 5V |
| VS source current | 1132 | 32 | 50 | 0.9 | μ κ μ Α | DUTT-0V 13-0.5V |
| IS COMP detect voltage ① | VISCOMP(1) | 0, 90 | 0, 94 | 0.98 | V | VREFIN≧1.25V |
| IS COMP detect voltage 2 | VISCOMP(2) | - | VREFIN×0.73 | _ | v | VREFIN<1.25V |
| VREF input voltage range | VREFIN | 0.6 | - | 1.6 | ٧ | No effect at VREF>1.25V |
| ((DUTY BLOCK)) | | | | | | |
| High voltage | VDUTY-OUTH | 2.8 | 3.1 | 3.4 | ٧ | |
| Low voltage | VDUTY-OUTL | - | - | 0.5 | ٧ | |
| DUTY-OUT sink resistance | RDUTY-OUTSink | - | 150 | 300 | Ω | |
| DUTY-OUT source resistance | RDUTY-OUTSouce | - | 250 | 500 | Ω | |
| ((OUTPUT BLOCK)) | De Ludd N | 0.75 | 1.5 | 2.0 | Ω | |
| LN output sink resistance LN output source resistance | RsinkLN RsourceLN | 0.75 2.5 | 1.5 5 | 3. 0 10 | Ω | |
| HN output sink resistance | RsinkHN | 2.5 | 2.5 | 5.0 | Ω | VBST-VSW=5. OV |
| HN output sink resistance | RsourceLN | 2.5 | 2.5 | 10 | Ω | VBST-VSW=5. 0V |
| MAX DUTY | MAX DUTY | 46.0 | 48.0 | 49.5 | % | FOUT=60kHz |
| OFF period | TOFF | 100 | 200 | 400 | ns | |
| Drive output frequency | FOUT | 58.5 | 60.0 | 61.5 | kHz | (RT=4. 7kΩ CT=235pF) |
| ((TIMER LATCH BLOCK)) | | | | | | |
| Timer Latch setting voltage | VCP | 1.94 | 2.0 | 2.06 | V | |
| Timer Latch setting current | ICP | 0.40 | 0.55 | 0. 70 | μA | |
| ((COMP CLOCK)) | MOCHEN | 0.100 | 0.405 | 0.510 | ., | 1000 0 0V |
| COMP1 over voltage detect voltage | VCOMPH VCOMP2 H | 2.460 | 2. 485 | 2.510 | V V | VSS>2.2V |
| COMP2 over voltage detect voltage COMP2 under voltage detect voltage ① | VCOMP2_H VCOMP_L_1 | 2. 460 1. 225 | 2. 485 1. 25 | 2. 510 1. 275 | V | VSS>2. 2V VSS>2. 2V |
| COMP2 under voltage detect voltage () COMP2 under voltage detect voltage (2) | VCOMP_L_1 | 0. 606 | 0. 625 | 0. 644 | V | VSS<2. 2V VSS<2. 2V |
| ((Synchronous Block)) | 100mr_L_2 | 0.000 | 0.020 | 0. 777 | ¥ | 100 12.21 |
| High voltage | VCT_SYNCH | 2.8 | 3.1 | 3.4 | ٧ | |
| Low voltage | VCT_SYNCL | - | | 0.5 | ٧ | 1 |
| CT_SYNC sink resistance | RCT_SYNC_SYNC | - | 150 | 300 | Ω | |
| CT_SYNC source resistance | RCT_SYNC_SOURCE | - 1 | 370 | 740 | Ω | 1 |
| | VCT_SYNC_IN_H | 2.0 | - | 3. 3 | V | |
| High voltage input range | | 2.0 | _ | 3. 5 | v | |

(This product is not designed to be radiation-resistant.)

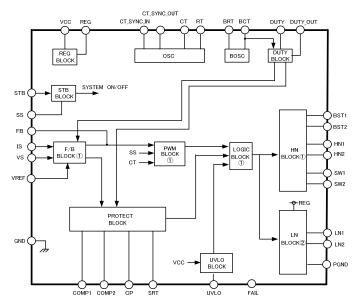


OPackage Dimensions



SSOP-A32 (Unit:mm)

OBlock Diagram



| PI No | | FUNCTION | | | | |
|----------|-------------|--------------------------------------------------------------------------------|--|--|--|--|
| 1 | PGND | Ground for FET drivers | | | | |
| 2 | LN2 | NMOS FET driver | | | | |
| 3 | HN2 | NMOS FET driver | | | | |
| 4 | SW2 | Lower rail voltage for $HN2$ output | | | | |
| 5 | BST2 | Boot-Strap input for HN2 output | | | | |
| 6 | CT_SYNC_IN | CT synchronous signal input pin | | | | |
| 7 | CT_SYNC_OUT | CT synchronous signal output pin | | | | |
| 8 | SRT | External resistor from SRT to RT for adjusting the triangle oscillator | | | | |
| 9 | RT | External resistor from SRT to RT for adjusting the triangle oscillator | | | | |
| 10 |) CT | External capacitor from CT to GND for adjusting the triangle oscillator | | | | |
| 11 | GND | GROUND | | | | |
| 12 | 2 BCT | External capacitor from BCT to GND for adjusting the BURST triangle oscillator | | | | |
| 13 | BRT | External resistor from BRT to GND for adjusting the BURST triangle oscillator | | | | |
| 14 | 4 DUTY | Control PWM mode and BURST mode | | | | |
| 15 | 5 DUTY_OUT | BURST signal output pin | | | | |
| 16 | 6 STB | Stand-by switch | | | | |
| 17 | 7 CP | External capacitor from CP to GND for Timer Latch | | | | |
| 18 | B FAIL | COMP2 under voltage protect clock output | | | | |
| 19 |) VREF | Reference voltage input pin for Error amplifier | | | | |
| 20 | VS VS | Error amplifier input | | | | |
| 21 | IS | Error amplifier input | | | | |
| 22 | 2 FB | Error amplifier output | | | | |
| 23 | 3 SS | External capacitor from SS to GND for Soft Start Control | | | | |
| 24 | COMP2 | Under, over voltage detect pin | | | | |
| 25 | 5 COMP1 | Over voltage detect pin | | | | |
| 26 | 6 VCC | Supply voltage input | | | | |
| 27 | 7 UVLO | External Under Voltage Lock Out | | | | |
| 28 | B REG | Internal regulator output | | | | |
| 29 |) BST1 | Boot-Strap input for HN1 output | | | | |
| 30 |) SW1 | Lower rail voltage for HN1 output | | | | |
| 31 | HN1 | NMOS FET driver | | | | |
| 32 | 2 LN1 | NMOS FET driver | | | | |

0.3MIN

0.15±0.1



ONOTE FOR USE

- When designing the external circuit, including adequate margins for variation between external devices and IC. Use adequate margins for steady state and transient characteristics.
- 2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
- 3. Mounting failures, such as misdirection or miscounts, may harm the device.
- 4. A strong electromagnetic field may cause the IC to malfunction.
- 5. The GND pin should be the location within $\pm 0.3V$ compared with the PGND pin.
- 6. BD9897FS incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
- 7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
- 8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
- 9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
- 1 O. By STB voltage, BD9897FS are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8~2.0V).
- 1 1. The pin connected a connector need to connect to the resistor for electrical surge destruction. This IC is a monolithic IC which (as shown is Fig-1) has P⁺ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

O(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

O(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

1 2. This IC is a monolithic IC which (as shown is Fig-1)has P⁺ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

O (When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

O(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

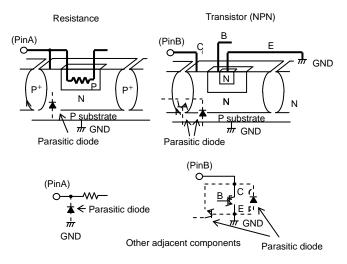


Fig-1 Simplified structure of a Bipolar IC

| | Notes |
|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | g or reproduction of this document, in part or in whole, is permitted without the ROHM Co.,Ltd. |
| The conten | t specified herein is subject to change for improvement without notice. |
| "Products") | It specified herein is for the purpose of introducing ROHM's products (hereinafte b. If you wish to use any such Product, please be sure to refer to the specifications be obtained from ROHM upon request. |
| illustrate th | of application circuits, circuit constants and any other information contained herein e standard usage and operations of the Products. The peripheral conditions mus to account when designing circuits for mass production. |
| However, s | was taken in ensuring the accuracy of the information specified in this document should you incur any damage arising from any inaccuracy or misprint of such , ROHM shall bear no responsibility for such damage. |
| examples of implicitly, a other partie | cal information specified herein is intended only to show the typical functions of and of application circuits for the Products. ROHM does not grant you, explicitly o ny license to use or exercise intellectual property or other rights held by ROHM and es. ROHM shall bear no responsibility whatsoever for any dispute arising from the technical information. |
| equipment | ets specified in this document are intended to be used with general-use electronic or devices (such as audio visual equipment, office-automation equipment, commu vices, electronic appliances and amusement devices). |
| The Produc | ts specified in this document are not designed to be radiation tolerant. |
| | M always makes efforts to enhance the quality and reliability of its Products, a ay fail or malfunction for a variety of reasons. |
| against the failure of ar shall bear r | sure to implement in your equipment using the Products safety measures to guard possibility of physical injury, fire or any other damage caused in the event of the product, such as derating, redundancy, fire control and fail-safe designs. ROHM responsibility whatsoever for your use of any Product outside of the prescribed of in accordance with the instruction manual. |
| system whi may result instrument fuel-contro any of the F | cts are not designed or manufactured to be used with any equipment, device or ch requires an extremely high level of reliability the failure or malfunction of which in a direct threat to human life or create a risk of human injury (such as a medica , transportation equipment, aerospace machinery, nuclear-reactor controller ller or other safety device). ROHM shall bear no responsibility in any way for use of Products for the above special purposes. If a Product is intended to be used for any al purpose, please contact a ROHM sales representative before purchasing. |
| be controlle | d to export or ship overseas any Product or technology specified herein that may ed under the Foreign Exchange and the Foreign Trade Law, you will be required to ense or permit under the Law. |



Thank you for your accessing to ROHM product informations. More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/