



AK4113

192kHz 24bit DIR with 6:1 Selector

GENERAL DESCRIPTION

The AK4113 is a 24-bit stereo digital audio receiver that supports sampling rates up to 216kHz. The channel status bits decoder supports both consumer and professional modes. The AK4113 automatically detects non-PCM bit streams such as Dolby Digital, MPEG etc. When combined with the multi channel codec (AK4626 or AK4628), the two chips provide a system solution for Dolby Digital applications. Control of AK4113 is achieved through a μ P or pin strapping (parallel mode). It is packaged in a space-saving 30-pin VSOP.

* Dolby Digital is a trademark of Dolby Laboratories.

FEATURES

- AES/EBU, IEC60958, S/PDIF, EIAJ CP1201 Compatible
- Low Jitter Analog PLL
- PLL Lock Range: 8k ~ 216kHz
- Clock source: PLL or X'tal
- 6-channel Receiver Input and 1-channel Transmission Output (Through output)
- Auxiliary Digital Input
- De-emphasis for 32kHz, 44.1kHz and 48kHz
- Detection Functions
 - Non-PCM Bit Stream Detection
 - DTS-CD Bit Stream Detection
 - Sampling Frequency Detection
(8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz)
 - Unlock & Parity Error Detection
 - Validity Detection
 - DAT Start ID Detection
- Up to 24bit Audio Data Format
- Audio Interface: Master or Slave Mode
- 40-bit Channel Status Buffer
- Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream
- Q-subcode Buffer for CD bit stream
- Serial μ P Interface: I²C (max. 400kHz) or 4-wire
- Two Master Clock Outputs: 64fs/128fs/256fs/512fs
- Operating Voltage: 2.7 to 3.6V with 5V Logic Tolerance
- Small Package: 30pin VSOP
- Ta: - 40 ~ 85°C

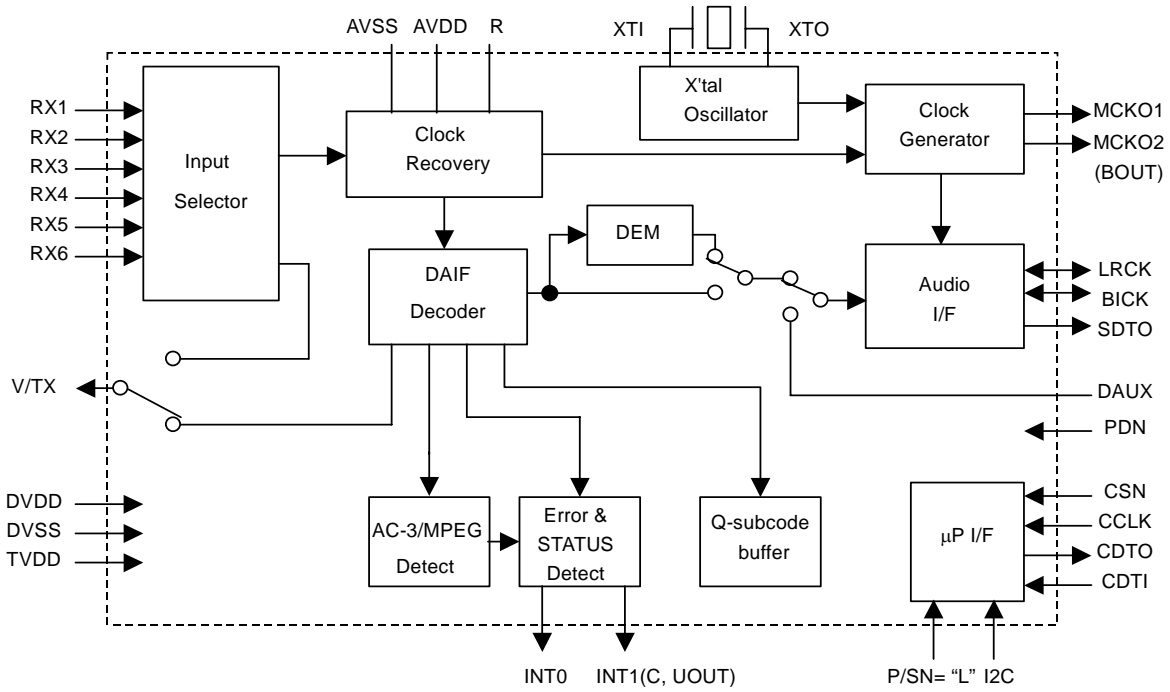


Figure 1. Serial control mode

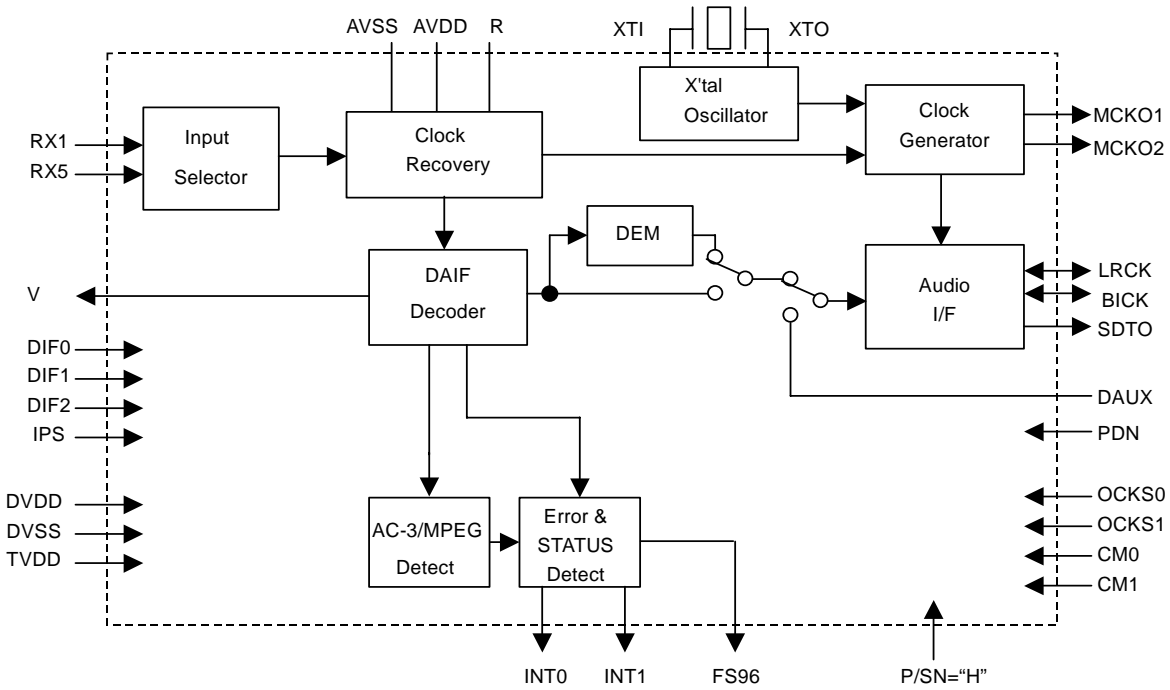
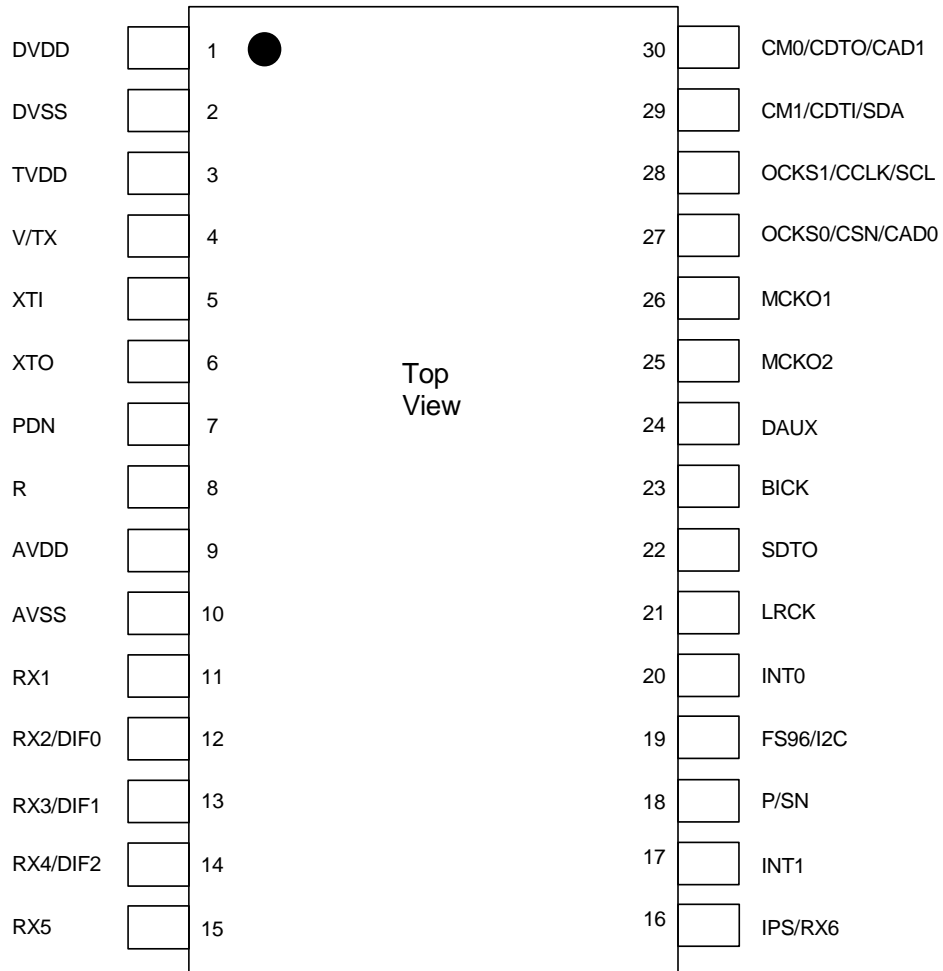


Figure 2. Parallel control mode

■ Ordering Guide

AK4113VF -40 ~ +85 °C 30pin VSOP (0.65mm pitch)
 AKD4113 Evaluation board for AK4113

■ PIN Layout



| PIN/FUNCTION | | | |
|--------------|----------|-----|--|
| No. | Pin Name | I/O | Function |
| 1 | DVDD | - | Digital Power Supply Pin, 3.3V |
| 2 | DVSS | - | Digital Ground Pin |
| 3 | TVDD | - | Input Buffer Power Supply Pin, 3.3V or 5V |
| 4 | V | O | Validity Flag Output Pin in Parallel control mode |
| | TX | O | Transmit channel (Through data) Output Pin in serial control mode |
| 5 | XTI | I | X'tal Input Pin |
| 6 | XTO | O | X'tal Output Pin |
| 7 | PDN | I | Power-Down Mode Pin When "L", the AK4113 is powered-down and reset. |
| 8 | R | - | External Resistor Pin This pin must be connected to AVSS via 15kΩ ±5% resistor. |
| 9 | AVDD | - | Analog Power Supply Pin |
| 10 | AVSS | - | Analog Ground Pin |
| 11 | RX1 | I | Receiver Channel #1 Pin (Internal Biased Pin) |
| 12 | DIF0 | I | Audio Data Interface Format #0 Pin in parallel control mode |
| | RX2 | I | Receiver Channel #2 Pin in serial control mode (Internal Biased Pin) |
| 13 | DIF1 | I | Audio Data Interface Format #1 Pin in parallel control mode |
| | RX3 | I | Receiver Channel #3 Pin in serial control mode (Internal Biased Pin) |
| 14 | DIF2 | I | Audio Data Interface Format #2 Pin in parallel control mode |
| | RX4 | I | Receiver Channel #4 Pin in serial control mode (Internal Biased Pin) |
| 15 | RX5 | I | Receiver Channel #5 Pin (Internal Biased Pin) |
| 16 | IPS | I | Input Channel Select Pin in parallel control mode |
| | RX6 | I | Receiver Channel #6 Pin (Internal Biased Pin) |
| 17 | INT1 | O | Interrupt #1 Pin (when BCU bit = "0") |
| | | | U-bit Output Pin (when BCU bit = "1", UCE bit = "0") |
| | | | C-bit Output Pin (when BCU bit = "1", UCE bit = "1") |
| 18 | P/SN | I | Parallel/Serial Select Pin "L": Serial control mode, "H": Parallel control mode |
| 19 | FS96 | O | 96kHz Sampling Detect Pin in parallel control mode This function is enabled when the input frequency of XTI is 24.576MHz. "L": fs=54kHz or less, "H": fs=64kHz or more |
| | I2C | I | I ² C Select Pin in Serial control mode. "L": 4-wire Serial, "H": I ² C |
| 20 | INT0 | I | Interrupt #0 Pin |
| 21 | LRCK | I/O | Output Channel Clock Pin |
| 22 | SDTO | O | Audio Serial Data Output Pin |
| 23 | BICK | I/O | Audio Serial Data Clock Pin |
| 24 | DAUX | I | Auxiliary Audio Data Input Pin |
| 25 | MCKO2 | O | Master Clock #2 Output Pin (when BCU bit = "0") |
| | | | Block Start Signal Output Pin (when BCU bit = "1") |
| 26 | MCKO1 | O | Master Clock #1 Output Pin |
| 27 | OCKS0 | I | Output Clock Select #0 Pin in parallel control mode |
| | CSN | I | Chip Select Pin in serial control mode, I2C pin = "L" |
| | CAD0 | I | Chip Address #0 Pin in serial control mode, I2C pin = "H" |

Note 1. Do not allow digital input pins except internal biased pins (RX1-6 pins) to float.

| No. | Pin Name | I/O | Function |
|-----|----------|-----|--|
| 28 | OCKS1 | I | Output Clock Select #1 Pin in parallel control mode |
| | CCLK | I | Control Data Clock Pin in serial control mode, I2C pin = "L" |
| | SCL | I | Control Data Clock Pin in serial control mode, I2C pin = "H" |
| 29 | CM1 | I | Master Clock Operation Mode #1 Pin in parallel control mode |
| | CDTI | I | Control Data Input Pin in serial control mode, I2C pin = "L" |
| | SDA | I/O | Control Data Pin in serial control mode, I2C pin = "H" |
| 30 | CM0 | I | Master Clock Operation Mode #0 Pin in parallel control mode |
| | CDTO | O | Control Data Output Pin in serial control mode |
| | CAD1 | I | Chip Address #1 Pin in serial control mode, I2C pin = "H" |

Note 1. Do not allow digital input pins except internal biased pins (RX1-6 pins) to float.

■ Handling of Unused Pin

The unused I/O pin should be processed appropriately as below.

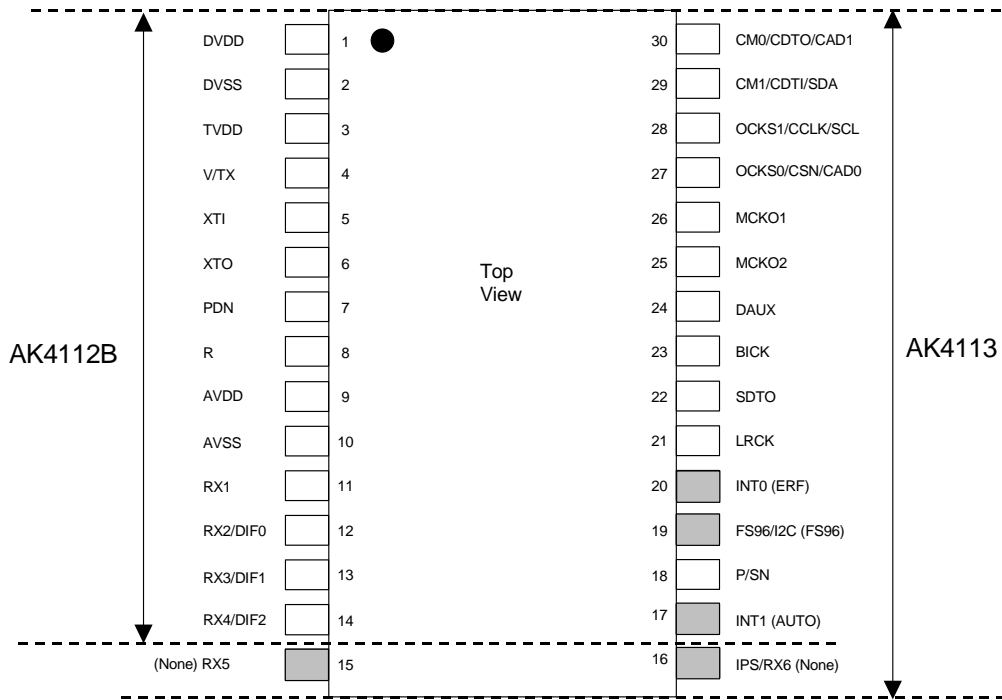
| Classification | Pin Name | Setting |
|----------------|---|---|
| Analog Input | RX1, RX2/DIF0, RX3/DIF1, RX4/DIF2, RX5, RX6/IPS | These pins should be open in serial control mode. |
| | RX1, RX5 | These pins should be open in parallel control mode. |
| Digital Input | DAUX, XTI | These pins should be connected to DVSS. |
| Digital Output | V/TX, XTO, INT0, INT1, MCKO1, MCKO2 | These pins should be open. |
| | I2C/FS96 | This pin should be open in parallel control mode. |
| | CAD1/CDTO/CM0 | This pin should be open in serial control mode and 4-wire mode (I2C pin = "L"). |

■ Compare AK4112B with AK4113

1. Function

| Function | | AK4112B | AK4113 |
|---|-----------------------|----------------------------|--|
| RX Input Channel | Serial control mode | 4ch | 6ch |
| | Parallel control mode | 1ch | 2ch |
| PLL Lock Range | | 22kHz to 108kHz | 8kHz to 216kHz |
| Resistor value for R pin | | 18k ± 1% | 15k ± 5% |
| PLL Lock Time | | ≤ 20ms | FAST bit = "0": ≤ (15ms+384/fs) FAST bit = "1": ≤ (15ms+1/fs) |
| DTS-CD Bit Stream Detection | | Not available | Available |
| DAT Start ID Detection | | Not available | Available |
| Q-subcode Buffer for CD bit Stream | | Not available | Available |
| fs Detection in serial control mode | | ≤ 54kHz ≥or ≥88.2kHz | 8k / 11.025k / 16k / 22.05k / 24k/ 32k / 44.1k / 48k / 64k / 88.2k / 96k / 176.4k / 192kHz |
| Serial μP Interface | | 4-wire | 4-wire/I ² C (max.400kHz) |
| Error Handling Pins | | AUTO, ERF, FS96 | INT0, INT1 |
| Master Clock Output Frequency | | 128fs/256fs/512fs | 64fs/128fs/256fs/512fs |
| Channel Status Bit | | 32bit | 40bit |
| MCKO2 Clock Source in serial control mode | | Depend on CM1-0 bits | Depend on CM1-0, XMCK and BCU bits |
| Audio I/F at Reset in serial control mode | | Master Mode | Slave Mode |
| Package | | 28pin VSOP | 30pin VSOP |

2. Pin Layout



Note:

- 1) Light gray highlights indicate the difference between AK4112B and AK4113.
- 2) The inside of “()” indicates the pin name of AK4112B.

3. Control register

Control registers of between AK4112B and AK4113 are not compatible.

ABSOLUTE MAXIMUM RATING

(AVSS, DVSS=0V; Note 2)

| Parameter | | Symbol | min | max | Units |
|--|---------------------|--------------|------|----------|-------|
| Power Supplies: | Analog | AVDD | -0.3 | 4.6 | V |
| | Digital | DVDD | -0.3 | 4.6 | V |
| | Input Buffer | TVDD | -0.3 | 6.0 | V |
| | AVSS-DVSS (Note 3) | Δ GND | | 0.3 | V |
| Input Current (Any pins except supplies) | | IIN | - | \pm 10 | mA |
| Input Voltage | | VIN | -0.3 | TVDD+0.3 | V |
| Ambient Temperature (Power applied) | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note 2. All voltage with respect to ground.

Note 3. AVSS and DVSS must be connected to the same ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device

Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 2)

| Parameter | | Symbol | min | typ | max | Units |
|-----------------|--------------|-------------|------|-----|-----|-------|
| Power Supplies: | Analog | AVDD | 2.7 | 3.3 | 3.6 | V |
| | Digital | DVDD | 2.7 | 3.3 | 3.6 | V |
| | Input Buffer | TVDD | DVDD | 3.3 | 5.5 | V |
| | Difference | AVDD - DVDD | -0.3 | 0 | 0.3 | V |
| | | | | | | |

Note 2. All voltage with respect to ground

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V;TVDD=2.7~5.5V)

| Parameter | Symbol | min | typ | max | Units |
|------------------------|--------|-----|-----|-----|------------|
| Input Resistance | Zin | | 10 | | k Ω |
| Input Voltage | VTH | 350 | | | mVpp |
| Input Hysteresis | VHY | - | 185 | | mV |
| Input Sample Frequency | fs | 8 | - | 216 | kHz |

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V;TVDD=2.7~5.5V; unless otherwise specified)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|------------|-----|----------|-------|
| Power Supply Current | | | | | |
| Normal operation: PDN pin = "H" (Note 4) | | | 26 | 42 | mA |
| Power down: PDN pin = "L" (Note 5) | | | 10 | 100 | μA |
| High-Level Input Voltage | VIH | 70% DVDD | - | TVDD | V |
| Low-Level Input Voltage | VIL | DVSS - 0.3 | - | 30% DVDD | V |
| High-Level Output Voltage (Except TX pin: Iout=400μA) | VOH | DVDD-0.4 | - | - | V |
| Low-Level Output Voltage (Except TX and SDA pins: Iout=400μA) | VOL | - | - | 0.4 | V |
| (SDA pin: Iout= 3mA) | VOL | - | - | 0.4 | V |
| TX Output Level (Note 6) | VTXO | 0.4 | 0.5 | 0.6 | V |
| Input Leakage Current (Except RX1-6, XTI pins) | Iin | - | - | ± 10 | μA |

Note 4. AVDD, DVDD=3.3V, TVDD=5.0V, CL=20pF, fs=216kHz, X'tal=24.576MHz, Clock Operation Mode 2, OCKS1 bit = "1", OCKS0 bit = "1". TX circuit = Figure 19, Master Mode; AVDD=5mA (typ), DVDD=21mA (typ), TVDD=0.1μA (typ).

Note 5. RX inputs are open and all digital input pins are held DVDD or DVSS.

Note 6. By using Figure 19

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V, TVDD=2.7~5.5V; CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|-------------------------------------|-----------|-------|---------|--------|-------|
| Master Clock Timing | | | | | |
| Crystal Resonator | Frequency | fXTAL | 11.2896 | 24.576 | MHz |
| External Clock | Frequency | fECLK | 11.2896 | 24.576 | MHz |
| | Duty | dECLK | 40 | 50 | % |
| MCKO1 Output | Frequency | fMCK1 | 1.024 | 27.648 | MHz |
| | Duty | dMCK1 | 40 | 50 | % |
| MCKO2 Output | Frequency | fMCK2 | 0.512 | 27.648 | MHz |
| | Duty | dMCK2 | 40 | 50 | % |
| PLL Clock Recover Frequency (RX1-6) | fpll | 8 | - | 216 | kHz |
| LRCK Frequency | fs | 8 | | 216 | kHz |
| Duty Cycle | dLCK | 45 | | 55 | % |
| Audio Interface Timing | | | | | |
| Slave Mode | | | | | |
| BICK Period | tBCK | 72 | | | ns |
| BICK Pulse Width Low | tBCKL | 27 | | | ns |
| Pulse Width High | tBCKH | 27 | | | ns |
| LRCK Edge to BICK "↑" | tLRB | 15 | | | ns |
| BICK "↑" to LRCK Edge | tBLR | 15 | | | ns |
| LRCK to SDTO (MSB) | tLRM | | | 20 | ns |
| BICK "↓" to SDTO | tBSD | | | 20 | ns |
| DAUX Hold Time | tDXH | 15 | | | ns |
| DAUX Setup Time | tDXS | 15 | | | ns |
| Master Mode | | | | | |
| BICK Frequency | fBCK | | 64fs | | Hz |
| BICK Duty | dBCK | | 50 | | % |
| BICK "↓" to LRCK | tMBLR | -15 | | 15 | ns |
| BICK "↓" to SDTO | tBSD | | | 15 | ns |
| DAUX Hold Time | tDXH | 15 | | | ns |
| DAUX Setup Time | tDXS | 15 | | | ns |

Note 7. BICK rising edge must not occur at the same time as LRCK edge.

SWITCHING CHARACTERISTICS (Continued)

(Ta=25°C; AVDD, DVDD=2.7~3.6V, TVDD=2.7~5.5V; CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|--|---------|-----|-----|-----|-------|
| Control Interface Timing (4-wire serial mode) | | | | | |
| CCLK Period | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDTI Setup Time | tCDS | 50 | | | ns |
| CDTI Hold Time | tCDH | 50 | | | ns |
| CSN "H" Time | tCSW | 150 | | | ns |
| CSN "↓" to CCLK "↑" | tCSS | 50 | | | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | | | ns |
| CDTO Delay | tDCD | | | 45 | ns |
| CSN "↑" to CDTO Hi-Z | tCCZ | | | 70 | ns |
| Control Interface Timing (I²C Bus mode): | | | | | |
| SCL Clock Frequency | fSCL | - | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | | - | μs |
| Clock Low Time | tLOW | 1.3 | | - | μs |
| Clock High Time | tHIGH | 0.6 | | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | - | μs |
| SDA Hold Time from SCL Falling (Note 8) | tHD:DAT | 0 | | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | - | μs |
| Capacitive load on bus | Cb | - | | 400 | pF |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | | 50 | ns |
| Reset Timing | | | | | |
| PDN Pulse Width | tPW | 150 | | | ns |

Note 8. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

Note 9. I²C is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd I²C components conveys a license under the Philips I²C patent to use the components in the I²C system, provided the system conform to the I²C specifications defined by Philips.

■ Timing Diagram

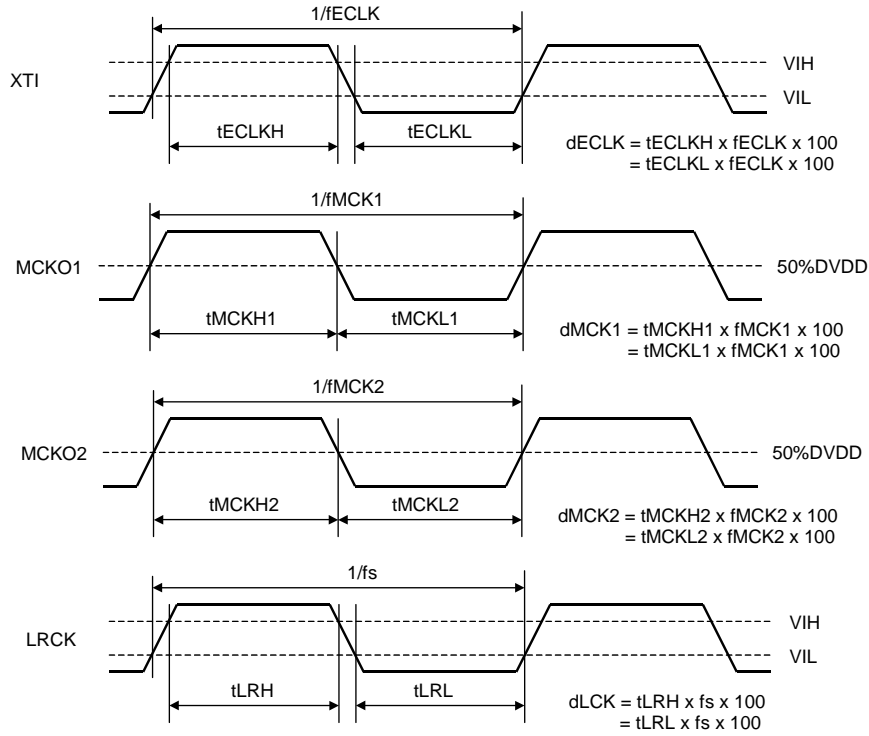


Figure 3. Clock Timing

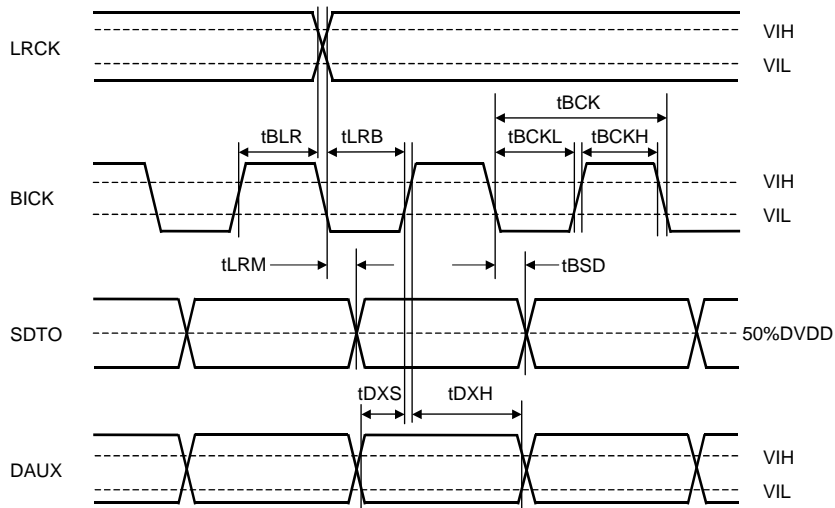


Figure 4. Serial Interface Timing (Slave Mode)

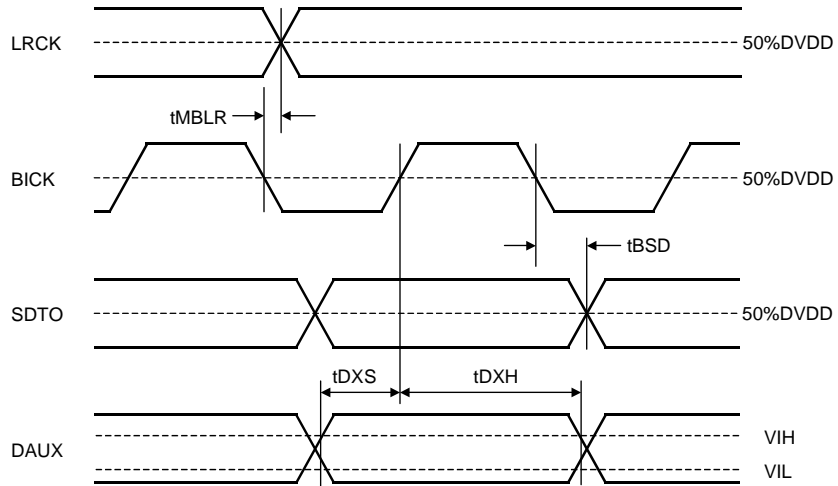


Figure 5. Serial Interface Timing (Master Mode)

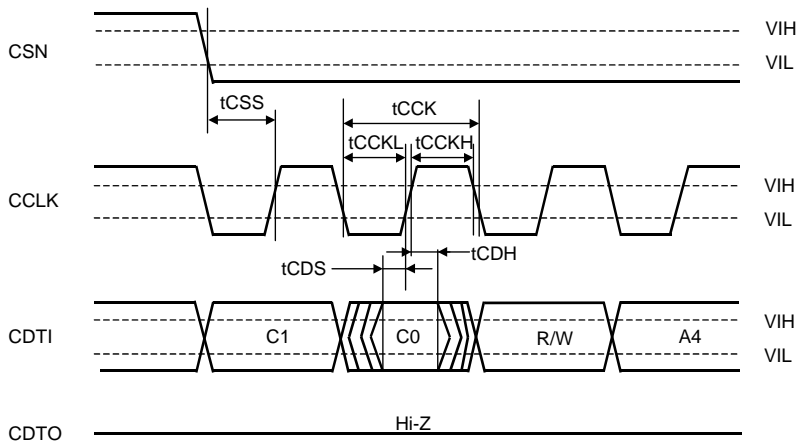


Figure 6. WRITE/READ Command Input Timing (4-wire serial mode)

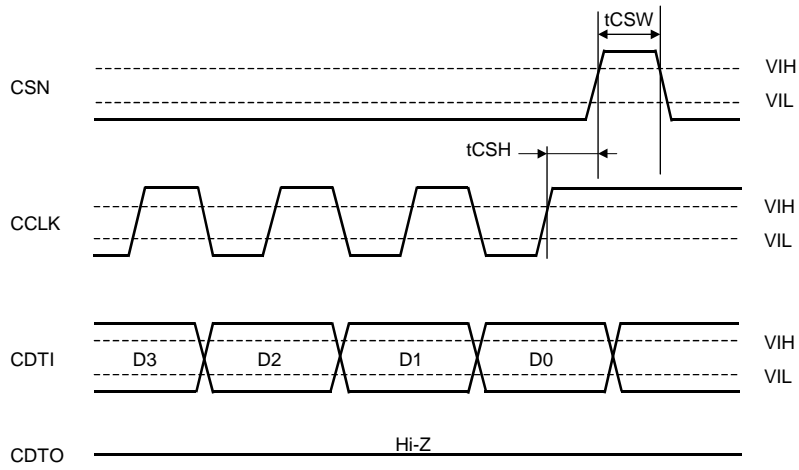


Figure 7. WRITE Data Input Timing (4-wire serial mode)

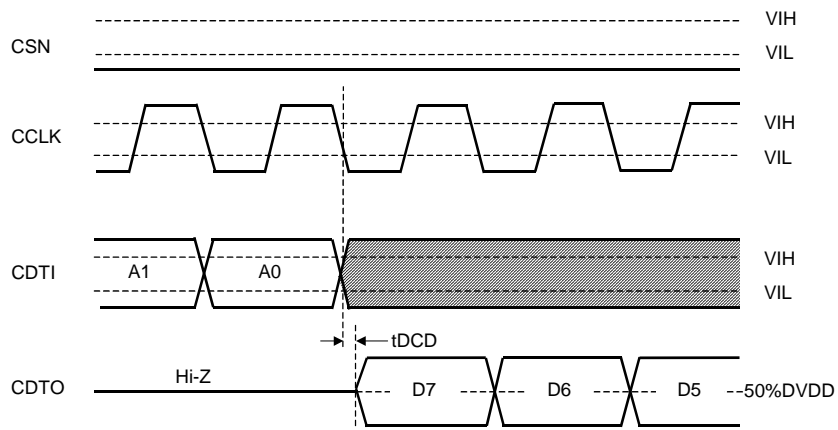


Figure 8. READ Data Output Timing 1 (4-wire serial mode)

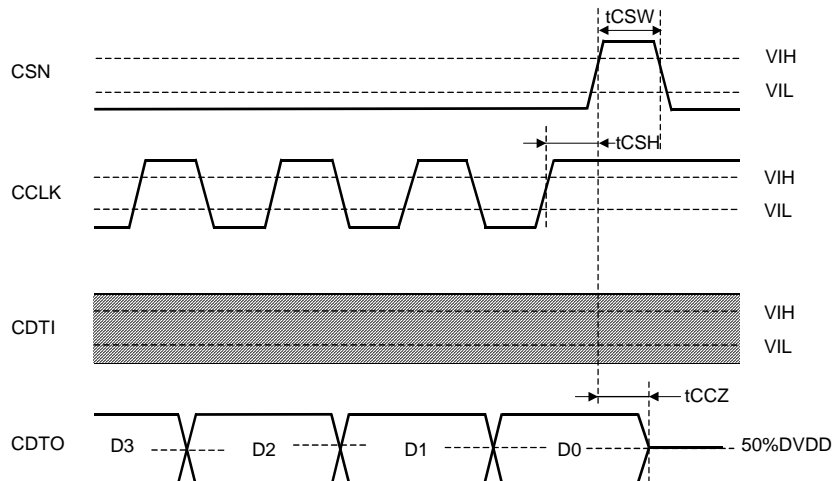


Figure 9. READ Data Output Timing 2 (4-wire serial mode)

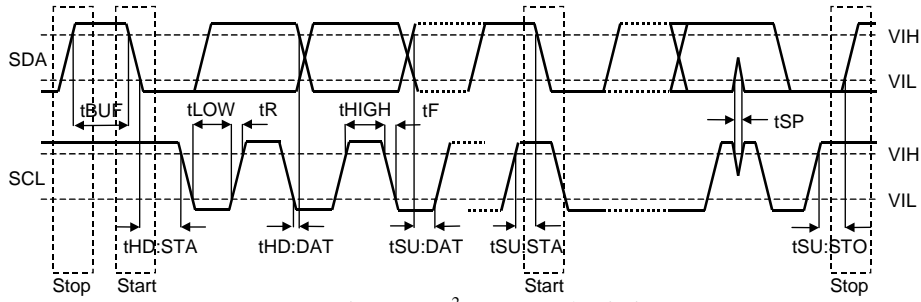


Figure 10. I²C Bus Mode Timing

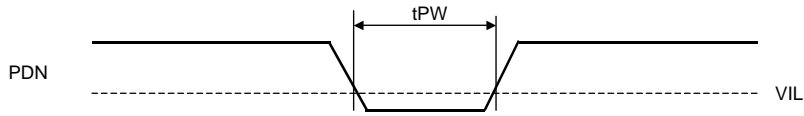


Figure 11. Power-down & Reset Timing

OPERATION OVERVIEW

■ **Non-PCM (Dolby Digital, MPEG, etc) and DTS-CD Bitstream Detection**

The AK4113 has a non-PCM bit stream auto-detection function. When the 32bit mode non-PCM preamble based on Dolby “Dolby Digital Data Stream in IEC 60958 Interface” is detected, the NPCM bit sets to “1”. The 96-bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the NPCM bit to “1”. Once the NPCM bit is set to “1”, it will remain “1” until 4096 frames pass through the chip without an additional sync pattern being detected. When those preambles are detected, the burst preambles Pc (burst information: Table 17) and Pd (length code: Table 18) that follow those sync codes are stored to registers. The AK4113 has also a DTS-CD bitstream auto-detection function. When the AK4113 detects DTS-CD bitstream, the DTSCD bit sets to “1”. If the next sync code does not occur within 4096frames, the DTSCD bit sets to “0” until a non-PCM bitstream is detected again. The ORed value of NPCM and DTSCD bits are output to AUTO bit. The AK4113 detects the 14-bit sync word and the 16-bit sync word of a DTS-CD bitstream, the detection function can be set ON/OFF by DTS14 and DTS16 bits in serial control mode.

In parallel control mode, logical OR value of the AUTO and AUDION bits are outputted to the INTI pin. The DTS-CD detects both the 14-bit sync word and the 16-bit sync word.

■ **216kHz Clock Recovery**

The integrated low jitter PLL has a wide lock range from 8kHz to 216kHz. The lock time depends on sampling frequency (fs) and FAST bit. (See Figure 12) FAST bit is useful at lower sampling frequency and is fixed to “0” in parallel control mode. In serial control mode, the AK4113 has a sampling frequency detection function (8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz) that uses either a clock comparison against the X’tal oscillator or the channel status information from the setting of XTL1-0 bits. In parallel control mode, the sampling frequency is detected by using the reference frequency, 24.576MHz. When the sampling frequency is more than 64kHz, FS96 pin goes to “H”. When the sampling frequency is less than 54kHz, FS96 pin goes to “L”. The PLL loses lock when the received sync interval is incorrect.

| FAST bit | PLL Lock Time | |
|----------|--|---------|
| 0 | $\leq (15 \text{ ms} + 384/\text{fs})$ | Default |
| 1 | $\leq (15 \text{ ms} + 1/\text{fs})$ | |

Figure 12. PLL Lock Time (fs: Sampling Frequency)

■ Clock Operation Mode

The CM0 and CM1 pins (or bits) select the clock source and the data source of SDTO. In Mode 2, the clock source is switched from PLL to X'tal when PLL goes unlock state. In Mode3, the clock source is fixed to X'tal, but PLL is also operating and the recovered data such as C bits can be monitored. For Mode2 and 3, it is recommended that the frequency of X'tal is different from the recovered frequency from PLL.

| Mode | CM1 | CM0 | UNLOCK | PLL | X'tal | Clock source | SDTO |
|------|-----|-----|--------|-----|-----------|--------------|------|
| 0 | 0 | 0 | - | ON | ON (Note) | PLL | RX |
| 1 | 0 | 1 | - | OFF | ON | X'tal | DAUX |
| 2 | 1 | 0 | 0 | ON | ON | PLL | RX |
| | | | 1 | ON | ON | X'tal | DAUX |
| 3 | 1 | 1 | - | ON | ON | X'tal | DAUX |

Default

ON: Oscillation (Power-up), OFF: STOP (Power-Down)

Note: When the X'tal is not used as clock comparison for fs detection (i.e. XTL1-0 bit = "11"), the X'tal is OFF.

Table 1. Clock Operation Mode Select

■ Master Clock

The AK4113 has two clock outputs, MCKO1 and MCKO2. MCKO2 has two modes. These modes can be selected by the XMCK bit.

1) When XMCK bit = "0" and BCU bit = "0"

This mode is compatible AK4112B and AK4114. These clocks are derived from either the recovered clock or the X'tal oscillator. The frequencies of the master clock outputs (MCKO1 and MCKO2) are set by OCKS0 and OCKS1 as shown in Table 2. The 512fs clock will not operate when the sampling frequency is 96kHz or 192kHz. The 256fs clock will not operate when the sampling frequency is 192kHz.

| No. | OCKS1 | OCKS0 | MCKO1 pin | MCKO2 pin | X'tal | fs (max) |
|-----|-------|-------|-----------|-----------|-------|----------|
| 0 | 0 | 0 | 256fs | 256fs | 256fs | 108 kHz |
| 1 | 0 | 1 | 256fs | 128fs | 256fs | 108 kHz |
| 2 | 1 | 0 | 512fs | 256fs | 512fs | 54 kHz |
| 3 | 1 | 1 | 128fs | 64fs | 128fs | 216 kHz |

Default

Table 2. Master Clock Output Frequency

2) When XMCK bit "1" and BCU bit = "0"

MCKO2 outputs the input clock of the XTI pin when BCU bit = "0" and XMCK bit = "1". The settings of CM1-0 and OCKS1-0 bits are ignored. The output frequency can be set by the DIV bit. MCKO1 outputs a clock that is selected by the CM1-0 bits and OCKS1-0 bits.

| XMCK bit | DIV bit | MCKO2 Clock Source | MCKO2 Frequency |
|----------|---------|--------------------|-----------------|
| 1 | 0 | X'tal | x 1 |
| 1 | 1 | X'tal | x 1/2 |

Table 3. Select output frequency of MCKO2

■ Clock Source

The following circuits are available to feed the clock to the XTI pin of the AK4113.

1) X'tal

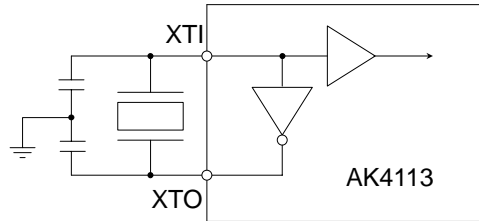


Figure 13. X'tal mode

Note: External capacitance depends upon the crystal oscillator (typ.10-40pF)

2) External clock

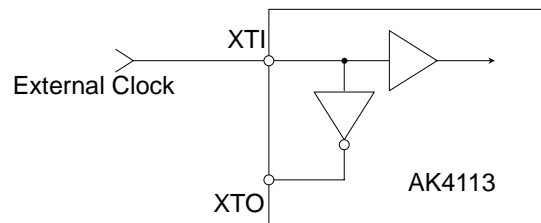


Figure 14. External clock mode

3) Fixed to the Clock Operation Mode 0

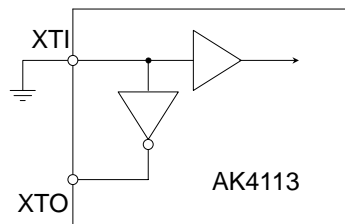


Figure 15. OFF Mode

■ Sampling Frequency and Pre-emphasis Detection

The AK4113 has two methods for detecting the sampling frequency.

1. Clock comparison between the recovered clock and X'tal oscillator
2. Sampling frequency information on channel status

The method is selected by the XTL1-0 bits. The detected frequency is available on the FS3-0 bits.

When XTL1-0 bits = "11", the sampling frequency is detected by the channel status sampling frequency information. The detected frequency is available on the FS3-0 bits. In parallel control mode, XTL1-0 bits are fixed to "10".

| XTL1 bit | XTL0 bit | X'tal Frequency |
|----------|----------|----------------------|
| 0 | 0 | 11.2896MHz |
| 0 | 1 | 12.288MHz |
| 1 | 0 | 24.576MHz |
| 1 | 1 | (Use channel status) |

Default

Table 4. Reference X'tal frequency

| Register output | | | | fs | Except XTL1-0 bit = "11" | XTL1-0 bit = "11" | | |
|-----------------|-----|-----|-----|-----------|----------------------------|-------------------------|-----------------------------|------------------|
| | | | | | Clock comparison (Note 10) | Consumer mode (Note 11) | Professional mode (Note 12) | |
| FS3 | FS2 | FS1 | FS0 | | | Byte3 Bit3,2,1,0 | Byte0 Bit7,6 | Byte4 Bit6,5,4,3 |
| 0 | 0 | 0 | 0 | 44.1kHz | 44.1kHz ± 3% | 0 0 0 0 | 0 1 | 0 0 0 0 |
| 0 | 0 | 0 | 1 | Reserved | - | 0 0 0 1 | (Others) | |
| 0 | 0 | 1 | 0 | 48kHz | 48kHz ± 3% | 0 0 1 0 | 1 0 | 0 0 0 0 |
| 0 | 0 | 1 | 1 | 32kHz | 32kHz ± 3% | 0 0 1 1 | 1 1 | 0 0 0 0 |
| 0 | 1 | 0 | 0 | 22.05kHz | 22.05kHz ± 3% | 0 1 0 0 | 0 0 | 1 0 0 1 |
| 0 | 1 | 0 | 1 | 11.025kHz | 11.025kHz ± 3% | | | |
| 0 | 1 | 1 | 0 | 24kHz | 24kHz ± 3% | 0 1 1 0 | 0 0 | 0 0 0 1 |
| 0 | 1 | 1 | 1 | 16kHz | 16kHz ± 3% | | | |
| 1 | 0 | 0 | 0 | 88.2kHz | 88.2kHz ± 3% | 1 0 0 0 | 0 0 | 1 0 1 0 |
| 1 | 0 | 0 | 1 | 8kHz | 8kHz ± 3% | | | |
| 1 | 0 | 1 | 0 | 96kHz | 96kHz ± 3% | 1 0 1 0 | 0 0 | 0 0 1 0 |
| 1 | 0 | 1 | 1 | 64kHz | 64kHz ± 3% | | | |
| 1 | 1 | 0 | 0 | 176.4kHz | 176.4kHz ± 3% | 1 1 0 0 | 0 0 | 1 0 1 1 |
| 1 | 1 | 1 | 0 | 192kHz | 192kHz ± 3% | 1 1 1 0 | 0 0 | 0 0 1 1 |

Note 10. At least ±3% range is identified as the value in the. Table 5. In case of intermediate frequency of those two, FS3-0 bits indicate no value. When the frequency is much bigger than 192kHz or much smaller than 8kHz, FS3-0 bits may indicate "0001" or "1101".

Note 11. In consumer mode, Byte3 Bit3-0 are copied to FS3-0 bits.

Note 12. In professional mode, FS3-0 bit indicates "0001" except for frequency shown by Table 5.

Table 5. fs Information

The pre-emphasis information is detected and reported on PEM bit. This information is extracted from channel 1 by default. It can be switched to channel 2 by the CS12 bit in control register.

| PEM bit | Pre-emphasis | Byte 0 Bits 3-5 |
|---------|--------------|-----------------|
| 0 | OFF | ≠ 0X100 |
| 1 | ON | 0X100 |

Table 6. PEM in Consumer Mode

| PEM bit | Pre-emphasis | Byte 0 Bits 2-4 |
|---------|--------------|-----------------|
| 0 | OFF | ≠ 110 |
| 1 | ON | 110 |

Table 7. PEM in Consumer Mode

■ De-emphasis Filter Control

The AK4113 includes a digital de-emphasis filter (tc=50/15µs). This is an IIR filter that corresponds to four sampling frequencies (32kHz, 44.1kHz and 48kHz). When DEAU bit="1", the de-emphasis filter is enabled automatically by the sampling frequency and pre-emphasis information in the channel status. The AK4113 is in this mode by default. In parallel control mode, the AK4113 is always placed in this mode and the status bits in channel 1 control the de-emphasis filter. In serial control mode, DEM1-0 bits control the de-emphasis filter when the DEAU is "0". The internal de-emphasis filter is bypassed and the recovered data is available without any change if the de-emphasis mode is OFF. When the PEM bit is "0", the internal de-emphasis filter is always bypassed.

| PEM bit | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Mode |
|---------|----------|---------|---------|---------|---------|
| 1 | 0 | 0 | 0 | 0 | 44.1kHz |
| 1 | 0 | 0 | 1 | 0 | 48kHz |
| 1 | 0 | 0 | 1 | 1 | 32kHz |
| 1 | (Others) | | | | OFF |
| 0 | x | x | x | x | OFF |

Table 8. De-emphasis Auto Control at DEAU bit = "1" (Default)

| PEM bit | DEM1 bit | DEM0 bit | Mode |
|---------|----------|----------|---------|
| 1 | 0 | 0 | 44.1kHz |
| 1 | 0 | 1 | OFF |
| 1 | 1 | 0 | 48kHz |
| 1 | 1 | 1 | 32kHz |
| 0 | x | x | OFF |

Default

Table 9. De-emphasis Manual Control at DEAU bit = "0"

■ System Reset and Power-Down

The AK4113 has a power-down mode for all circuits using the PDN pin or it can be partially powerd-down with the PWN bit. The RSTN bit initializes the register and resets the internal timing. In parallel control mode, only control by the PDN pin is enabled. The AK4113 should be reset once by bringing PDN pin = "L" upon power-up.

PDN Pin:

All analog and digital circuits are placed in power-down and reset mode by bringing PDN pin = "L". All the registers are initialized, and clocks are stopped. Reading/Witting to the registers are disabled.

RSTN Bit (Address 00H; D0):

All the registers except PWN and RSTN bits are initialized by bringing RSTN bit = "0". The internal timings is also initialized. Writing to registers is not available except the PWN and RSTN bits. Reading from the registers is disabled.

PWN Bit (Address 00H; D1):

The clock recovery is initialized by bringing PWN bit = "0". In this case, the clocks are stopped. The registers are not initialized and the mode settings are maintained. Writing and reading to the registers are enabled.

■ Bi-phase Input

Six receiver inputs (RX1-6) are available in serial control mode. IPS2-0 bits select the receiver channel. In parallel control mode, two receiver inputs (RX1 or RX5) are available. The receiver channel is selected by IPS pin. Each input includes an amplifier for unbalanced mode that can accept a signal of 350mV or more. When BCU and UCE bits are changed, the Block start signal, C bit and U bit can output from each pins. (See Table 12 and Figure 16)

| IPS2 bit | IPS1 bit | IPS0 bit | INPUT Data |
|----------|----------|----------|------------|
| 0 | 0 | 0 | RX1 |
| 0 | 0 | 1 | RX2 |
| 0 | 1 | 0 | RX3 |
| 0 | 1 | 1 | RX4 |
| 1 | 0 | 0 | RX5 |
| 1 | 0 | 1 | RX6 |
| 1 | 1 | 0 | No use |
| 1 | 1 | 1 | No use |

Default

Table 10. Recovery Data Select at serial control mode

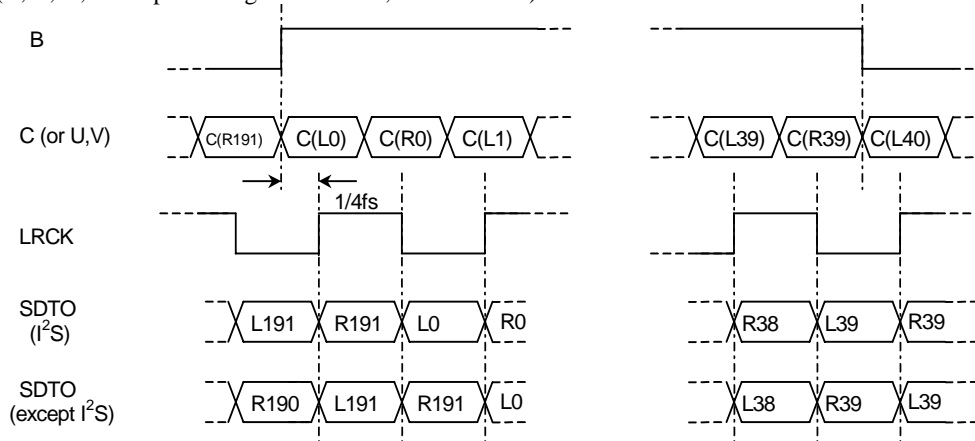
| IPS pin | INPUT Data |
|---------|------------|
| L | RX1 |
| H | RX5 |

Table 11. Recovery Data Select at parallel control mode

| BCU bit | UCE bit | MCKO2 pin | INT1 pin |
|---------|----------------|---------------------------|--------------|
| 0 | x (Don't care) | MCKO2 clock output | INT1 output |
| 1 | 0 | Block start signal output | U-bit output |
| 1 | 1 | Block start signal output | C-bit output |

Table 12. B, C, U output pins select

(B, C, U, V Output timing at RX mode, Master mode)



* The block signal goes high at the start of frame 0 and remains high until the end of frame 39.

Figure 16. B, C, U, V Output Timing

■ Bi-phase Output

In serial control mode, the source of the loop-through output from TX is selected from RX1-6. The bi-phase loop-through output is selected by OPS2-0 bits. The bi-phase loop-through output from TX can be stopped by XTE bit. In parallel control mode, the bi-phase loop-through output can not be outputted.

| OPS2 bit | OPS1 bit | OPS0 bit | INPUT Data |
|----------|----------|----------|------------|
| 0 | 0 | 0 | RX1 |
| 0 | 0 | 1 | RX2 |
| 0 | 1 | 0 | RX3 |
| 0 | 1 | 1 | RX4 |
| 1 | 0 | 0 | RX5 |
| 1 | 0 | 1 | RX6 |
| 1 | 1 | 0 | No use |
| 1 | 1 | 1 | No use |

Default

Table 13. Output Data Select

■ Bi-phase signal input/output circuit

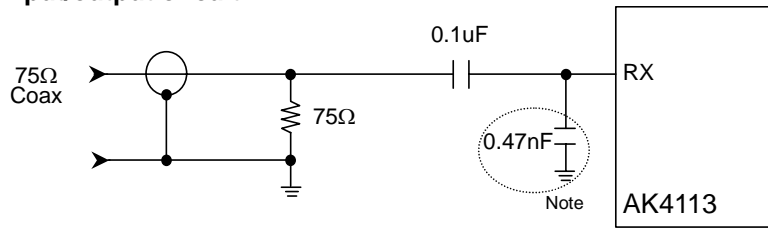


Figure 17. Consumer Input Circuit (Coaxial Input)

Note: For coaxial input, if a coupling level to this input from the next RX input line pattern exceeds 50mV, there may be an incorrect operation. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.

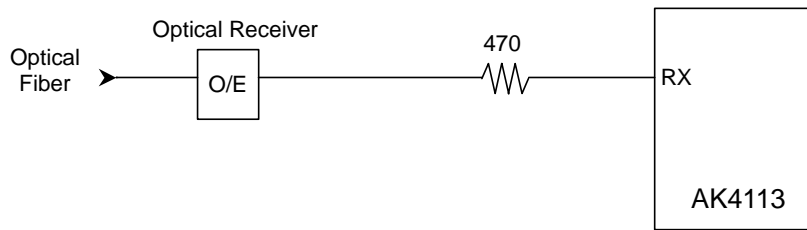


Figure 18. Consumer Input Circuit (Optical Input)

For coaxial input in serial mode, the input level of RX line is small, so care must be taken to avoid crosstalk among the RX input lines. In this case, a shield is recommended between the input lines. In parallel control mode, two channel inputs (RX1 and RX5) are available, RX2, RX3, RX4 and RX6 change to other pins for mode settings. Those pins must be fixed to “H” or “L” because they are not normal logic input.

The AK4113 includes the TX output buffer. The output level meets combination $0.5V \pm 20\%$ using the external resistor network. The T1 in Figure 19 is a transformer of 1:1.

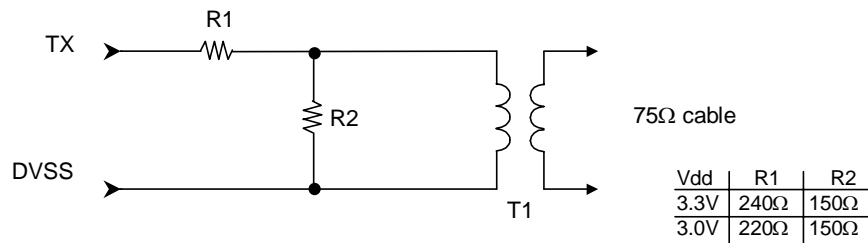


Figure 19. TX External Resistor Network

■ U-bit buffers

The AK4113 has a Q-subcode buffer for CD application. The AK4113 takes the Q-subcode into registers by the following method.

1. The sync word (S0,S1) is constructed of at least 16 "0"s.
2. The start bit is "1".
3. Those 7bits Q-W follows to the start bit.
4. The distance between two start bits are 8-16 bits.

The QINT bit in the control register goes to "1" when the new Q-subcode differs from old one, and goes to "0" when the QINT bit is read.

| | | | | | | | | | |
|-----|---|-----|-----|-----|-----|-----|-----|-----|------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | * |
| S0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0... |
| S1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0... |
| S2 | 1 | Q2 | R2 | S2 | T2 | U2 | V2 | W2 | 0... |
| S3 | 1 | Q3 | R3 | S3 | T3 | U3 | V3 | W3 | 0... |
| : | : | : | : | : | : | : | : | : | : |
| S97 | 1 | Q97 | R97 | S97 | T97 | U97 | V97 | W97 | 0... |
| S0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0... |
| S1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0... |
| S2 | 1 | Q2 | R2 | S2 | T2 | U2 | V2 | W2 | 0... |
| S3 | 1 | Q3 | R3 | S3 | T3 | U3 | V3 | W3 | 0... |
| : | : | : | : | : | : | : | : | : | : |

(*) number of "0" : min=0; max=8.

Figure 20. Configuration of U-bit (CD)

| | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|-----|-----|-----|------|-----|-----|-----|-----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | Q8 | Q9 | Q10 | Q11 | Q12 | Q13 | Q14 | Q15 | Q16 | Q17 | Q18 | Q19 | Q20 | Q21 | Q22 | Q23 | Q24 | Q25 |
| CTRL | | | | ADRS | | | | TRACK NUMBER | | | | | | | | INDEX | | | | | | | |
| Q26 | Q27 | Q28 | Q29 | Q30 | Q31 | Q32 | Q33 | Q34 | Q35 | Q36 | Q37 | Q38 | Q39 | Q40 | Q41 | Q42 | Q43 | Q44 | Q45 | Q46 | Q47 | Q48 | Q49 |
| MINUTE | | | | | | | | SECOND | | | | | | | | FRAME | | | | | | | |
| Q50 | Q51 | Q52 | Q53 | Q54 | Q55 | Q56 | Q57 | Q58 | Q59 | Q60 | Q61 | Q62 | Q63 | Q64 | Q65 | Q66 | Q67 | Q68 | Q69 | Q70 | Q71 | Q72 | Q73 |
| ZERO | | | | | | | | ABSOLUTE MINUTE | | | | | | | | ABSOLUTE SECOND | | | | | | | |
| Q74 | Q75 | Q76 | Q77 | Q78 | Q79 | Q80 | Q81 | Q82 | Q83 | Q84 | Q85 | Q86 | Q87 | Q88 | Q89 | Q90 | Q91 | Q92 | Q93 | Q94 | Q95 | Q96 | Q97 |
| ABSOLUTE FRAME | | | | | | | | CRC $G(x)=x^{16}+x^{12}+x^5+1$ | | | | | | | | | | | | | | | |

Figure 21. Q-subcode

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 13H | Q-subcode Address / Control | Q9 | Q8 | ... | ... | ... | ... | Q3 | Q2 |
| 14H | Q-subcode Track | Q17 | Q16 | ... | ... | ... | ... | Q11 | Q10 |
| 15H | Q-subcode Index | ... | ... | ... | ... | ... | ... | ... | ... |
| 16H | Q-subcode Minute | ... | ... | ... | ... | ... | ... | ... | ... |
| 17H | Q-subcode Second | ... | ... | ... | ... | ... | ... | ... | ... |
| 18H | Q-subcode Frame | ... | ... | ... | ... | ... | ... | ... | ... |
| 19H | Q-subcode Zero | ... | ... | ... | ... | ... | ... | ... | ... |
| 1AH | Q-subcode ABS Minute | ... | ... | ... | ... | ... | ... | ... | ... |
| 1BH | Q-subcode ABS Second | ... | ... | ... | ... | ... | ... | ... | ... |
| 1CH | Q-subcode ABS Frame | Q81 | Q80 | ... | ... | ... | ... | Q75 | Q74 |

Figure 22. Q-subcode register

■ Error Handling

The following nine events cause the INT0 and INT1 pins to show the status of the interrupt condition. When the PLL is OFF (Clock Operation Mode 1), INT0 and INT1 pins go to “L”.

1. UNLCK : PLL unlock state detect
“1” when the PLL loses lock. The AK4113 loses lock when the distance between two preamble is not correct or when those preambles are not correct.
2. PAR : Parity error or bi-phase coding error detection
“1” when parity error or bi-phase coding error is detected, updated every sub-frame cycle.
3. AUTO : Non-Linear PCM or DTS-CD Bit Stream detection
The OR function of NPCM and DTSCD bits is available at the AUTO bit.
4. V : Validity flag detection
“1” when validity flag is detected. Updated every sub-frame cycle.
5. AUDION : Non-audio detection
“1” when the “AUDION” bit in recovered channel status indicates “1”. Updated every block cycle.
6. STC : Sampling frequency or pre-emphasis information change detection
When either FS3-0 bit or PEM bit is changed, it maintains “1” during 1 sub-frame.
7. QINT : U-bit Sync flag
“1” when the Q-subcode differs from the old one. Updated every sync code cycle for Q-subcode.
8. CINT : Channel status sync flag
“1” when received C bit differs from the old one. Updated every block cycle.
9. DAT : DAT Start ID detect
“1” when the category code indicates “DAT” and “DAT Start ID” is detected. When DCNT bit is “1”, it does not indicate “1” even if “DAT Start ID” is detected again within “3841 x LRCK”.
When “DAT Start ID” is detected again after “3840 x LRCK” passed, it indicates “1”. When DCNT bit is “0”, it indicates “1” every “DAT Start ID” detection.

1. Parallel control mode

In parallel control mode, the INT0 pin outputs the ORed signal between UNLCK and PAR. The INT1 pin outputs the ORed signal between AUTO and AUDION. Once INT0 goes "H", it maintains "H" for 1024/fs cycles after the all error events are removed. Table 14 shows the state of each output pins when the INT0/1 pin is "H".

| Event | | | | Pin | | | |
|-------|-----|------|--------|---------|---------|---------------|---------|
| UNLCK | PAR | AUTO | AUDION | INT0 | INT1 | SDTO | V |
| 1 | x | x | x | "H" | Note 13 | "L" | "L" |
| 0 | 1 | x | x | | | Previous Data | Output |
| 0 | 0 | x | x | "L" | | Output | Output |
| x | x | 1 | x | Note 14 | "H" | Note 15 | Note 16 |
| x | x | x | 1 | | | | |
| x | x | 0 | 0 | | "L" | | |

Note 13. INT1 pin outputs "L" or "H" in accordance with the ORed signal between AUTO and AUDION.

Note 14. INT0 pin outputs "L" or "H" in accordance with the ORed signal between UNLCK and PAR.

Note 15. SDTO pin outputs "L", "Previous Data" or "Normal Data" in accordance with the ORed signal between UNLCK and PAR.

Note 16. V pin outputs "L" or "Normal operation" in accordance with the ORed signal between PAR and UNLCK.

Table 14. Error Handling in parallel control mode (x: Don't care)

2. Serial control mode

In serial control mode, the INT1 and INT0 pins output an ORed signal based on the above nine interrupt events. When masked, the interrupt event does not affect the operation of the INT1-0 pins (the masks do not affect the registers in 07H and DAT bit). Once the INT0 pin goes to "H", it remains "H" for 1024/fs (this value can be changed with the EFH1-0 bits) after all events not masked by mask bits are cleared. INT1 pin immediately goes to "L" when those events are cleared.

UNLCK, PAR, AUTO, AUDION and V bits in Address=07H indicate the interrupt status events above in real time. Once QINT, CINT and DAT bits goes to "1", it stays "1" until the register is read.

When the AK4113 loses lock, the channel status bit, user bit, Pc and Pd are initialized. In this initial state, INT0 pin outputs the ORed signal between UNLCK and PAR bits. INT1 pin outputs the ORed signal between AUTO and AUDION bits.

| Event | | | Pin | | |
|-------|-----|--------|---------------|--------|--------|
| UNLCK | PAR | Others | SDTO | V | TX |
| 1 | x | x | "L" | "L" | Output |
| 0 | 1 | x | Previous Data | Output | Output |
| x | x | x | Output | Output | Output |

Table 15. Error Handling in serial control mode (x: Don't care)

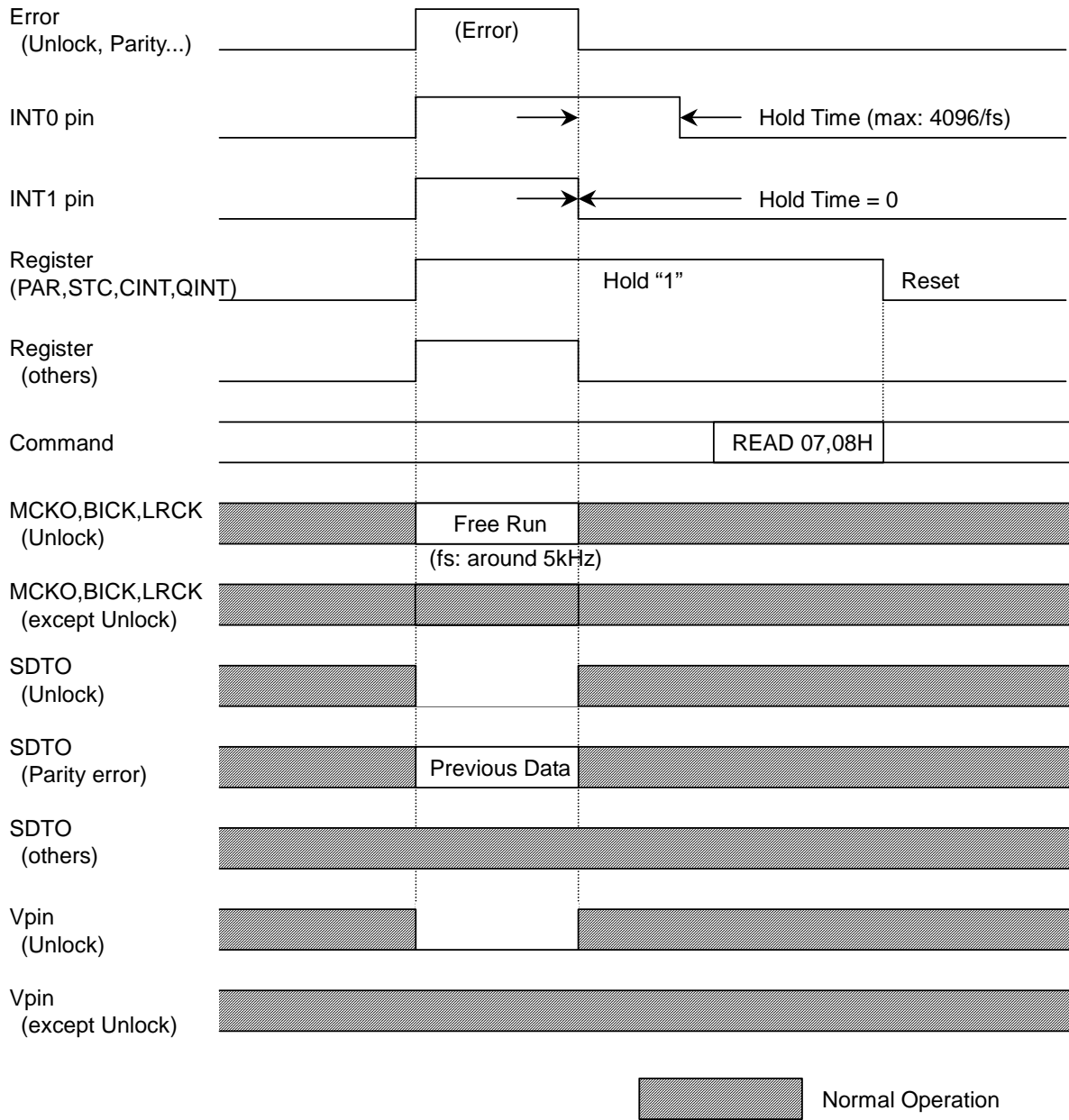


Figure 23. INT0/1 pin Timing

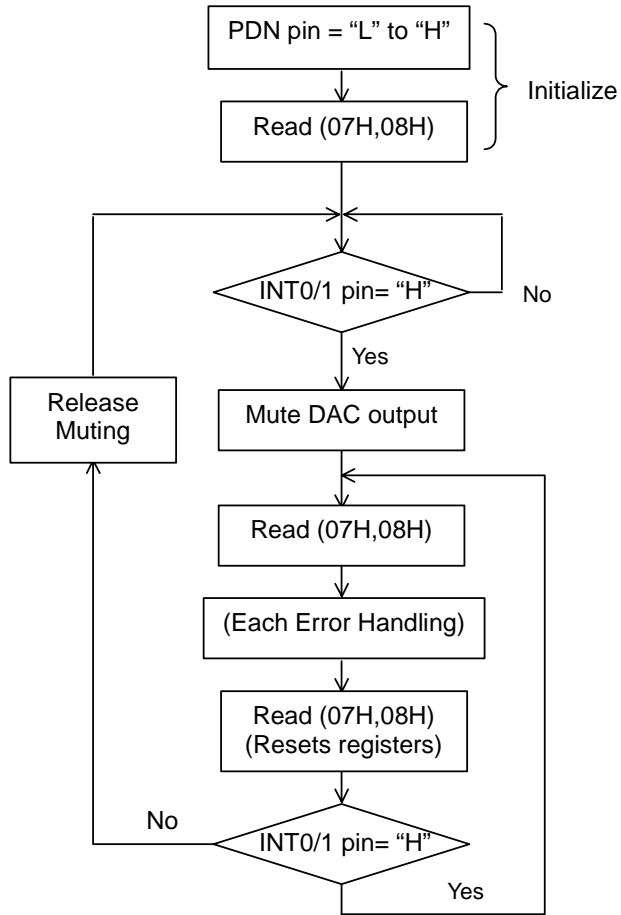


Figure 24. Error Handling Sequence Example 1

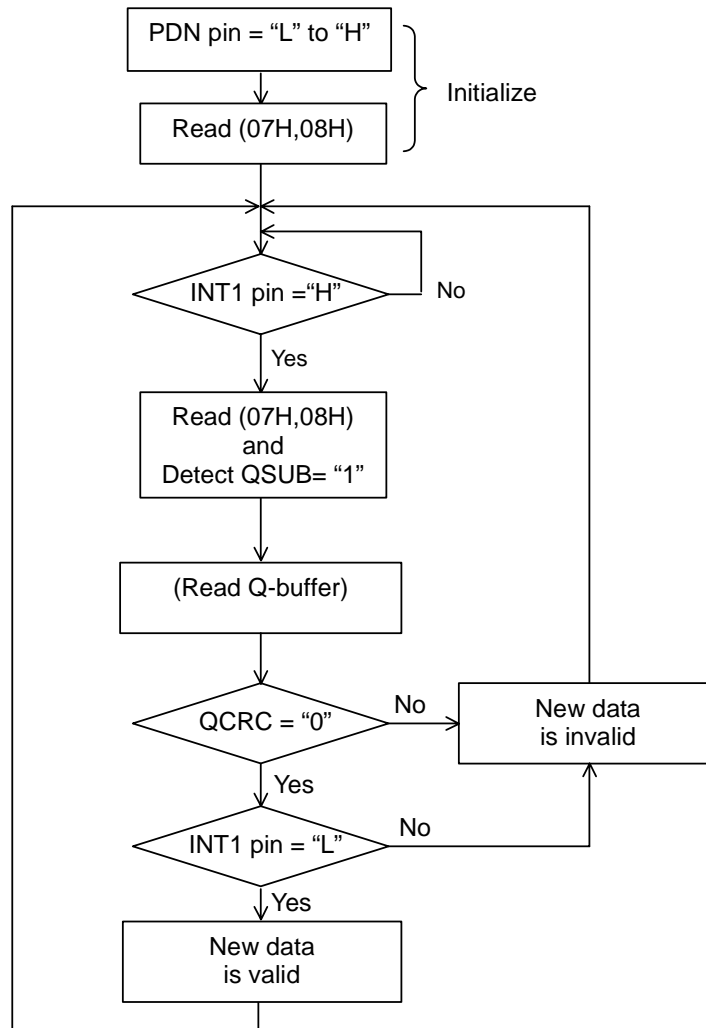


Figure 25. Error Handling Sequence Example (for Q/CINT)

■ Audio Serial Interface Format

The DIF0, DIF1 and DIF2 pins can select eight serial data formats as shown in Table 16. In all formats the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and DAUX is latched on the rising edge of BICK. BICK outputs 64fs clock in Mode 0-5. Mode 6-7 are Slave Modes, and BICK is available up to 128fs at fs=48kHz. If the data word length is equal or less than 20-bits (Mode0-2), the LSBs in the sub-frame are truncated. In Mode 3-7, the last 4-LSBs are auxiliary data (see Figure 26). When the Parity Error, Bi-phase Error or Frame Length Error occurs in a sub-frame, the AK4113 continues to output the last normal sub-frame data from SDTO repeatedly until the error is removed. When the Unlock Error occurs, AK4113 outputs "0" from SDTO. If DAUX is used, the data is transformed and outputted from SDTO. DAUX is used in Clock Operation Mode 1, 3 and unlock state of Mode 2. The input data format to DAUX should be left justified except in Mode 5 and 7. In Mode 5 or 7, both the input data format of DAUX and output data format of SDTO are I²S. Mode 6 and 7 are Slave Modes that corresponds to the Master Mode of Mode 4 and 5. In Slave mode, LRCK and BICK should be synchronized with MCKO1/2.

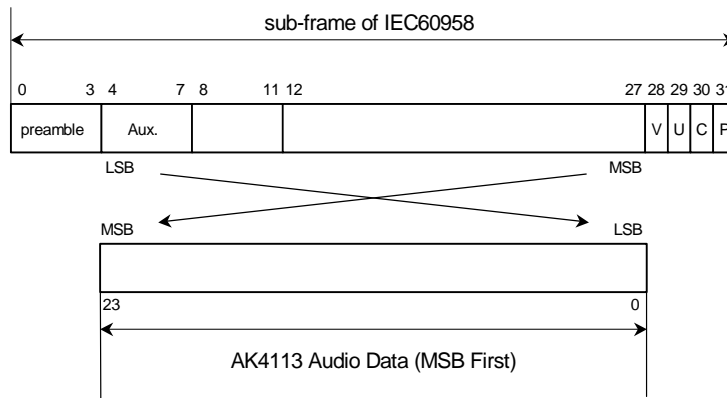


Figure 26. Bit configuration

| Mode | DIF2 | DIF1 | DIF0 | DAUX | SDTO | LRCK | | BICK | |
|------|------|------|------|--------------------------|--------------------------|------|-----|-----------------------|-----|
| | | | | | | | I/O | | I/O |
| 0 | 0 | 0 | 0 | 24-bit, Left justified | 16-bit, Right justified | H/L | O | 64fs | O |
| 1 | 0 | 0 | 1 | 24-bit, Left justified | 18-bit, Right justified | H/L | O | 64fs | O |
| 2 | 0 | 1 | 0 | 24-bit, Left justified | 20-bit, Right justified | H/L | O | 64fs | O |
| 3 | 0 | 1 | 1 | 24-bit, Left justified | 24-bit, Right justified | H/L | O | 64fs | O |
| 4 | 1 | 0 | 0 | 24-bit, Left justified | 24-bit, Left justified | H/L | O | 64fs | O |
| 5 | 1 | 0 | 1 | 24-bit, I ² S | 24-bit, I ² S | L/H | O | 64fs | O |
| 6 | 1 | 1 | 0 | 24-bit, Left justified | 24-bit, Left justified | H/L | I | 64-128fs (Note 17) | I |
| 7 | 1 | 1 | 1 | 24-bit, I ² S | 24-bit, I ² S | L/H | I | 64-128fs (Note 17) | I |

Default

Table 16. Audio Data Format

Note 17. This frequency must not exceed a maximum BICK frequency that is defined in "Switching Characteristics".

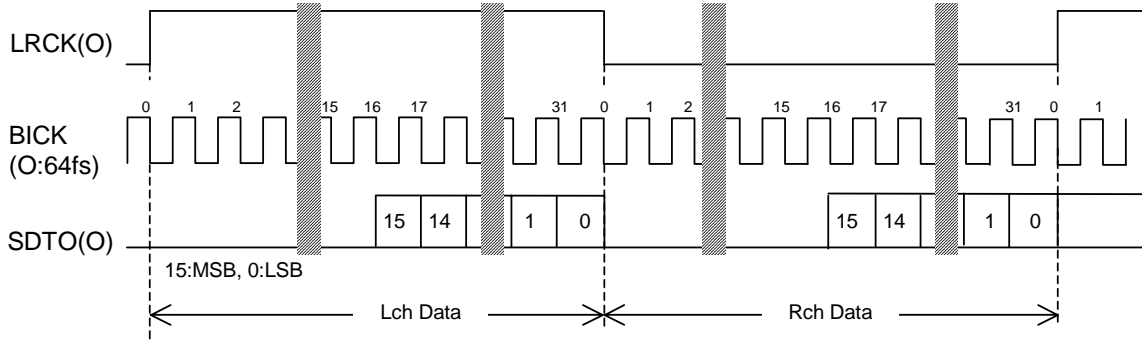


Figure 27. Mode 0 Timing

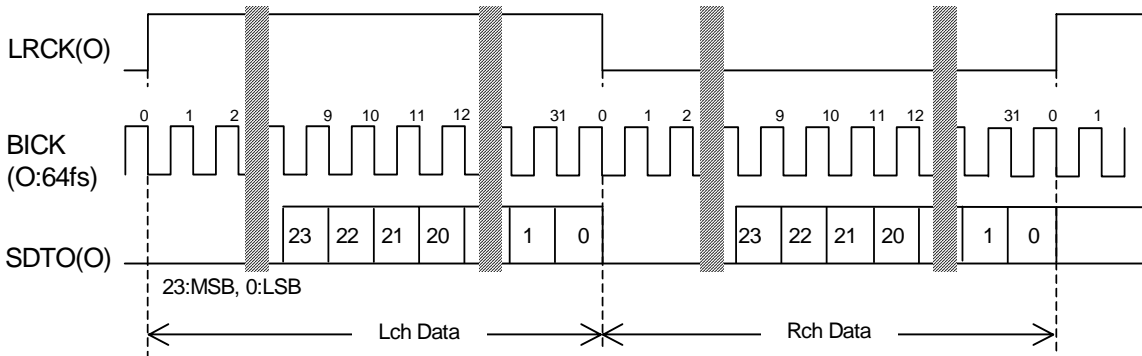


Figure 28. Mode 3 Timing

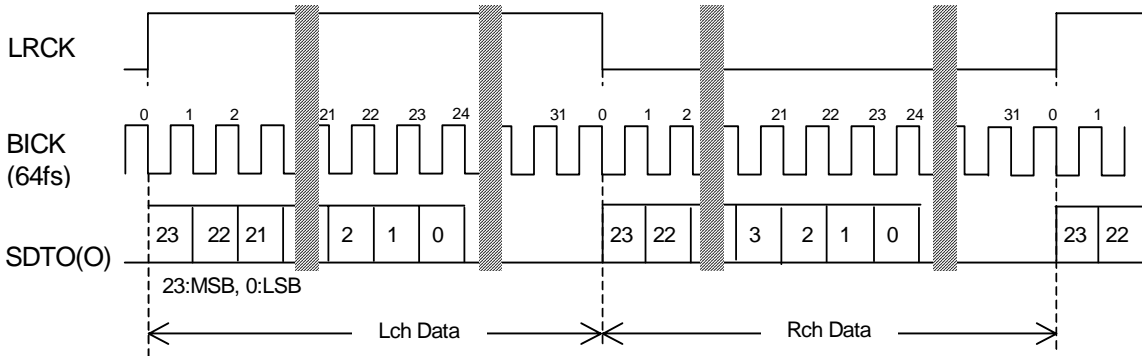


Figure 29. Mode 4, 6 Timing

Mode4 : LRCK, BICK : Output
 Mode6 : LRCK, BICK : Input

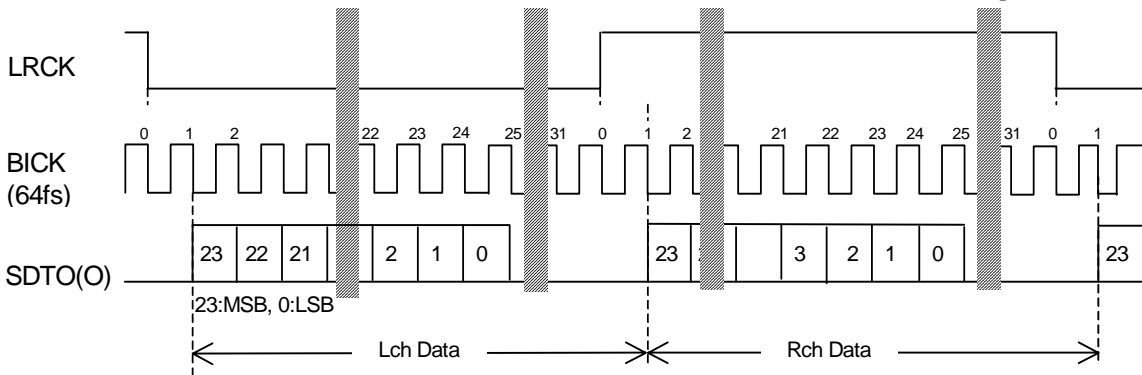


Figure 30. Mode 5, 7 Timing

Mode5 : LRCK, BICK : Output
 Mode7 : LRCK, BICK : Input

■ Serial Control Interface

1. 4-wire serial control mode (I2C pin = “L”)

The internal registers may be either written or read by the 4-wire μP interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, C1-0 are fixed to “00”), Read/Write (1-bit), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN pin = “L” resets the registers to their default values.

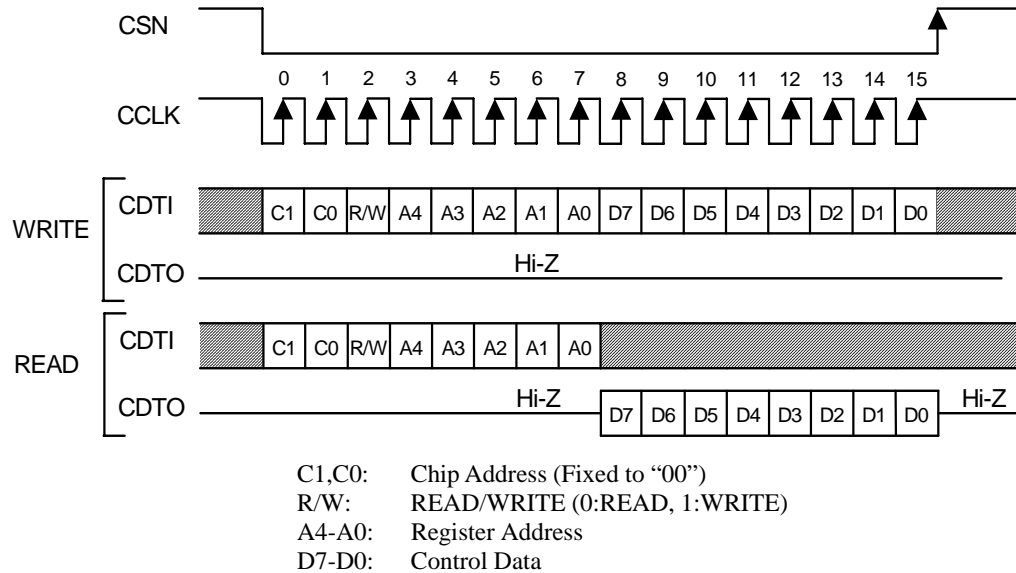


Figure 31. 4-wire Serial Control I/F Timing

* The control data can not be written when the CCLK rising edge is 15times or less or 17times or more during CSN pin is “L”.

2. I²C bus control mode (I2C pin = "H")

The AK4113 supports a fast-mode I²C-bus system (max : 400kHz).

2-1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4113 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

2-1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

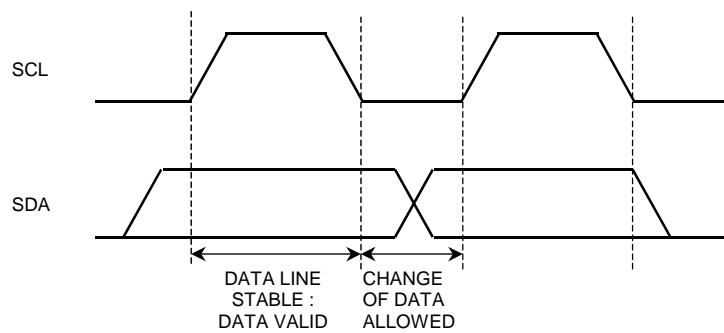


Figure 32. Data transfer

2-1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.

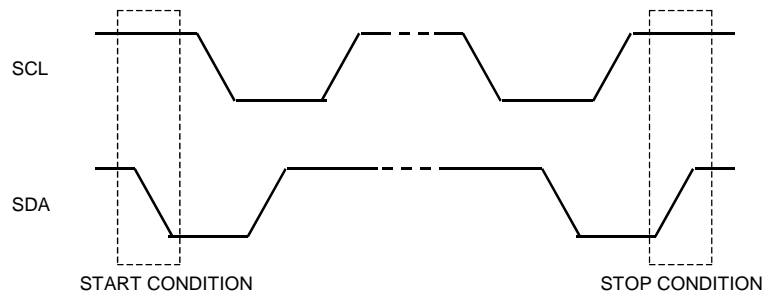


Figure 33. START and STOP conditions

2-1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable “L” during “H” period of this clock pulse. The AK4113 will generate an acknowledge after each byte has been received.

In the read mode, the slave, the AK4113 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

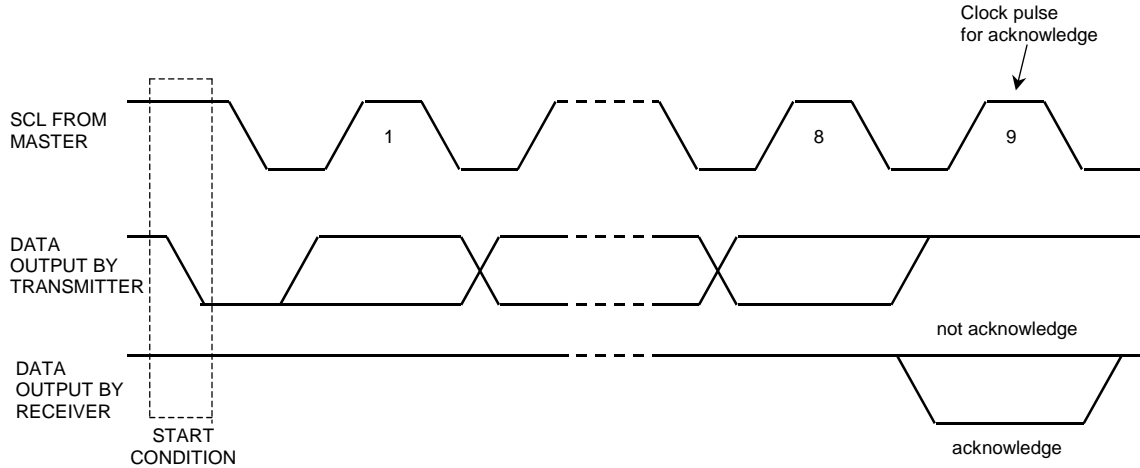
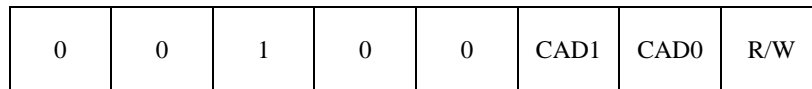


Figure 34. Acknowledge on the I²C-bus

2-1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.

The most significant five bits of the slave address are fixed as “00100”. The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set them. The eighth bit (LSB) of the first byte (R/W bit) defines whether a write or read condition is requested by the master. A “1” indicates that the read operation is to be executed. A “0” indicates that the write operation is to be executed.



(Those CAD1/0 should match with CAD1/0 pins.)

Figure 35. The First Byte

2-2. WRITE Operations

Set R/W bit = “0” for the WRITE operation of AK4113.

After receipt the start condition and the first byte, the AK4113 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4113. The format is MSB first, and those most significant 3-bits are “Don’t care”.

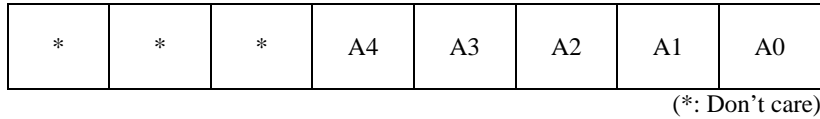


Figure 36. The Second Byte

After receipt the second byte, the AK4113 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

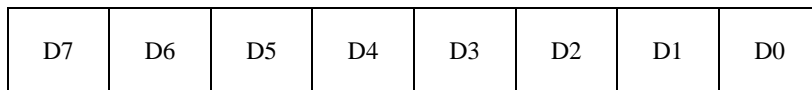


Figure 37. Byte structure after the second byte

The AK4113 is capable of more than one byte write operation by one sequence.

After receipt of the third byte, the AK4113 generates an acknowledge, and awaits the next data again. The master can transmit more than one words instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1CH prior to generating the stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

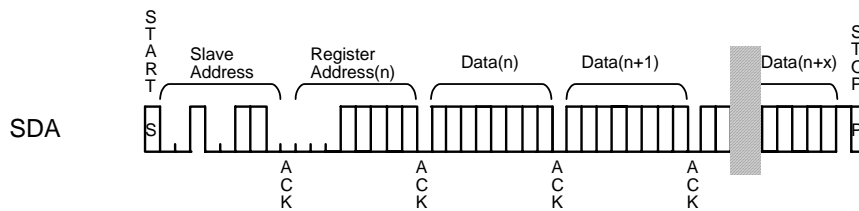


Figure 38. WRITE Operation

2-3. READ Operations

Set R/W bit = “1” for the READ operation of AK4113.

After transmission of a data, the master can read next address’s data by generating the acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1CH prior to generating the stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The AK4113 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-3-1. CURRENT ADDRESS READ

The AK4113 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1.

After receipt of the slave address with R/W bit set to “1”, the AK4113 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4113 discontinues transmission

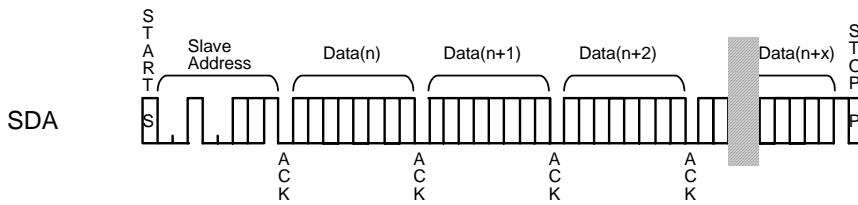


Figure 39. CURRENT ADDRESS READ

2-3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation.

The master issues the start condition, slave address(R/W bit =“0”) and then the register address’s acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to “1”. Then the AK4113 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4113 discontinues transmission.

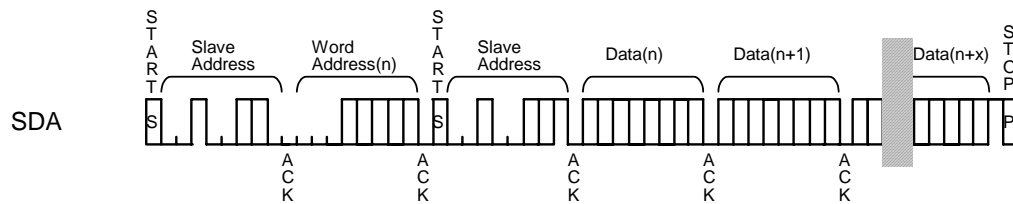


Figure 40. RANDOM READ

■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------------|-------|-------|-------|-------|-------|-------|--------|-------|
| 00H | CLK & Power Down Control | CS12 | BCU | CM1 | CM0 | OCKS1 | OCKS0 | PWN | RSTN |
| 01H | Format & De-em Control | V/TX | DIF2 | DIF1 | DIF0 | DEAU | DEM1 | DEM0 | 0 |
| 02H | Input/ Output Control 0 | 0 | XTL1 | XTL0 | UCE | TXE | OPS2 | OPS1 | OPS0 |
| 03H | Input/ Output Control 1 | EFH1 | EFH0 | FAST | XMCK | DIV | IPS2 | IPS1 | IPS0 |
| 04H | INT0 MASK | MQIT0 | MAUT0 | MCIT0 | MULK0 | MV0 | MSTC0 | MAUD0 | MPAR0 |
| 05H | INT1 MASK | MQIT1 | MAUT1 | MCIT1 | MULK1 | MV1 | MSTC1 | MAUD1 | MPAR1 |
| 06H | DAT Mask & DTS Detect | 0 | 0 | 0 | DCNT | DTS16 | DTS14 | MDAT1 | MDAT0 |
| 07H | Receiver status 0 | QINT | AUTO | CINT | UNLCK | V | STC | AUDION | PAR |
| 08H | Receiver status 1 | FS3 | FS2 | FS1 | FS0 | PEM | DAT | DTSCD | NPCM |
| 09H | Receiver status 2 | 0 | 0 | 0 | 0 | 0 | 0 | QCRC | CCRC |
| 0AH | RX Channel Status Byte 0 | CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
| 0BH | RX Channel Status Byte 1 | CR15 | CR14 | CR13 | CR12 | CR11 | CR10 | CR9 | CR8 |
| 0CH | RX Channel Status Byte 2 | CR23 | CR22 | CR21 | CR20 | CR19 | CR18 | CR17 | CR16 |
| 0DH | RX Channel Status Byte 3 | CR31 | CR30 | CR29 | CR28 | CR27 | CR26 | CR25 | CR24 |
| 0EH | RX Channel Status Byte 4 | CR39 | CR38 | CR37 | CR36 | CR35 | CR34 | CR33 | CR32 |
| 0FH | Burst Preamble Pc Byte 0 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| 10H | Burst Preamble Pc Byte 1 | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| 11H | Burst Preamble Pd Byte 0 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| 12H | Burst Preamble Pd Byte 1 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| 13H | Q-subcode Address/Control | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 |
| 14H | Q-subcode Track | Q17 | Q16 | Q15 | Q14 | Q13 | Q12 | Q11 | Q10 |
| 15H | Q-subcode Index | Q25 | Q24 | Q23 | Q22 | Q21 | Q20 | Q19 | Q18 |
| 16H | Q-subcode Minute | Q33 | Q32 | Q31 | Q30 | Q29 | Q28 | Q27 | Q26 |
| 17H | Q-subcode Second | Q41 | Q40 | Q39 | Q38 | Q37 | Q36 | Q35 | Q34 |
| 18H | Q-subcode Frame | Q49 | Q48 | Q47 | Q46 | Q45 | Q44 | Q43 | Q42 |
| 19H | Q-subcode Zero | Q57 | Q56 | Q55 | Q54 | Q53 | Q52 | Q51 | Q50 |
| 1AH | Q-subcode ABS Minute | Q65 | Q64 | Q63 | Q62 | Q61 | Q60 | Q59 | Q58 |
| 1BH | Q-subcode ABS Second | Q73 | Q72 | Q71 | Q70 | Q69 | Q68 | Q67 | Q66 |
| 1CH | Q-subcode ABS Frame | Q81 | Q80 | Q79 | Q78 | Q77 | Q76 | Q75 | Q74 |

Note: When PDN pin goes “L”, the registers are initialized to their default values.

When RSTN bit goes “0”, the internal timing is reset and the registers are initialized to their default values.

All data can be written to the register even if PWN bit is “0”.

For addresses from 1DH to 1FH, data must not write.

■ Register Definitions

Reset & Initialize

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|------|-----|-----|-----|-------|-------|-----|------|
| 00H | CLK & Power Down Control | CS12 | BCU | CM1 | CM0 | OCKS1 | OCKS0 | PWN | RSTN |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

RSTN: Timing Reset & Register Initialize

0: Reset & Initialize

1: Normal Operation (Default)

PWN: Power Down

0: Power Down

1: Normal Operation (Default)

OCKS1-0: Master Clock Frequency Select (See Table 2)

CM1-0: Master Clock Operation Mode Select (See Table 1)

BCU: Block start (B), C, U Output Mode (See Table 12)

0: Disable (Default)

1: Enable

CS12: Channel Status Select

0: Channel 1 (Default)

1: Channel 2

Select which channel status is used to derive C-bit buffer, AUDION, PEM, FS3-0, Pc and Pd. The de-emphasis filter is controlled by channel 1 in the parallel control mode.

Format & De-emphasis Control

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------------|------|------|------|------|------|------|------|----|
| 01H | Format & De-em Control | V/TX | DIF2 | DIF1 | DIF0 | DEAU | DEM1 | DEM0 | 0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | RD |
| | Default | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

DEM1-0: 32, 44.1, 48kHz De-emphasis Control (See Table 9)

DEAU: De-emphasis Auto Detect Enable

0: Disable

1: Enable (Default)

DIF2-0: Audio Data Format Control (See Table 16; Default: "110")

V/TX: V/TX Output Select

0: Validity Flag Output. (Default)

This output is updated every fs cycle.

1: TX

Input/Output Control

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|----|------|------|-----|-----|------|------|------|
| 02H | Input/ Output Control 0 | 0 | XTL1 | XTL0 | UCE | TXE | OPS2 | OPS1 | OPS0 |
| | R/W | RD | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

OPS2-0: Output Through Data Select for TX pin (See Table 13; Default: “000”)

TXE: TX pin Output Enable

0: Disable. TX pin outputs “L”.

1: Enable (Default)

UCE: C-bit, U-bit output setting (See Table 12, Default: “0”)

XTL1-0: Reference X’tal frequency Select (See Table 4, Default: 00)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|------|------|------|------|-----|------|------|------|
| 03H | Input/ Output Control 1 | EFH1 | EFH0 | FAST | XMCK | DIV | IPS2 | IPS1 | IPS0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

IPS2-0: Input Recovery Data Select (See Table 10; Default: “000”)

DIV: MCKO2 Output Frequency Select at X’tal Mode (See Table 3)

0: x 1 (Default)

1: x 1/2

XMCK: MCKO2 pit output select (See Table 3)

0: Depends on CM1-0 bits and OCKS1-0 bits (Default)

1: Fixed to X’tal Mode

FAST: PLL Lock Time Select

0: $\leq (15\text{ms} + 384/\text{fs})$ (Default)

1: $\leq (15\text{ms} + 1/\text{fs})$

EFH1-0: INT0 pin Hold Time Select

00: 512/fs

01: 1024/fs (Default)

10: 2048/fs

11: 4096/fs

Mask Control for INT0

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-------|-------|-------|-------|-----|-------|-------|-------|
| 04H | INT0 MASK | MQIT0 | MAUTO | MCIT0 | MULK0 | MV0 | MSTC0 | MAUD0 | MPAR0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

- MPAR0: Mask enable for PAR bit
 0: Mask disable (Default)
 1: Mask enable
- MAUD0: Mask enable for AUDION bit
 0: Mask disable
 1: Mask enable (Default)
- MSTC0: Mask enable for STC bit
 0: Mask disable
 1: Mask enable (Default)
- MV0: Mask enable for V bit
 0: Mask disable
 1: Mask enable (Default)
- MULK0: Mask enable for UNLCK bit
 0: Mask disable (Default)
 1: Mask enable
- MCIT0: Mask enable for CINT bit
 0: Mask disable
 1: Mask enable (Default)
- MAUTO: Mask enable for AUTO bit
 0: Mask disable
 1: Mask enable (Default)
- MQIT0: Mask enable for QINT bit
 0: Mask disable
 1: Mask enable (Default)

When mask is set to “1”, corresponding event does not affect INT0 pin operation.

Mask Control for INT1

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-------|-------|-------|-------|-----|-------|------|-------|
| 05H | INT1 MASK | MQIT1 | MAUT1 | MCIT1 | MULK1 | MV1 | MSTC1 | MAUD | MPAR1 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |

- MPAR1: Mask enable for PAR bit
0: Mask disable
1: Mask enable (Default)
- MAUD1: Mask enable for AUDION bit
0: Mask disable (Default)
1: Mask enable
- MSTC1: Mask enable for STC bit
0: Mask disable
1: Mask enable (Default)
- MV1: Mask enable for V bit
0: Mask disable
1: Mask enable (Default)
- MULK1: Mask enable for UNLCK bit
0: Mask disable
1: Mask enable (Default)
- MCIT1: Mask enable for CINT bit
0: Mask disable
1: Mask enable (Default)
- MAUT1: Mask enable for AUTO bit
0: Mask disable (Default)
1: Mask enable
- MQIT1: Mask enable for QINT bit
0: Mask disable
1: Mask enable (Default)

When mask is set to “1”, corresponding event does not affect INT1 pin operation.

DAT Mask & DTS Detect

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|----|----|----|------|-------|-------|-------|-------|
| 06H | DAT Mask & DTS Detect | 0 | 0 | 0 | DCNT | DTS16 | DTS14 | MDAT1 | MDAT0 |
| | R/W | RD | RD | RD | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

- MDAT0: Mask enable for DAT bit
0: Mask disable
1: Mask enable (Default)
When mask is set to “1”, DAT event does not affect INT0 pin operation.
- MDAT1: Mask enable for DAT bit
0: Mask disable
1: Mask enable (Default)
When mask is set to “1”, DAT event does not affect INT1 pin operation.
- DTS14: DTS-CD 14bit Sync Word Detect
0: Disable
1: Enable (Default)
- DTS16: DTS-CD 16bit Sync Word Detect
0: Disable
1: Enable (Default)
- DCNT: DAT Start ID Counter
0: Disable
1: Enable (Default)

Receiver Status 0

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|------|------|------|-------|----|-----|--------|-----|
| 07H | Receiver status 0 | QINT | AUTO | CINT | UNLCK | V | STC | AUDION | PAR |
| | R/W | RD | RD | RD | RD | RD | RD | RD | RD |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PAR: Parity Error or Bi-phase Error Status

0: No Error

1: Error

This bit goes to “1”, if a Parity Error or Biphase Error is detected in the sub-frame.

AUDION: Audio Bit Output

0: Audio

1: Non Audio

This bit is made by encoding channel status bits.

STC: Sampling Frequency or Pre-emphasis Information Change Detection

0: No detect

1: Detect

This bit goes to “1” when either the FS3-0 or PEM bit changes.

V: Validity of channel status

0: Valid

1: Invalid

UNLCK: PLL Lock Status

0: Lock

1: Unlock

CINT: Channel Status Buffer Interrupt

0: No change

1: Changed

This bit goes to “1” when C-bit stored in register addresses 0AH to 0EH changes.

AUTO: Non-PCM Auto Detect

0: No detect

1: Detect

QINT: Q-subcode Buffer Interrupt

0: No change

1: Changed

This bit goes to “1” when Q-subcode stored in register addresses 13H to 1CH changes.

STC, QINT, CINT and PAR bits are initialized when 07H is read.

Receiver Status 1

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|-----|-----|-----|-----|-----|-----|-------|------|
| 08H | Receiver status 1 | FS3 | FS2 | FS1 | FS0 | PEM | DAT | DTSCD | NPCM |
| | R/W | RD | RD | RD | RD | RD | RD | RD | RD |
| | Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

NPCM: Non-PCM Bit Stream Auto Detection

0: No detect

1: Detect

DTSCD: DTS-CD Bit Stream Auto Detection

0: No detect

1: Detect

DAT: DAT Start ID Detect

0: No detect

1: Detect

DAT bit is initialized when 08H is read.

PEM: Pre-emphasis Detect

0: OFF

1: ON

This bit is made by encoding channel status bits.

FS3-0: Sampling Frequency detection (See Table 5)

Receiver Status 1

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|----|----|----|----|----|------|------|
| 09H | Receiver status 1 | 0 | 0 | 0 | 0 | 0 | 0 | QCRC | CCRC |
| | R/W | RD | RD | RD | RD | RD | RD | RD | RD |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

CCRC: Cyclic Redundancy Check for Channel Status

0: No error

1: Error

This bit is enabled only in professional mode and only for the channel selected by the CS12 bit.

QCRC: Cyclic Redundancy Check for Q-subcode

0: No error

1: Error

Receiver Channel Status

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|--------------------------|-----------------|------|------|------|------|------|------|------|
| 0AH | RX Channel Status Byte 0 | CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
| 0BH | RX Channel Status Byte 1 | CR15 | CR14 | CR13 | CR12 | CR11 | CR10 | CR9 | CR8 |
| 0CH | RX Channel Status Byte 2 | CR23 | CR22 | CR21 | CR20 | CR19 | CR18 | CR17 | CR16 |
| 0DH | RX Channel Status Byte 3 | CR31 | CR30 | CR29 | CR28 | CR27 | CR26 | CR25 | CR24 |
| 0EH | RX Channel Status Byte 4 | CR39 | CR38 | CR37 | CR36 | CR35 | CR34 | CR33 | CR32 |
| R/W | | RD | | | | | | | |
| Default | | Not initialized | | | | | | | |

CR39-0: Receiver Channel Status Byte 4-0

All 40 bits are updated at the same time every bock (192 frames) cycle.

Burst Preamble Pc/Pd in non-PCM encoded Audio Bitstreams

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|--------------------------|-----------------|------|------|------|------|------|-----|-----|
| 0FH | Burst Preamble Pc Byte 0 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| 10H | Burst Preamble Pc Byte 1 | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| 11H | Burst Preamble Pd Byte 0 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| 12H | Burst Preamble Pd Byte 1 | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| R/W | | RD | | | | | | | |
| Default | | Not initialized | | | | | | | |

PC15-0: Burst Preamble Pc Byte 0 and 1

PD15-0: Burst Preamble Pd Byte 0 and 1

Q-subcode Buffer

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|-----------------------------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| 13H | Q-subcode Address / Control | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 |
| 14H | Q-subcode Track | Q17 | Q16 | Q15 | Q14 | Q13 | Q12 | Q11 | Q10 |
| 15H | Q-subcode Index | Q25 | Q24 | Q23 | Q22 | Q21 | Q20 | Q19 | Q18 |
| 16H | Q-subcode Minute | Q33 | Q32 | Q31 | Q30 | Q29 | Q28 | Q27 | Q26 |
| 17H | Q-subcode Second | Q41 | Q40 | Q39 | Q38 | Q37 | Q36 | Q35 | Q34 |
| 18H | Q-subcode Frame | Q49 | Q48 | Q47 | Q46 | Q45 | Q44 | Q43 | Q42 |
| 19H | Q-subcode Zero | Q57 | Q56 | Q55 | Q54 | Q53 | Q52 | Q51 | Q50 |
| 1AH | Q-subcode ABS Minute | Q65 | Q64 | Q63 | Q62 | Q61 | Q60 | Q59 | Q58 |
| 1BH | Q-subcode ABS Second | Q73 | Q72 | Q71 | Q70 | Q69 | Q68 | Q67 | Q66 |
| 1CH | Q-subcode ABS Frame | Q81 | Q80 | Q79 | Q78 | Q77 | Q76 | Q75 | Q74 |
| R/W | | RD | | | | | | | |
| Default | | Not initialized | | | | | | | |

Q2-81: Q-subcode (Figure 20 and Figure 21)

All 80 bits are updated at the same time every sync code cycle for Q-subcode.

■ Burst Preambles in non-PCM Bitstreams

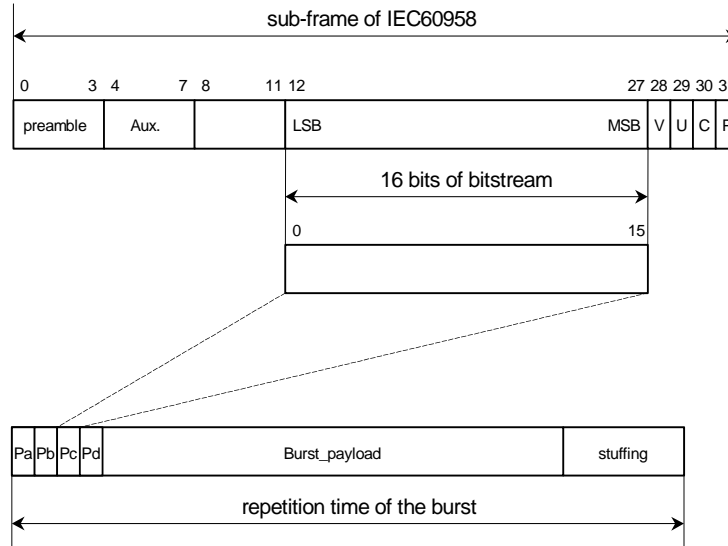


Figure 41. Data structure in IEC60958

| Preamble word | Length of field | Contents | Value |
|---------------|-----------------|-------------|-----------------|
| Pa | 16 bits | sync word 1 | 0xF872 |
| Pb | 16 bits | sync word 2 | 0x4E1F |
| Pc | 16 bits | Burst info | see Table 18 |
| Pd | 16 bits | Length code | numbers of bits |

Table 17. Burst preamble words

| Bits of Pc | Value | Contents | Repetition time of burst in IEC60958 frames |
|------------|----------|---|---|
| 0-4 | 0 | data type NULL data | ≤4096 |
| | 1 | Dolby AC-3 data | 1536 |
| | 2 | reserved | |
| | 3 | PAUSE | |
| | 4 | MPEG-1 Layer1 data | 384 |
| | 5 | MPEG-1 Layer2 or 3 data or MPEG-2 without extension | 1152 |
| | 6 | MPEG-2 data with extension | 1152 |
| | 7 | MPEG-2 AAC ADTS | 1024 |
| | 8 | MPEG-2, Layer1 Low sample rate | 384 |
| | 9 | MPEG-2, Layer2 or 3 Low sample rate | 1152 |
| | 10 | reserved | |
| | 11 | DTS type I | 512 |
| | 12 | DTS type II | 1024 |
| | 13 | DTS type III | 2048 |
| | 14 | ATRAC | 512 |
| | 15 | ATRAC2/3 | 1024 |
| 16-31 | reserved | | |
| 5, 6 | 0 | reserved, shall be set to "0" | |
| 7 | 0 | error-flag indicating a valid burst_payload | |
| | 1 | error-flag indicating that the burst_payload may contain errors | |
| 8-12 | | data type dependent info | |
| 13-15 | 0 | bit stream number, shall be set to "0" | |

Table 18. Fields of burst info Pc

■ Non-PCM Bitstream timing

1) When Non-PCM preamble is not coming within 4096 frames.

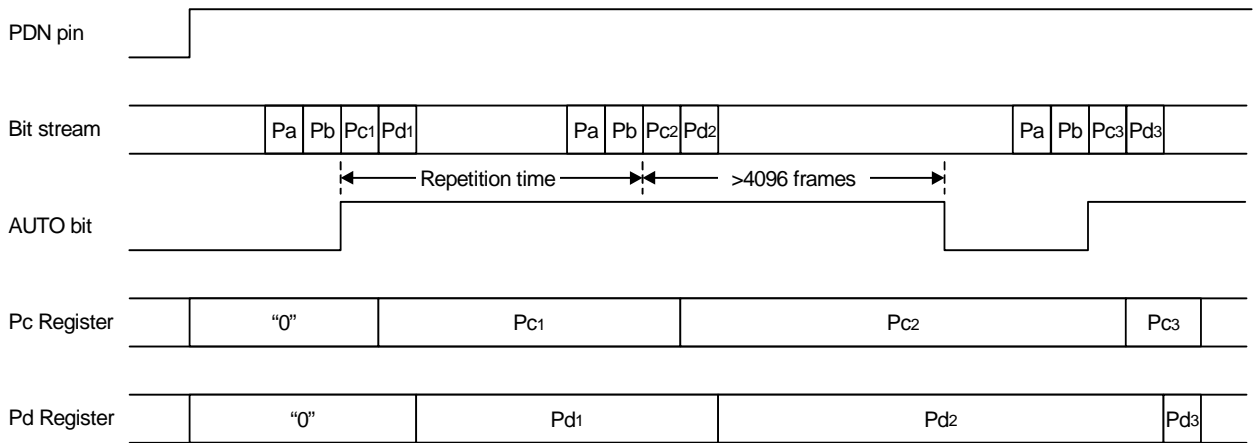


Figure 42. Timing Example 1

2) When Non-PCM bitstream stops (When MULK0 bit = "0")

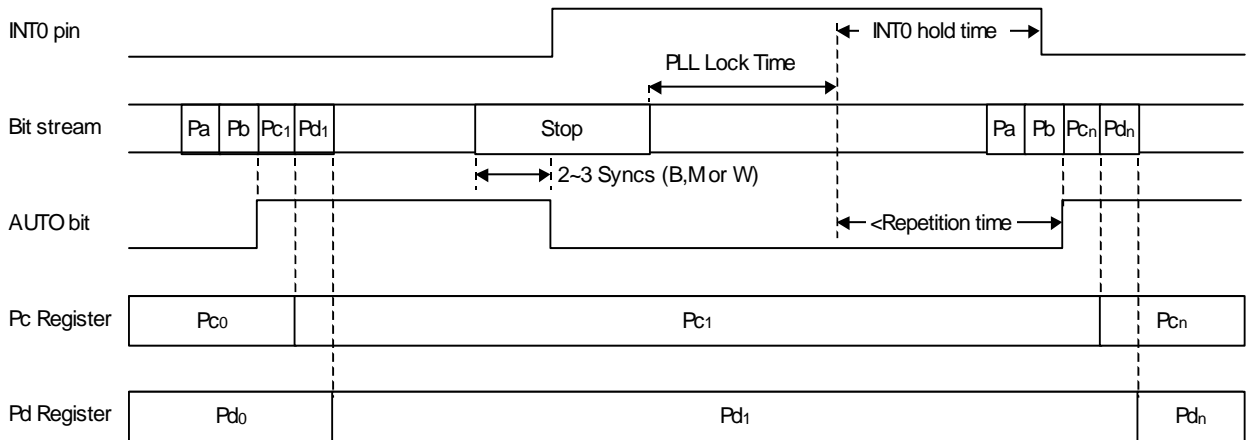


Figure 43. Timing Example 2

SYSTEM DESIGN

Figure 44 shows the example of system connection diagram for serial control mode.

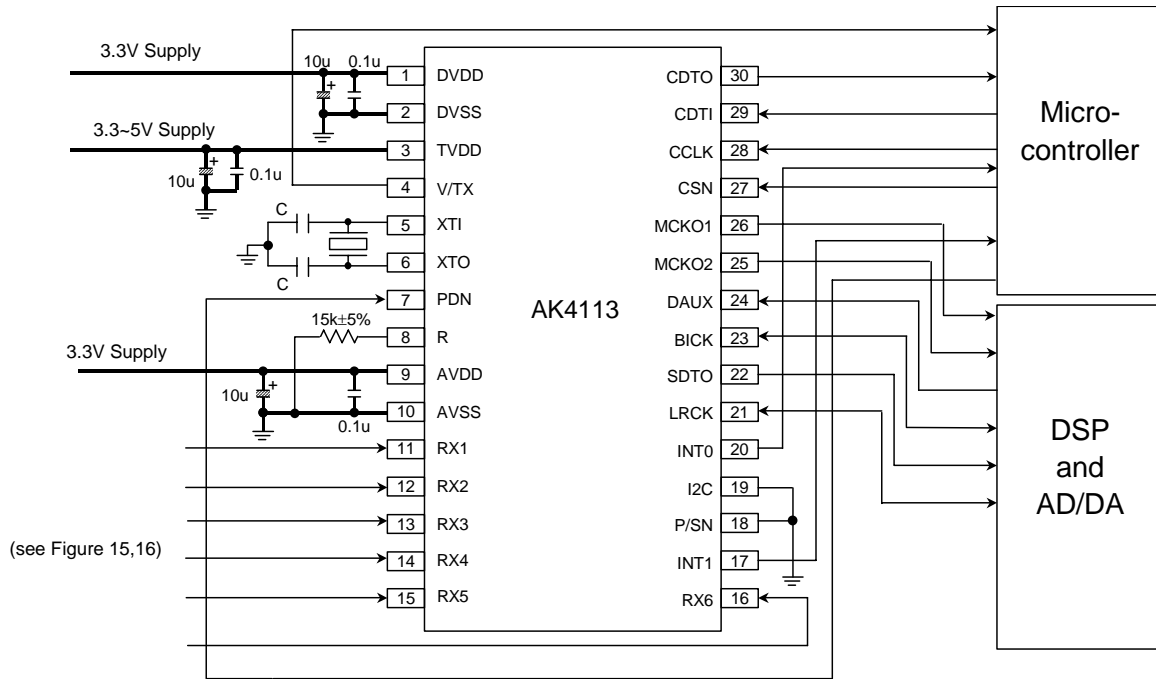


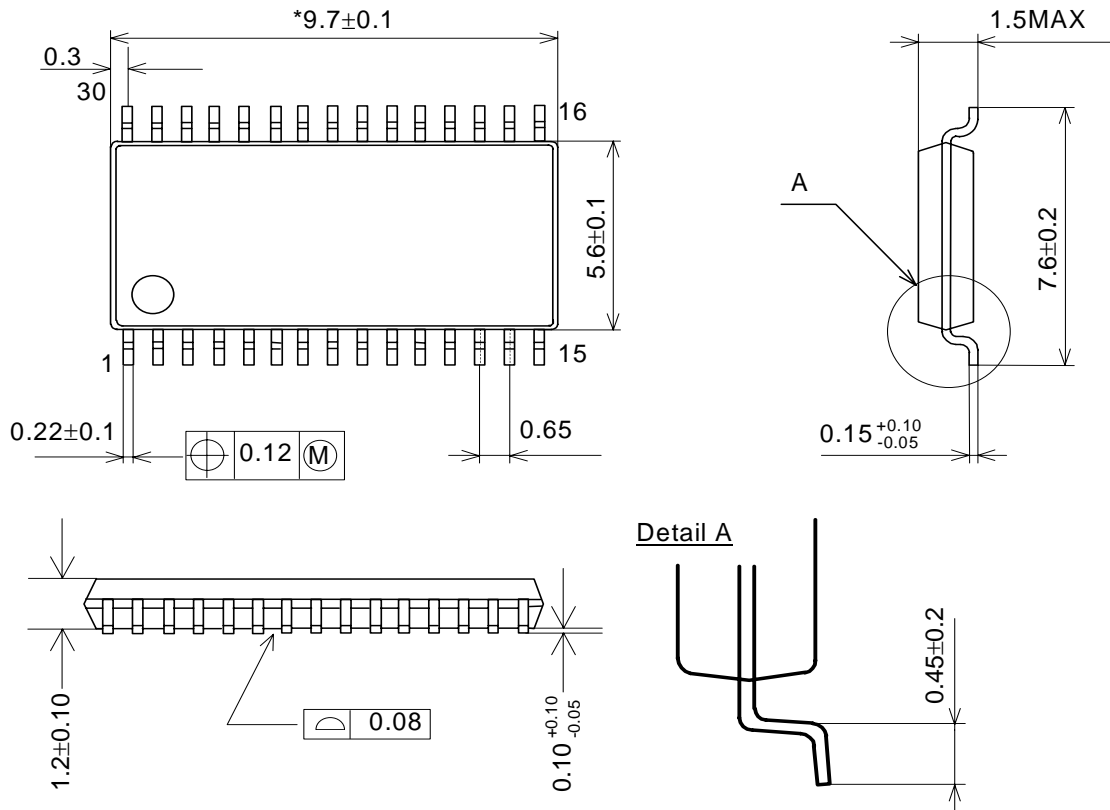
Figure 44. Typical Connection Diagram (4-wire serial control mode)

Notes:

- For setting of XTL1-0 bits, refer to Table 4.
- "C" depends on the crystal oscillator
- AVSS and DVSS must be connected the same ground plane.
- Digital signals, especially clocks, should be kept away from the R pin in order to avoid an effect to the clock jitter performance.

PACKAGE

30pin VSOP (Unit: mm)

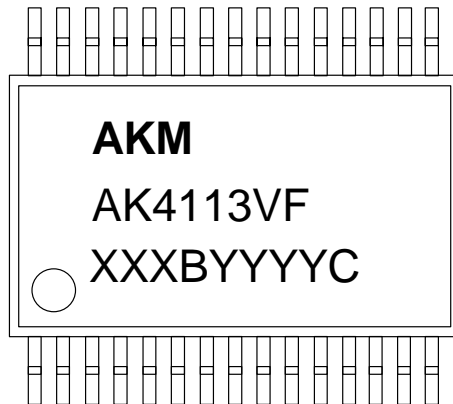


NOTE: Dimension "*" does not include mold flash.

■ **Material & Lead finish**

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder plate (Pb Free)

MARKING



XXXXYYYYC: Date code identifier

XXXB: Lot number (X : Digit number, B : Alpha character)

YYYYC: Assembly date (Y : Digit number C : Alpha character)

Revision History

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|-----------------|----------|---------------|---------|------------------------------------|
| 04/10/20 | 00 | First Edition | | |
| 05/03/08 | 01 | Error Correct | 3, 5, 7 | Pin Name: #14; RX4/IPS2 → RX4/DIF2 |

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